$9.95

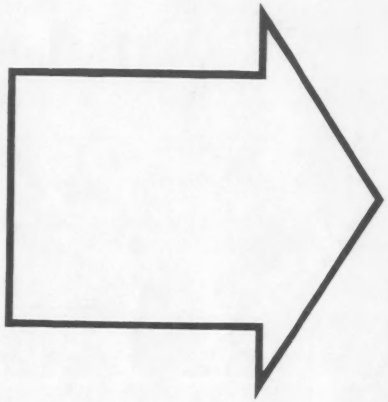
BIPOLAR LSI 1984 Databook

FIFTH EDITION

Monolithic MMI Memories

BIPOLAR LSI

DATABOOK
FIFTH EDITION



Monolithic Memories®

Introduction

This book has been prepared to give the user a concise list of all Bipolar LSI Products offered by Monolithic Memories. It is divided by products into sections on Military Products Division, PROMs, ROMs, Character Generators. PLE™, PAL®/HAL® Circuits, HMSI™, FIFOs, Memory Support Series, Arithmetic Elements and Logic, Multipliers/Dividers, Interface and General Information which has a Listing of Available Literature. Each section has been designed to allow the user the most useable format for the products described. The PROM, ROM, and Character Generator sections give data in the "generic" form allowing a quick review of the trade-off between devices. Inserted also are newer PROM data sheets shown with more detail. Cross references and selection guides are given where applicable. FIFO, PAL, HMSI, Arithmetic Elements, Multipliers/Dividers and Interface data sheets are shown in detail for each product. This LSI data book was formatted with you, the user, in mind. For more information, contact the local Monolithic Memories sales representative or franchised distributor. In section 16 of this book Monolithic Memories Sales Reps and Franchised Distributor are listed, for your convenience.

Prices

All prices are in U.S. dollars and are subject to change without notice.

Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of $1000 ($250 per line item) except for the following:

HAL® Circuits—The $2-3K N.R.E. and mask charge can be amortized over the initial production commitment. The minimum initial production commitment is 5K units within one year; the minimum quantity per release is 1K.

ProPAL Circuits—When purchased the initial phase of a HAL Circuit, there is no additional N.R.E and there is a nominal adder for programming and testing. The minimum quantity per release is 500 units. When purchased without a follow-on the $1-2K N.R.E. can be amortized over a minimum initial production commitment of 2500 units.

ROMs—There is a minimum order requirement of $2500 and 500 units plus a one time (per bit pattern) mask charge of $750.

Terms

70%/30 days, 30%/45 days from date of invoice, FOB Sunnyvale, California.

Commercial/Military Codes

The letter codes "C" and "M" are used to denote commercial and military level device limits as follows:

Commercial—TA = 0°C to +75°C
VCC = 5V ±5%

Military—TA = −55°C to +125°C
VCC = 5V ± 10%

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

PACKAGE CODE	DESCRIPTION
J	Ceramic dual-in-line (600 mil wide)
JS	Ceramic dual-in-line (300 mil wide)
N	Plastic dual-in-line (600 mil wide)
NS	Plastic dual-in-line (300 mil wide)
D	Side brazed ceramic dual-in-line
F	Flat Pack
L	Leadless
T	Inverted "D" package

See "Part Numbering Systems" for complete part descriptions.

General

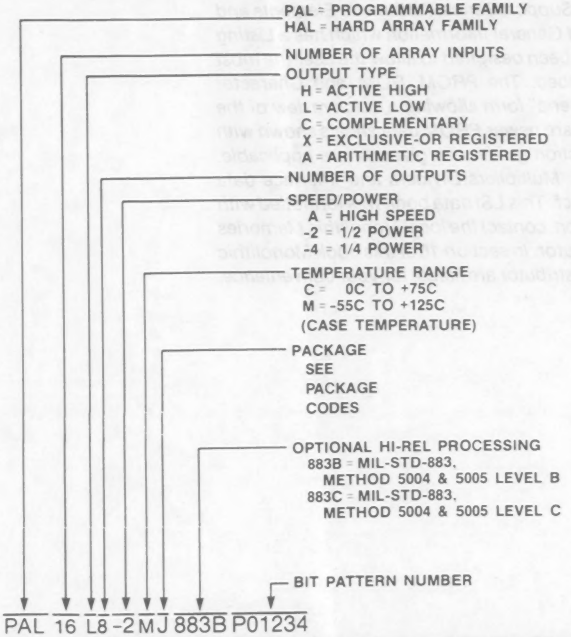
Unless otherwise specified the standard packages are "J" or "N" packages. In some instances the "D" package is the only package available. Other non-standard packages and other military Level 883B devices not listed may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

Screening Options

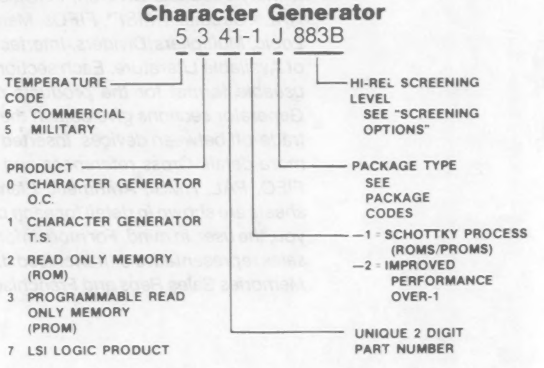
PROCESS LEVEL	PART MARKING
MIL-STD-883 Method 5004 and 5005 Level B	883B (Suffix)
MIL-STD-883 Method 5004 and 5005 Level C	883C (Suffix)

Part Numbering Systems

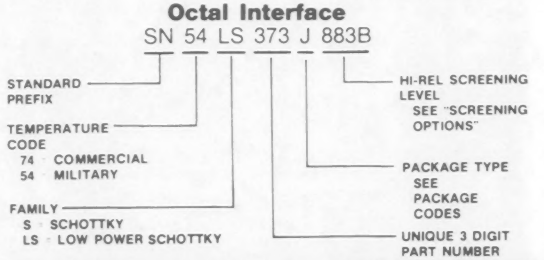
PAL® Circuits Programmable Array Logic



PROMS — ROMS Character Generator



Octal Interface



Ordering Military Information

Products have different numbering formats. These formats are shown in the following columns with detailed descriptions of what each part means. These formats in conjunction with the product selection guides by function will enable you to select the proper military level component.

PAL®
Programmable Array Logic

PAL 14 L 4 M J 883B

- PROGRAMMABLE ARRAY LOGIC FAMILY
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - H = Active High
  - L = Active Low
  - C = Complementary
  - R = Registered
  - A = Arithmetic Registered
  - X = Exclusive or Registered
- NUMBER OF OUTPUTS
- POWER SELECTION
- TEMPERATURE RANGE
  - M = -55°C to +125°C
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack
  - L = Leadless Chip
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Level B
  - 883S = Mil-Std-883, Level S

Standard Performance PROMs

5 3 41-2 J 883B

- TEMPERATURE CODE
  - 6 = Commercial
  - 5 = Military
- PRODUCT
  - 3 = Programmable Read Only Memory (PROM)
- UNIQUE 2 DIGIT PART NUMBER
- PERFORMANCE
  - -1 = Schottky Process (PROMS)
  - -2 = Improved Performance Over-1
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack
  - L = Leadless Chip
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Level B
  - 883S = Mil-Std-883, Level S

Octal Interface

SN 54 LS 373 J 883B

- STANDARD PREFIX
- TEMPERATURE RANGE
  - 54 = -55°C to +125°C
- FAMILY
  - S = Schottky
  - LS = Low Power Schottky
- UNIQUE 3-DIGIT PART NUMBER
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack
  - L = Leadless Chip
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Level B
  - 883S = Mil-Std-883, Level S

High Performance PROMs

5 3 S 32 8 1 A J 883B

- TEMPERATURE
  - 6 = Commercial
  - 5 = Military
- PRODUCT
  - 3 = Programmable Read Only Memory (PROM)
- FAMILY
  - S = Schottky
  - RA = Registered Asynchronous
  - RS = Registered Synchronous
  - D = Diagnostic
  - DA = Diagnostic Asynchronous
- MEMORY SIZE
  - 0 = 256 bit
  - 1 = 1024 bit
  - 2 = 2048 bit
  - 4 = 4096 bit
  - 8 = 8192 bit
  - 16 = 16384 bit
  - 32 = 32768 bit
- NUMBER OF OUTPUTS
  - 4 = 4 bit
  - 8 = 8 bit
- OUTPUT DESIGNATOR
  - 0 = Open Collector
  - 1 = Three State
  - 3 = Two State
- PERFORMANCE
  - None = Standard
  - A = Enhanced
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack
  - L = Leadless Chip
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Level B
  - 883C = Mil-Std-883, Level S

PLE™
Programmable Logic Element

PLE 5 P 8 M J 883B

- PROGRAMMABLE LOGIC ELEMENT
- NUMBER OF INPUTS
- OUTPUT TYPE
  - P = Programmable Polarity
  - R = Registered
- NUMBER OF OUTPUTS
- TEMPERATURE RANGE
  - M = -55°C to +125°C
- PACKAGE TYPE
  - J = Ceramic Dip
  - F = Flat Pack
  - L = Leadless Chip
- HI-REL SCREENING LEVEL
  - 883B = Mil-Std-883, Level B
  - 883S = Mil-Std-883, Level S

JAN PART NUMBERING SYSTEM

J M 38510/ 503 01 B R A

- **J** — JAN Designator. Parts cannot be marked with a "J" unless qualified and approved for listing on QPL.
- **M 38510/** — General Procurement Spec
- **503** — Defines Device Type
  - Refers to Detail Spec.
  - 203 1K PROM (256 x 4)
  - 204 2K PROM (512 x 4)
  - 206 4K PROM (1K x 4)
  - 207 256 PROM (32 x 8)
  - 208 4K PROM (512 x 8)
  - 209 8K PROM (1K x 8, 2K x 4)
  - 210 16K PROM (2K x 8, 4K x 4)
  - 211 32K PROM (4K x 8)
  - 324 Octal Buffer
  - 325 Octal Flip Flops
  - 328 Octal Transceiver
  - 503 Programmable Array Logic
  - 504 Programmable Array Logic
- **01** — Processing Level
  - Class S
  - Class B
  - Class C
- **B** — Case Outline
- **R** — Package Type
  - E 16 Lead 1/4 x 7/8 Dip
  - F 16 Lead 1/4 x 3/8 Flatpack
  - J 24 Lead 1/2 x 1 1/4 Dip
  - K 24 Lead 3/8 x 5/8 Flatpack
  - R 20 Lead 1/4 x 1'—' 1/16 Dip
  - V 18 Lead 1/4 x 15/16" Dip
  - X * 20 Lead .35 x .35 LCC
  - X * * 24 Lead 3/8 x 3/8 Flatpack
  - Y * 20 Lead 3/8 x 3/8 Flatpack
  - Y * * 20 Lead 5/16 x 1.0 Dip
  - Z 24 Lead 1/4 x 3/8 Flatpack

  * PAL Slash Sheet
  * * PROM Slash Sheet
- **A** — Lead Finish
  - A Hot Solder Dip
  - B Tin Plate
  - C Gold Plate
  - X Any Lead Finish

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Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." MIL-M-38510 plays a significant role in structuring Monolithic Memories' quality program.

Monolithic Memories' facilities in Sunnyvale were certified in June of 1977 by DESC, Defense Electronics Supply Center, to manufacture and qualify to Class B and Class C Schottky Bipolar PROMs, ROMs and RAMs in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at Monolithic Memories is on process control as reflected in the use of many monitors and audits rather than gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

Monolithic Memories' advanced low-power Schottky TTL process uses such techniques as redundant masking to reduce random defects and self-aligning masking to reduce active chip area. Although more costly than the standard SSI or MSI Schottky TTL processes, these approaches yield better quality, increased reliability and lower overall cost due to higher net die per wafer. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design-process compatibility by careful sample selection of lots reflecting process variable extremes.

Screening

Much of the assembly (packaging only) is performed offshore at our Penang, Malaysia facility. The facility has been qualified and is routinely monitored for conformance to MIL-STD-883 by Monolithic Memories' military customers as well as by Monolithic Memories' Quality Control Department. All standard military hermetic Monolithic Memories products are 100% screened to MIL-STD-883 Class C. This includes:

- Pre-cap inspection.*
- High-temperature storage at 150°C.
- Temperature cycling, –65°C to +150°C.
- Constant acceleration.
- Fine and gross leak.
- Final electrical test.
- Q.A. sample acceptance testing.

*Modified for LSI.

Standard commercial hermetic product receives the following screens and monitors to insure the highest possible product quality.

- Pre-cap inspection*
- High temperature storage
- Temperature cycle
- Constant acceleration
- Fine and gross leak

} Daily monitors in lieu of 100% screening which insure the AQL levels before are met or exceeded.

- Final electrical test

*Modified MIL-STD-883 Pre cap.

The product assurance levels which Monolithic Memories guarantees are listed in the table on this page.

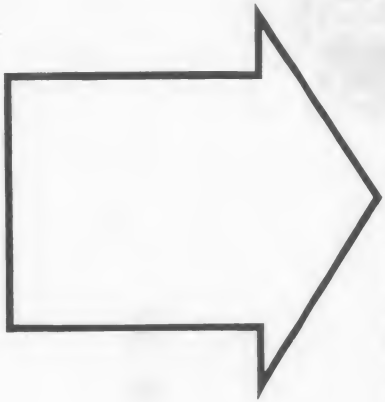
Reliability Engineering maintains product surveillance through routine sampling and submission to MIL-STD-883, method 5005, qualification testing. Additional step-stress and extended (limit) testing conditions are used when warranted. In general, failure rates have been found to be two orders of magnitude better than MIL-HDBK-217 estimates.

The quality organization is defined into three departments:

- Quality control
- Quality assurance
- Reliability assurance

Quality Assurance (AQL) Levels

TEST	LEVEL I COMMERCIAL (%)	LEVEL II MILITARY (%)
Hermeticity (includes fine and gross)	0.65	0.4
Electrical		
DC at 25°C	.40	.25
Functional at 25°C	.40	.25
AC at 25°C	.65	.40
DC at Temperature Extremes	.65	.65
Functional at Temperature Extremes	.65	.65
AC at Temperature Extremes	1.5	1.5



MILITARY CONTENTS

Introduction

In August, 1982 Monolithic Memories Inc. formed a Military Products Division. Although Monolithic Memories has participated in the defense market for some time, we feel that by focusing on this very demanding customer base with a totally dedicated resource, we can provide aerospace and military systems manufacturers with a new industry standard of service and responsiveness.

Monolithic Memories offers devices to a full complement of military screening levels:

Monolithic Memories Inc. Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B

In addition, we welcome the opportunity to review and quote to customer source control drawings. Our spec Review group is measured to a 2 week turn-around time on drawing reviews, so our customers will receive a timely response on our ability to meet custom requirements.

Monolithic Memories is Certified by the Defense Electronics Supply Center to assemble and test Mil-M-38510 Class B devices at its Sunnyvale, California facility.

Offshore Assembly facilites are located in Penang, Malaysia.

Standard Processing Flows

Monolithic Memories Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows which the Military Products Division currently operates to include:

Modified Level S
JAN 38510
DESC Drawing Program
Mil-Std 883 Class B

In addition, these flows are expanded to provide for factory programming on PAL circuits and PROMS, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost — no price adders for custom processing.
- Improved lead time — no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

For your reference, we have included our Modified Level S flow and our Mil-Std-883 Class B flow. For your planning purposes, we have included typical throughput times for each operation, as product proceeds through the processing flow.

It is the policy of Monolithic Memories, to always operate to the most current revision of Mil-Std-883.

Standard Military Flow Chart

SCREENING	MODIFIED LEVEL S	REQUIREMENT	AVERAGE THROUGHPUT TIME
	MIL-STD-883, METHOD 5004		DAYS
S.E.M.	2018	Sample	10
Assembly	USA assembly		10
Non-destruct bond pull	2023 (sample)	LTPD = 5 REJ = 0 SS = 2, all wires	2
Die shear	2019 (sample)	REJ = 0	2
Internal visual	2010 cond. A (modified)	100%	10
Stabilization bake	1008	100%	2
Temperature cycling	1010	100%	2
Constant acceleration	2001 test cond. D or E Y_1 orientation only	100%	2
Seal A) Fine B) Gross	1014 cond. A cond. C	100%	3
Particle impact noise detection (PIND)	2020 cond. A only	100%	5
Interim electrical parameters	Per applicable device specification TA = 25°C only programming step	100%	4
Serialization		100%	2
X-RAY	2012 two views X and Y axis only	100%	3
Interim electrical parameter	Per applicable device specification TA = 25°C only (delta's when required)	100%	2
Burn in	1015 cond. D TA = +125°C, (min.) time = 240HRS	100%	15
Post electrical parameters	Per applicable device specification TA = 25°C only (delta's when required)	100%	2
Percent defect allowable	PDA = 5%	100%	2
Delta calculations (when applicable)	Per applicable device specification		2
Final electrical parameters (hot and cold extremes)	Per applicable device specification	100%	6
Freeze out (nichrome only)	Option	Option	5
Final electrical (delta's when applicable)	Per applicable device specification TA = 25°C only	100%	2
Delta calculations (when applicable)	Per applicable device specification		2
Group A lot	5005 Level S		2
Group B inspection lot	5005 class B		5
Group C	5005 class B	Every 3 months	40
Group D	5005 class B	Every 6 months	20
External visual	2009	100%	2

Average throughput times are for your information to give you a better understanding of the time involved for each processing step. Since delivery time could be extended due to die availability, or shortened by utilizing partially processed inventories, the above throughput times listed should not be interpreted as delivery lead time. Contact your local sales representative for delivery lead time on specific part types.

Standard Military Flow Chart

CLASS B	REQUIREMENT	AVERAGE THROUGHPUT TIME
MIL-STD-883, METHOD 5004		DAYS
Typically offshore assembly		10
2010 cond. B	100%	5
1008	100%	2
1010	100%	2
2001 test cond. D or E Y_1 orientation only	100%	2
1014 cond. A cond. C	100%	3
		2
Per applicable device specification TA = 25°C only	100%	2
1015 cond. C or D TA = +125°C (min.), time = 160HRS	100%	10
Per applicable device specification TA = 25°C only	100%	2
PDA = 10%		2
Per applicable device specification	100%	6
5005 class B		3
5005 class B		5
5005 class B Generic Data	Every 3 months	40
5005 class B available in lieu of	Every 6 months	20
2009 lot qualification	100%	2

Die Information

Introduction

Monolithic Memories' "Die" program is a quality oriented, comprehensive plan, designed to serve the expanding hybrid market.

We believe that quality is the natural result of our concentrated emphasis in reliability at the design development, process and manufacturing stages.

The chip reliability is enhanced by our "Test Philosophy". The die is screened to tighten electrical limits. As a result, we can fully guarantee performance to the data sheet parameter conditions and limits specified for each packaged product.

Testing

All die is 100% probed at 25°C to a temperature correlated test program. Temperature simulation (-55°C to 125°C or 0°C to 75°C) is accomplished via V_{CC} variation and test limit guardbanding for DC and functional parameters.

NOTE: AC parameters are guaranteed by design and periodic statistical sampling.

Visual Inspection

- 100% inspection to 2010B (unless otherwise specified)
- Silox Inspection
- X200 High Magnification
- Wafer saw completely through
- No ink on die

Physical Characteristics

- All die are passivated
- Aluminum or aluminum/copper metallization
- May be assembled by industry standard die attach, lead bond and sealing techniques for LSI Bi-Polar products
- 15/20 mils thick typically (with no gold backing)

Quality Control: Lot Acceptance

2010B Visual Inspection

- 0.4 AQL for Military product lots

NOTE: The visual criteria is guaranteed within the periphery of the bond pads unless otherwise negotiated.

Traceability

- To original wafer fab runs

Packaging

- Waffle pack; sized for the specific product
- One waffle pack per plastic bag
- Vacuum seal with dessicant
- As a minimum, each waffle pack is labeled with:
  - Monolithic Memories part number
  - Date indicating lot acceptance

Standard Shipment Data

- 1 copy device bonding diagram
- 1 copy of device metallization layer
- 1 copy wafer fab trace (military die shipments only)

Processing Environment

Die is processed and handled under the specifically controlled environments delineated by Fed.-Std-209.

Other Capabilities

When required, the following options are available. Contact the factory.

- Package sample testing
- Wafer lot qualification
- Custom flows

Ordering Information

- Monolithic Memories part number plus "X" in lieu of the package letter designation
- Please submit all applicable source control drawings, or documents for review
- Specify all non-standard requirements, i.e. die thickness, visual requirements

Die Flow Traveler

SEQ	TEST	TEST CONDITIONS	IN	OUT	OPER.	DATE
	Wafer Lot Dispatch (MPS8004) _____ (MPS9522) _____					
	Wafer Sort (MPS8100) _____ (MPS9522) _____	☐ Wafer Sort Guard Band Probe for Mil Temp Operation (-55°C to + 125°C) Only One Reprobe Allowed				
	Wafer Lot Dispatch (MPS8004) _____ (MPS9522) _____					
	Saw Through (MPS40367) _____ (MPS40346) _____	Record Die trace # on Die prep run card Saw wafer completely through!				
	Clean (MPS40432) _____	Record Die trace # on Die prep run card				
	Plate (MPS40364) _____	Uninked Die Only!				
	Die Sort Visual Inspection (MPSSPD40900) ___	Mil-Std-883 Method 2010 Cond. B				
	Final Plate (MPS9522) _____	Plate Die in proper size waffle plate (ie) Die should not be able to rotate in cavity or protrude above plate.				
	2nd Optical Q.C. Gate (MPS41265) _____	Mil-Std-883 Method 2010 Cond. B 200 X Magnification AQL = 0.4% Record date of acceptance on waffle pack				
	Q.C. Visual Decision Point (MPS9522) _____	Lot must meet 0.4% AQL ☐ Accept ☐ Reject Reject lots return to production for 100% visual rescreen.				
	Pack And Vacuum Seal (MPS9522) _____	Place only one waffle pack per bag. Do not stack waffle packs, package each waffle pack of die in a plastic bag, vacuum seal with dessicant and moisture indicator. Package label must be visible.				
	Dispatch (MPS26895) _____					
	Data Pack / To Bonded Stock (MPS26000) _____ (MPS9511) _____	1 copy of device bonding diagram 1 copy of device top layer (blue line) 1 copy of fab trace				
	QA III (MPS21065) _____					
	Ship (MPS9520) _____					

JAN Program

Monolithic Memories is certified by the Defense Electronics Supply Center to fabricate wafers in both our 3- and 4-inch fab lines and to assemble and test MIL-M-38510 Class B PROMs and PAL circuits in our Sunnyvale facilities. Monolithic Memories has, in addition, been awarded full laboratory suitability to conduct all qualification and quality conformance testing in accordance with MIL-STD-883, Method 5005.

Monolithic Memories has listed in the Qualified Parts List Part I, a 5301-ID (M38510/20302BEC) and in Part II, a PAL10H8J (M38510/50301BRA), PAL14H4J (M38510/50303BRA), PAL10L8J (M38510/50306BRA) and PAL16R4J (M38510/50404BRA).

Near Future QPL I plans include the:

PAL10H8J	PAL16R6AJ
PAL14H4J	53S441J (1K X 4 PROM)
PAL10L8J	53S1681J (2K X 8 PROM)
PAL16R4AJ	
PAL16L8AJ	53S841J (2K X 4 PROM)
PAL16R8AJ	53S3281J (4K X 8 PROM)

Selected devices will be further qualified in leadless chip carriers and cerpacs.

Long term QPL I plans include FIFO's, Low-Power PAL circuits and Octal Interface.

Our goal in the Military Products Division is to support the JAN38510 Program with a continual flow of new high-performance, Advanced Technology Products.

Monolithic Memories Products for which slash sheet specifications currently exist are listed in the "M38510 Slash Sheet Cross Reference to Generic Part Number."

M38510
Slash Sheet Cross Reference to Generic Part Number

M38510	01	02	03	04	05	06	07	08	09
203	5300-1	5301-1							
204	53S240	53S241							
206	53S440	53S441							
207	53S080	53S081							
208	5340-2	5341-2		5348-2	5349-2				
209	53S840	53S841	5380-2	5381-2					
210	53S1680	53S1681			(Will be adding 53S1641)				
211	53S3280	53S3281							
324	54LS240	54LS241	54LS244						
325	54LS273	54LS373	54LS374	54LS377					
328			54LS245						
503	10H8	12H6	14H4	16H2	16C1	10L8	12L6	14L4	16L2
504	16L8	16R8	16R6	16R4	16X4	16A4			

DESC Drawing Program

Monolithic Memories is an active participant in the DESC Drawing Program. For contracts invoking MIL-STD-454 we offer our full PAL product line to DESC Drawings 81035 and 81036. The idea behind the DESC Drawing Program is to standardize MIL-STD-883B microcircuits where fully qualified JAN product is not available. The advantage to the user is that DESC Drawings are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Since semiconductor demand is on the rise, and lead times will be a major concern, DESC Drawings should always be considered to improve availability over source control drawings.

Monolithic Memories dual marks PAL devices with both the Generic part number and the DESC Drawing number. PAL products can be procured to either part number as a standard product, through both OEM and Distributor Channels.

The following cross reference will allow you to determine the appropriate DESC Drawing part numbers for each PAL product.

Future DESC print activity will include Octal Interface and PROMs. Monolithic Memories will work with DESC to generate drawings for new PAL products as well as our family of FIFO devices.

DESC Drawing/Generic Part Type Cross Reference

DESC DRAWING PART NO.: 81035	01	Y	X
DRAWING NO.	DEVICE TYPE	CASE OUTLINE	LEAD FINISH
PALS: DESC DRAWING	GENERIC PART NUMBER	DESC DRAWING	GENERIC PART NUMBER
8103501 RX	PAL10H8 MJ 883B	8103601 RX	PAL16L8 MJ 883B
8103501 XX	PAL10H8 ML 883B	8103601 XX	PAL16L8 ML 883B
8103501 YX	PAL10H8 MF 883B	8103601 YX	PAL16L8 MF 883B
8103502 RX	PAL12H6 MJ 883B	8103602 RX	PAL16R8 MJ 883B
8103502 XX	PAL12H6 ML 883B	8103602 XX	PAL16R8 ML 883B
8103502 YX	PAL12H6 MF 883B	8103602 YX	PAL16R8 MF 883B
8103503 RX	PAL14H4 MJ 883B	8103603 RX	PAL16R6 MJ 883B
8103503 XX	PAL14H4 ML 883B	8103603 XX	PAL16R6 ML 883B
8103503 YX	PAL14H4 MF 883B	8103603 YX	PAL16R6 MF 883B
8103504 RX	PAL16H2 MJ 883B	8103604 RX	PAL16R4 MJ 883B
8103504 XX	PAL16H2 ML 883B	8103604 XX	PAL16R4 ML 883B
8103504 YX	PAL16H2 MF 883B	8103604 YX	PAL16R4 MF 883B
8103505 RX	PAL16C1 MJ 883B	8103605 RX	PAL16X4 MJ 883B
8103505 XX	PAL16C1 ML 883B	8103605 XX	PAL16X4 ML 883B
8103505 YX	PAL16C1 MF 883B	8103605 YX	PAL16X4 MF 883B
8103506 RX	PAL10L8 MJ 883B	8103606 RX	PAL16A4 MJ 883B
8103506 XX	PAL10L8 ML 883B	8103606 XX	PAL16A4 ML 883B
8103506 YX	PAL10L8 MF 883B	8103606 YX	PAL16A4 MF 883B
8103507 RX	PAL12L6 MJ 883B	8103607 RX	PAL16L8 AMJ883B
8103507 XX	PAL12L6 ML 883B	8103607 XX	PAL16L8 AML883B
8103507 YX	PAL12L6 MF 883B	8103607 YX	PAL16L8 AMF883B
8103508 RX	PAL14L4 MJ 883B	8103608 RX	PAL16R8 AMJ883B
8103508 XX	PAL14L4 ML 883B	8103608 XX	PAL16R8 AML883B
8103508 YX	PAL14L4 MF 883B	8103608 YX	PAL16R8 AMF883B
8103509 RX	PAL16L2 MJ 883B	8103609 RX	PAL16R6 AMJ883B
8103509 XX	PAL16L2 ML 883B	8103609 XX	PAL16R6 AML883B
8103509 YX	PAL16L2 MF 883B	8103609 YX	PAL16R6 AMF883B
		8103610 RX	PAL16R4 AMJ883B
		8103610 XX	PAL16R4 AML883B
		8103610 YX	PAL16R4 AMF883B
PROM: 82008A1 JX	53S3281 MJ 883B	OCTALS: 7801201 RX	54LS240 MJ 883B
82008A1 ZX	53S3281 ML 883B	7704701 RX	54LS244 MJ 883B
		8002101 RX	54LS245 MJ 883B
		7801001 RX	54LS273 MJ 883B
		7801101 RX	54LS374 MJ 883B

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"
Mil-Q-9858A, "Quality Program Requirements"
Mil-I-45208, "Inspection System Requirements"

Monolithic Memories facilities in Sunnyvale were recertified in December, 1982 by the Defense Electronics Supply Center (DESC), to manufacture and qualify Schottky Bipolar PROMS and PAL circuits in accordance with Mil-M-38510 Class B and Class C. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of Mil-M-38510. Monolithic Memories has also demonstrated compliance to the strict requirements of both controlled and captive lines connected with special Military programs.

Process and Quality Control

Monolithic Memories low power schottky TTL process, used in the manufacture of all PROM and PAL circuits, uses techniques such as redundant and composite masking to reduce random defects in the active chip area. This approach results in improved quality, increased reliability and lower overall cost due to higher yields. The quality philosophy at Monolithic Memories emphasizes process controls, as reflected in the use of effective in-process monitors and audits, in addition to gate inspections.

Quality Assurance

The Military Products Division measures/screens all products to the following AQL levels:

TEST	MILITARY
Hermeticity (including fine and gross)	0.4
Electrical	.1
DC at 25° C	.1
Functional at 25° C	.1
AC at 25° C	.1
DC at Temperature Extremes	.1
Functional at Temperature Extremes	.1
AC at Temperature Extremes	.1

The QA organization at Monolithic Memories ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of Mil-Std-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

Product Qualification/Quality Conformance Inspection

The Military Products Division has a quality conformance testing program in accordance with Mil-Std-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that Monolithic Memories' Reliability Department, as a minimum, conduct full qualification testing per Method 5005 of Mil-Std-883. Once qualified, each package type (from each assembly line) and device (by technology group as delineated in Mil-M-38510) are incorporated into Monolithic Memories Quality Conformance Inspection program which utilizes the requirements of Mil-M-38510.

When Military Programs do not require that qualification data be run on the specific lot shipped, Monolithic Memories Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and destruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following generic data is available:

Group B — Package related tests

- Qualification is performed every 6 weeks of manufacture on each shippable package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly integrity

Group C — Product/Process related tests

- Qualification is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- Life test data may be used to qualify similar technologies, as long as it uses the same manufacturing process.
- Purpose: To monitor the reliability of the process and parametric performance for each product technology.
- Monolithic Memories Group C Generic Families:
    1. PROMS — Schottky Nichrome
    2. PROMS — Titanium Tungsten
    3. PAL Circuits
    4. Logic, Multiplier, Fifo
    5. Octal Interface

Group D — In-depth package related tests

- Qualification is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Manufacturing and Screening Locations

JAN Products, Monolithic Memories Modified Level "S", and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified assembly line in Sunnyvale, California.

Mil-Std-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by Monolithic Memories Quality Department, as well as by many of our customers, to manufacture Mil-Std-883 Class B product. Conformance to Mil-Std-883 requirements is routinely monitored through audits at the Penang facility, as well as incoming inspections in Sunnyvale prior to completion of Burn-In and Final Test. Manufacturing capabilities for each Monolithic Memories facility are highlighted on the chart below.

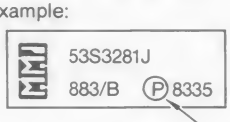
Manufacturing Capabilities

	Sunnyvale	Penang
Assembly	X	X
Precap Inspection	X	X
Environmental Testing	X	X
Electrical PreTest	X	X
Burn-In	X	
Post Burn-In electricals (Group A Requirements)	X	
Mark	X	X
Factory Programming (when applicable)	X	
Qualification and Quality Conformance Testing	X	

A country of origin designator is marked on all military devices prior to shipment. This designator identifies the assembly location of the device, and appears as a single letter code before the date code marking. Designators used are:

S = Sunnyvale, California assembly
P = Penang, Malaysia assembly

Marking Example:



Country of Origin Designator

AC Testing

Although Monolithic Memories offers a large selection of programmable products, it must be pointed out that AC Testing cannot be performed on many of our product types without their being programmed. For those devices which must be programmed prior to AC Tests and are ordered unprogrammed, Monolithic Memories must "guarantee" their AC Performance.

Newer devices in the PROM and PAL families do allow preprogram AC testability.

Since the **guaranteeing** of parameters can be a serious concern for the Military user, we have outlined several approaches to address the AC screening issue.

1. Monolithic Memories can pull a **Sample** from a lot using our own **Standard patterns** (designed to blow in excess of 50 percent of the fuses) and perform AC testing at 25°C, and temperature extremes.
   a) PAL products processed to DESC prints include programmability samples and AC testing at room temperature as a standard.
   b) AC at high- and low-temperature extremes is a cost adder to standard processing.
2. Monolithic Memories can program parts using custom programs submitted by the customer. AC can then be done with the following options:
   a) Sample AC at 25°C
   b) Sample AC at 25°C, -55°C, 125°C
   c) 100% AC at 25°C
   d) 100% AC at 25°C, -55°C and 125°C (not available on PAL products)

Options b through d are cost adders to basic processing.

On PAL products where custom programming is performed and AC testing is required, additional vector generation and fault coverage analysis is required, as well as AC program checkout. Non-recurring engineering charges are applicable to this type of requirement.

To give you an idea of delivery differences for the options discussed above, general lead times are as follows:

- Unprogrammed:
  Cerdip, 4 — 6 weeks
  Flat pack, 8 — 12 weeks
  Leadless, 6 — 12 weeks
  (consult monthly leadtime guide for individual part types)
- Unprogrammed product using our standard pattern to verify AC at room temperature on sample basis (option 1). Add 2 weeks to standard delivery.
- Programmed product using customer programs with sample AC (option 2a and b). Add 6 weeks to standard delivery. Delivery quoted will be after receipt of customer design package.
- 100% AC testing at 25°C — Standard Monolithic Memories pattern or customer pattern, (option c). Contact factory.

Remember, for ProPALs, customer must provide design package including Boolean Equations, "Seed" function test sequence, package stipulation and AC test vectors, when required. Delivery quotes for this type of product begin **after** receipt of this data from the customer.

ElectroStatic Discharge

The Military Products Division will take all necessary precautions to ensure that ESD is not a cause of a zapped or degraded unit being shipped to a customer. Procedures for handling of units to protect against ESD have been implemented for all Monolithic Memories devices in critical areas.

AN ESD Program has been implemented by the Monolithic Memories Quality Assurance Department to continually review improved methods for more effective precautions in handling ESD sensitive semiconductor devices.

Major Program Participation

Monolithic Memories is a supplier of Military components to most major Department of Defense Programs. A partial listing of program participation is provided.

AMRAAM	F - 15	LAMPS	SUBACS
ASPJ	F - 16	LATIRN	TRIDENT
AWACS	F - 18	PATRIOT	UYK - 43
B - 1	HARM	PERSHING	UYK - 44
B - 52	HARPOON	PHALANX	VLS
CRUISE	HAWK	SIDEWINDER	
DIVADS	HELLFIRE	SPARROW	

Military PROM Performance Analysis

(Max. Military Limits—Three State Only)

Size	FMI		AMD		RAYTHEON		HARRIS		NATIONAL		SIGNETICS		T.I.	
	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}
¼K 32 x 8	5331-1 53S081 53S081A	60/125 35/125 25/125	27S19 27S19A —	50/115 35/115 —	— — —	— — —	7603-2 — —	60/130 — —	— 54S288 —	— 45/110 —	82S123 — —	65/85 — —	18S030 — —	50/110 — —
1K 256 x 4	5301-1 53S141	75/130 55/130	— 27S21	— 60/130	— —	— —	7611-2 7611A-2	75/130 65/130	54S287 —	60/130 —	82S129 —	70/125 —	24S10 —	75/100 —
2K 256 x 8	5309-1	80/155	—	—	—	—	—	—	54LS471	70/100	—	—	28L22	75/100
2K 518 x 4	5306-1 53S241	75/130 55/130	27S13 27S13A	60/130 40/130	29611A —	60/130 —	7621-2 7621A-2	85/130 70/130	54S571 54S571A	65/130 60/130	82S131 —	70/140 —	— —	— —
4K 512 x 8	5341-1 5341-2	80/155 70/155	— 27S31	— 70/175	— —	— —	7641-2 7641A-2	85/170 70/170	54S474 —	75/170 —	82S141 —	90/185 —	28S46 —	70/135 —
	5349-1 5349-2	80/155 70/155	— 27S29	— 70/160	29621 29621A	80/155 60/155	7649-2 —	80/170 —	54S472 54S472A	75/170 60/155	82S147 82S147A	75/165 60/165	28S42 —	70/135 —
4K 1K x 4	5353-1 5353-2	75/175 65/140	— 27S33	— 70/145	— —	— —	7643-2 7643A-2	85/140 70/140	54S573 —	75/140 —	82S137 —	80/150 —	24S41 —	75/140 —
	53S441 53S441A	55/140 50/140	— 27S33A	— 45/145	— —	— —	— —	— —	54S573A —	60/140 —	82S137A —	70/150 —	— —	— —
8K 1K x 8	5381-1 5381-2	125/175 70/175	— 27S181	— 80/185	29631 29631A	90/170 60/170	7681-2 —	90/170 —	— 77S181	— 75/170	82S181 82S181A	90/185 80/185	28S86 28S86A	65/170 50/170
8K Reg 1K x 8	53RS881 53RS881A	*25/180 *20/180	27S37 27S37A	30/185 25/185	— —	— —	— —	— —	— —	— —	— —	— —	— —	— —
8K 2K x 4	5389-1 5389-2	100/170 70/170	— —	— —	29651 29651A	90/170 70/170	7685-2 —	90/170 —	— 77S185	— 75/140	82S185 —	115/130 —	24S81 —	85/175 —
	53S841 53S841A	55/150 50/150	27S185 27S185A	55/150 45/150	— —	— —	— —	— —	— —	— —	82S185A —	80/160 —	— —	— —
16K 2K x 8	53S1681 53S1681A	60/185 45/185	27S191 27S191A	65/185 50/185	29681A —	70/180 —	76161-2 —	80/180 —	77S191 —	80/175 —	82S191A —	70/185 —	— —	— —
16K Reg. 2K x 8	53RA1681 53RA1681A	*25/185 *20/185	27S45/47 27S45/47A	30/185 25/185	— —	— —	— —	— —	— —	— —	— —	— —	— —	— —
	53RS1681 53RS1681A	*25/185 *20/185	27S45/47 27S45/47A	30/185 25/185	— —	— —	— —	— —	— —	— —	— —	— —	— —	— —
16K 4K x 4	53S1641 53S1641A	65/175 50/175	27S41 27S41A	65/170 50/170	— —	— —	76165-2 —	80/170 —	— —	— —	— —	— —	— —	— —
16K Diag. 4K x 4	53D1641 53DA1643	*25/190 *25/190	27S85 27S85	30/190 30/190	— —	— —	— —	— —	— —	— —	— —	— —	— —	— —
32K 4K x 8	53S3281 53S321A	60/190 50/190	27S43 27S43A	65/185 55/185	29671A —	80/195 —	76321-2 —	75/190 —	77S321 —	65/190 —	82S321 —	80/185 —	— —	— —

*Clock to output time.

Package Information

Leadless Chip Carrier

Monolithic Memories will be offering our PROM, PLE, PAL/-HAL circuits, HMSI, FIFO, Octal Interface, 54S7XX Memory Support and Arithmetic Element/Logic families in 20 and 28 square, ceramic/metal LCC (Leadless Chip Carriers) packages.

PROMs
- 20 square LCC
  1/4K, 1K, 2K and 4K
- 28 square LCC
  4K, 8K, 16K and 32K

PLE™ (Programmable Logic Elements)
- 20 square LCC
  Derived from 1/4K and 4K PROM
- 28 square LCC
  Derived from 8K and 16K PROM

PAL/HAL Arrays (20 terminal series)
- 20 square LCC

PAL/HAL Arrays (24 terminal series)
- 28 square LCC

HMSI™
- 28 square LCC

FIFO Memories
- 20 square LCC

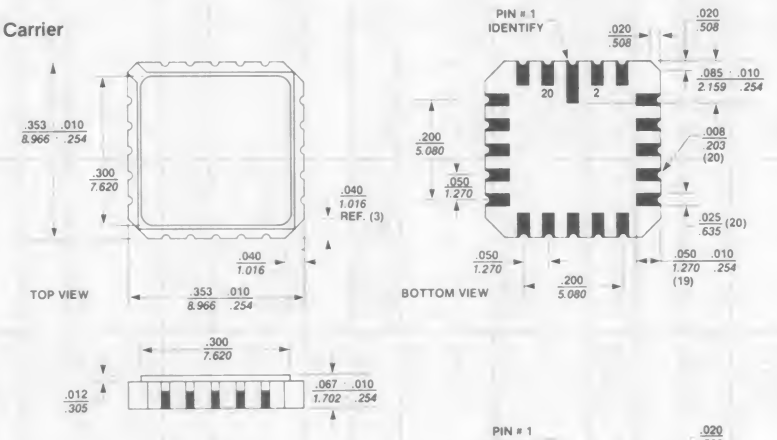
Octal Interface
- 20 square LCC

54S7XX Memory Support
- 20 square LCC

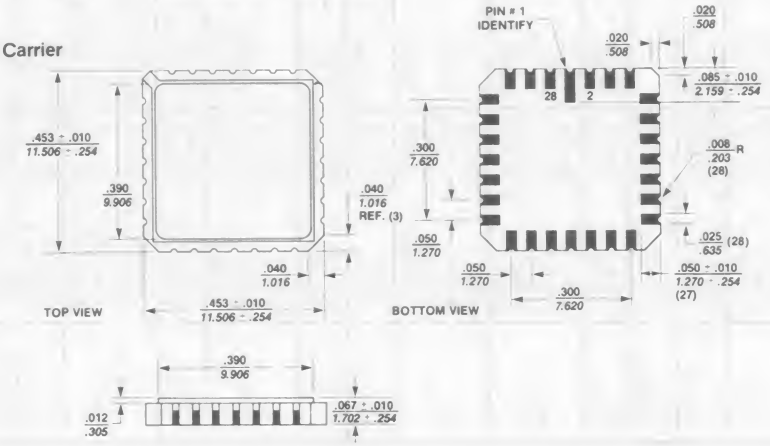
Arithmetic Element/Logic
- 20 square LCC

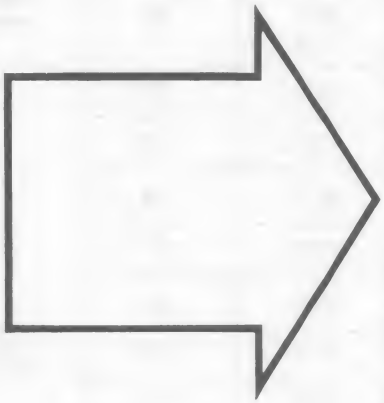
Multipliers
- 44L

L20 Leadless Chip Carrier



L28 Leadless Chip Carrier





PROM Selection Guide

SIZE	PINS	DEVICE NUMBER	OUTPUT	T_{AA}(ns) COM'L/MIL	I_{CC}(mA) COM'L/MIL	COMMENTS
¼K 32 × 8	16	53/6330-1 53/6331-1	OC TS	55/60	125	
		53/63S080 53/63S081 53/63S081A	OC TS TS	25/35 17/25	125	Designed for PLE market
1K 256 × 4	16	53/6300-1 53/6301-1	OC TS	55/75	130	
		53/63S140 53/63S141	OC TS	45/55	130	
2K 512 × 4	16	53/6305-1 53/6306-1	OC TS	60/75	130	
		53/63S240 53/63S241	OC TS	45/55	130	
2K 256 × 8	20	53/6308-1 53/6309-1	OC TS	70/80	155	
	24	6336-2	TS	70/80	155	Contact factory for military versions
4K 1K × 4	18	53/6352-1 53/6353-1	OC TS	60/75	175	For PLE market
		53/6353-2	TS	50/65	140	
		53/63S441 53/63S441A	TS	45/55 35/50		
		53/63RA441	TS	*30/35	190	w/output Registers
4K 512 × 8	24	53/6340-1 53/6341-1	OC TS	70/80	155	
		53/6341-2	TS	55/70	155/175	
	20	53/6348-1 53/6349-1	OC TS	70/80	155	
		53/6349-2	TS	55/70	155/175	
8K 2K × 4	18	53/6388-1 53/6389-1	OC TS	70/100	170	
		53/6389-2	TS	55/70	155/170	
		53/63S841 53/63S841A	TS	50/55 35/50	150	For PLE market
8K 1K × 8	24	53/6380-1 53/6381-1	OC TS	90/125	175	All devices are available in Skinnydip (JS)
		53/6380-2 53/6381-2	OC TS	70/90 55/70	170/175	
		53/63RS881 53/63RS881A	TS	*20/25 *15/20	180	w/output registers
16K 4K × 4	20	53/63S1641 53/63S1641A	TS	50/65 35/50	175	For PLE market
16K 4K × 4	24	53/63D1641 53/63DA1643	TS	20/25	190	Registered PROMs with Diagnostic on Chip (DDC)
16K 2K × 8	24	53/63S1681 53/63S1681A	TS	50/65 35/50	185	
16K 2K × 8	24	53/63RA1681 53/63RA1681A	TS	*20/25 *15/20	185	PROMs with output Registers
	24	53/63RS1681 53/63RS1681A	TS	*20/25 *15/20		
32K 4K × 8	24	53/63S3281 53/63S3281A	TS	50/60 40/50	190	

* Clock to Output time.

Bipolar PROM Cross-Reference Guide

Memory Description													
Organization	Pins	Output	[redacted]	AMD	Fair-child	Fujitsu	Harris	Intel	Motorola	National	Raytheon	Signetics	TI
¼K 32 x 8	16	OC	6330-1 63S080	27S18	—	—	7602	—	—	74S188	—	82S23	18SA030
		TS	6331-1 63S081/A	27S19	—	—	7603	—	—	74S288	—	82S123	18S030
1K 256 x 4	16	OC	6300-1 63S140	27S20	—	—	7610	—	—	74S387	—	82S126	24SA10
		TS	6301-1 63S141	27S21	—	—	7611	—	—	74S287	—	82S129	24S10
2K 256 x 8	20	OC	6308-1	—	—	—	—	—	—	—	—	—	18SA22
		TS	6309-1	—	—	—	—	—	—	74LS471	—	—	18S22
2K 512 x 4	16	OC	6305-1 63S240	27S12	—	—	7620	—	7620	74S570	—	82S130	—
		TS	6306-1 63S241	27S13	—	—	7621	—	7621	74S571	29611	82S131	—
4K 512 x 8	20	OC	6348-1	27S28	—	7123	7648	—	—	74S473	—	—	28SA42
		TS	6349-1, -2	27S29	—	7124	7649	—	—	74S472	29621	82S147	28S42
	24	OC	6340-1	27S30	—	—	7640	—	7640	74S475	—	—	28SA46
		TS	6341-1, -2	27S31	—	—	7641	—	7641	74S474	—	82S141	28S46
4K 1024 x 4	18	OC	6352-1	27S32	—	—	7642	—	7642	74S572	—	—	24SA41
		TS	6353-1, -2 63S441 63S441A	27S33	—	—	7643	—	7643	74S573	—	82S137	24S41
8K 2048 x 4	18	OC	6388-1	27S184	93514	7127	7684	—	7684	87S184	—	82S184	24SA81
		TS	6389-1, -2 63S841 63S841A	27S185	93515	7128	7685	—	7685	87S185	29651	82S185	24S81
8K 1024 x 8	24	OC	6380-1, -2	27S180	93450	7131	7680	—	7680	87S180	—	82S180	28SA86
		TS	6381-1, -2	27S181	93451	7132	7681	3628	7681	87S181	29631	82S181	28S86
8K Reg 1024 x 8	24	TS	63RS881 63RS881A	27S37	—	—	—	—	—	87SR181	—	—	—
					—	—	—	—	—	—	—	—	—
16K 2048 x 8	24	TS	63S1681 63S1681A	27S191	93Z511	7138	76161	3636	76161	87S191	29681	82S191	28S166
16K Reg 2048 x 8	24	TS	63RA1681/A 63RS1681/A	27S47	—	—	—	—	—	—	—	—	—
					—	—	—	—	—	—	—	—	—
16K 4096 x 4	20	TS	63S1641 63S1641A	27S41	93513	7134	76165	—	—	—	—	—	—
16K Diag. 4096 x 4	24	TS	63D1641	27S85	—	—	—	—	—	—	—	—	—
		2S	63DA1643	27S85	—	—	—	—	—	—	—	—	—
32K 4096 x 8	24	TS	63S3281 63S3281A	27S43	—	7142	76321	3632	—	87S321	29671	82S321	—

NOTE: Only Commercial Specification part numbers are listed.

Commercial PROM Performance Analysis

(Max. Commercial Limits—Three State Only)

Size	FMI		AMD		FUJITSU		HARRIS		NATIONAL		SIGNETICS		T.I.	
	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}	Part No.	T_{AA}/I_{CC}
¼K 32 x 8	6331-1 63S081 63S081A	55/125 25/125 17/125	27S19 27S19A –	40/115 25/115 –	– – –	– – –	7603-5 – –	50/130 – –	– 74S288 –	– 35/110 –	82S123 – –	50/77 – –	18S030 – –	40/110 – –
1K 256 x 4	6301-1 63S141	55/130 45/130	– 27S21	– 45/130	– –	– –	7611-5 7611A-5	60/130 40/130	74S287 –	50/130 –	82S129 –	50/120 –	24S10 –	55/120 –
2K 256 x 8	6309-1	70/155	–	–	–	–	–	–	74LS471	60/100	–	–	28L22	70/100
2K 512 x 4	6306-1 63S241	60/130 45/130	27S13 27S13A	50/130 30/130	– –	– –	7621-5 7621A-5	70/130 40/130	74S571 74S571A	55/130 45/130	82S131 –	50/140 –	– –	– –
4K 512 x 8	6341-1 6341-2	70/155 55/155	– 27S31	– 55/175	– –	– –	7641-5 7641A-5	70/170 50/170	74S474 74S474A	65/170 45/170	82S141 –	60/175 –	28S46 –	60/135 –
	6349-1 6349-2	70/155 55/155	– 27S29	– 55/160	– 7124E	– 45/170	7649-5 7649A-5	60/170 45/170	74S472 74S472A	60/170 45/155	82S147 82S147A	60/155 45/155	28S42 –	60/135 –
4K 1K x 4	6353-1 6353-2	60/175 50/140	– 27S33	– 55/140	– –	– –	7643-5 7643A-5	60/140 50/140	74S573 –	60/140 –	82S137 –	60/140 –	24S41 –	60/100 –
	63S441 63S441A	45/140 35/140	– 27S33A	– 35/140	– –	– –	– –	– –	74S573A 74S573B	45/140 35/140	82S137A 82S137B	45/140 35/140	– –	– –
8K 1K x 8	6381-1 6381-2	90/175 55/170	– 27S181	– 60/185	– 7132E	– 55/175	7681-5 7681A-5	70/170 50/170	– 87S181	– 60/170	82S181 82S181A	70/175 55/175	– 28S86A	– 60/165
8K Reg. 1K x 8	63RS881 63RS881A	*20/180 *15/180	27S37 27S37A	25/175 20/175	– –	– –	– –	– –	87SR181 –	20/175 –	– –	– –	– –	– –
8K 2K x 4	6389-1 6389-2	70/170 55/155	– –	– –	– –	– –	7685-5 –	70/170 –	– 87S185	– 55/170	82S185 –	100/120 –	24S81 24S81-55	70/175 55/175
	63S841 63S841A	50/150 35/150	27S185 27S185A	50/150 35/150	– –	– –	7685A5 –	45/170 –	– –	– –	82S185A 82S185B	50/155 45/155	– –	– –
16K 2K x 8	63S1681 63S1681A	50/185 35/185	27S191 27S191A	50/185 35/185	7138H 7138Y	45/180 35/180	76161-5 –	60/180 –	87S191 –	65/175 –	82S191A –	55/175 –	28S166-55 –	55/130 –
16K Reg. 2K x 8	63RA1681 63RA1681A	*20/185 *15/185	27S45/47 27S45/47A	25/185 20/185	–	–	–	–	–	–	–	–	–	–
	63RS1681 63RS1681A	*20/185 *15/185	27S45/47 27S45/47A	25/185 20/185	–	–	–	–	–	–	–	–	–	–
16K 4K x 4	63S1641 63S1641A	50/175 35/175	27S41 27S41A	50/170 35/170	– –	– –	76165-5 –	60/170 –	– –	– –	– –	– –	– –	– –
16K Diag. 4K x 4	63D1641 63DA1643	*20/190 *20/190	27S85 27S85	25/190 25/190	– –	– –	– –	– –	– –	– –	– –	– –	– –	– –
32K 4K x 8	63S3281 63S3281A	50/190 40/190	27S43 27S43A	55/185 40/185	7142M –	55/185 –	76321-5 –	65/190 –	87S321 –	55/185 –	82S321 –	70/175 –	– –	– –

*Clock to Output Time

High Performance Ti-W PROM Family

53/63SXXX 53/63SXXXA

Features/Benefit

- From 256 Bit to 32768 Bit of memory
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage programming
- Highest speed Schottky PROM family available
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current
- Compatible pin configurations for upward expansion

Applications

- Microprogram control store
- microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The family features common electrical parameters and programming algorithm, low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. the 53 series is specified for the military ranges.

New Programming Technique:

Our new HIGH Performance PROMs use an elevated voltage at V_{CC} instead of using a separate programming pin (one of the enables) as in the Standard Performance PROMs using nichrome fuses. Changes in the internal circuitry were made to optimize speed and accordingly the unblown fuse represents a LOW at the output. When a fuse is programmed it reflects a high at the output.

Unblown Fuse

Blown Fuse

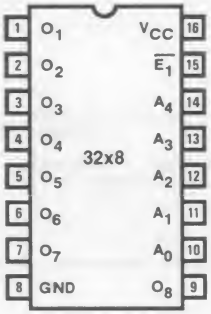
High Performance PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to + 75°C	- 55°C to + 125°C
¼K	32 x 8	OC TS	16, (20)	N,J,F,W (L)	63S080 63S081	53S080 53 S081
1K	256 x 4	OC TS	16, (20)	N,J,F,W (L)	63S140 63S141	53S140 53S141
2K	512 x 4	OC TS	16, (20)	N,J,F,W (L)	63S240 63S241	53S240 53S241
4K	1024 x 4	TS	18, (20)	N,J,F, (L)	63S441 63S441A	53S441 53S441A
8K	2048 x 4	TS	18, (20)	N,J,F, (L)	63S841 63S841A	53S841 53S841A
16K	4096 x 4	TS	20	N, J, F	63S1641 63S1641A	53S1641 53S1641A
	2048 x 8	TS	24, (28)	J,JS,F, (L)	63S1681 63S1681A	53S1681 53S1681A
32K	4096 x 8	TS	24, (28)	*J (L)	63S3281 63S3281A	53S3281 53S3281A

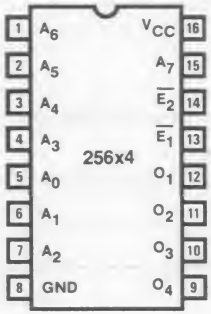
* Flat-pack contact the factory ( ) = Military Product

Pin Configurations

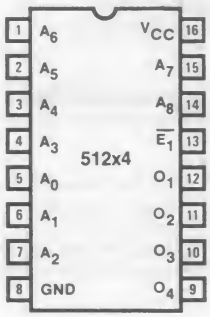
53/63S080
53/63S081



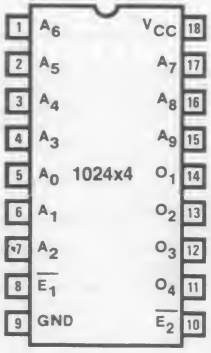
53/63S140
53/63S141



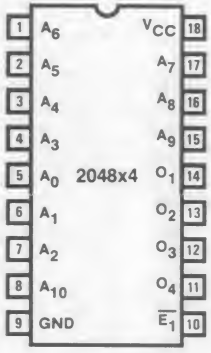
53/63S240
53/63S241



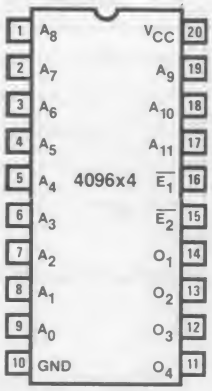
53/63S441
53/63S441A



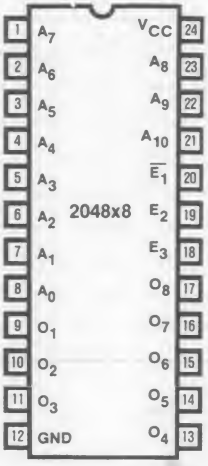
53/63S841
53/63S841A



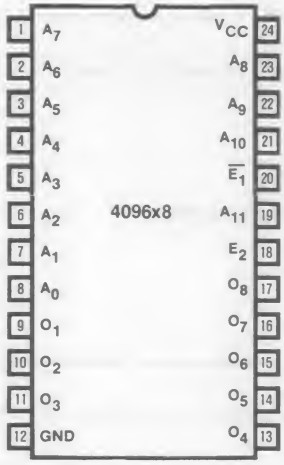
53/63S1641
53/63S1641A



53/63S1681
53/63S1681A



53/63S3281
53/63S3281A



3

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5V to 7V
Input voltage ..... -1.5V to 7V
Off-state output voltage ..... -0.5V to 5.5V
Storage temperature range ..... -65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM except S1681, S3281			0.45	
				COM S1681, S3281			0.5	
V_{OH}	High-level output voltage*	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = -2mA		2.4			V
			COM I_{OH} = -3.2mA					
I_{OZL}	Off-state output current*	V_{CC} = MAX	V_O = 0.4V				-40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				40	μA
			V_O = 5.5V				100	
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded. All outputs open.	S080, S081			90	125	mA
			S140, S141			80	130	
			S240, S241			90	130	
			S441, S441A			95	140	
			S841, S841A			110	150	
			S1641, S1641A			130	175	
			S1681, S1681A			135	185	
			S3281, S3281A			150	190	

* Three-state only.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics

Over Commercial Operating Conditions

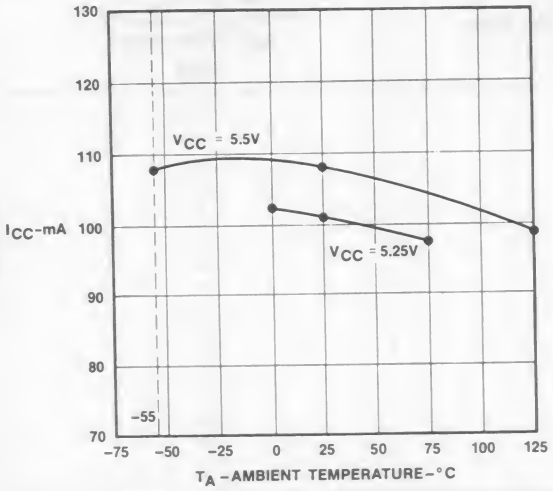
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME MAX
63S080, 63S081	25	20
63S140, 63S141	45	25
63S240, 63S241	45	25
63S441	45	25
63S441A	35	25
63S841	50	25
63S841A	35	25
63S1641	50	25
63S1641A	35	25
63S1681	50	30
63S1681A	35	25
63S3281	50	30
63S3281A	40	30

Over Military Operating Conditions

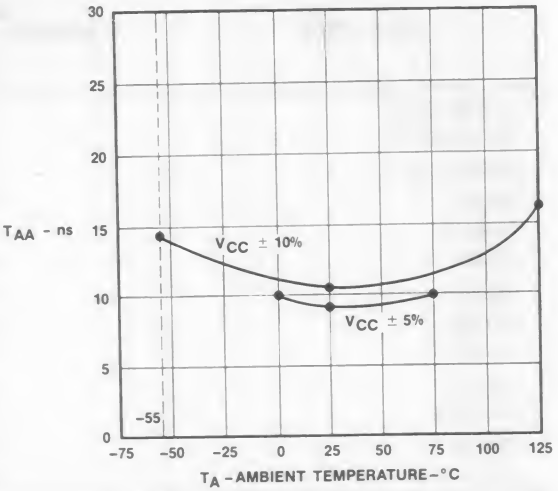
*DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME MAX
53S080, 53S081	35	30
53S140, 53S141	55	30
53S240, 53S241	55	30
53S441	55	30
53S441A	50	30
53S841	55	30
53S841A	50	30
53S1641	65	30
53S1641A	50	30
53S1681	60	35
53S1681A	50	30
53S3281	60	35
53S3281A	50	35

63S081
53S081

Typical I_{CC} vs Temperature

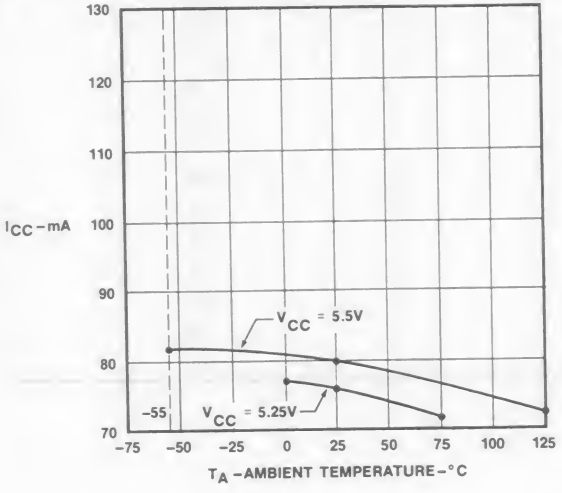


Typical T_{AA} vs Temperature

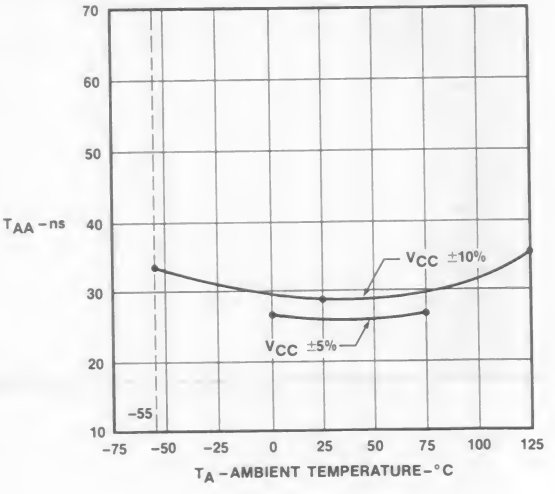


63S141
53S141

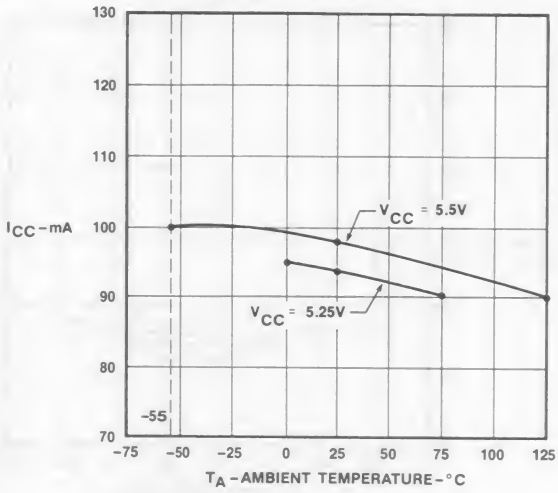
Typical I_{CC} vs Temperature



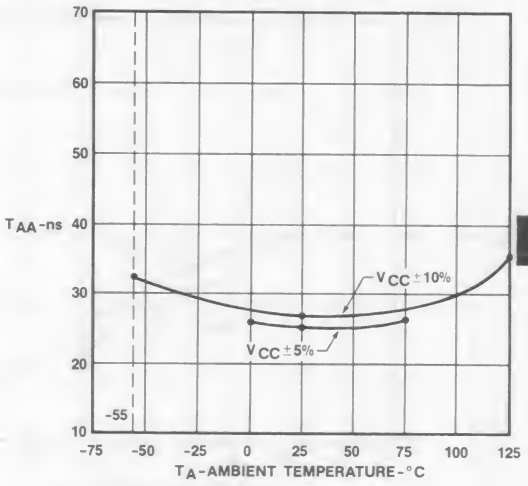
Typical T_{AA} vs Temperature



Typical I_{CC} vs Temperature



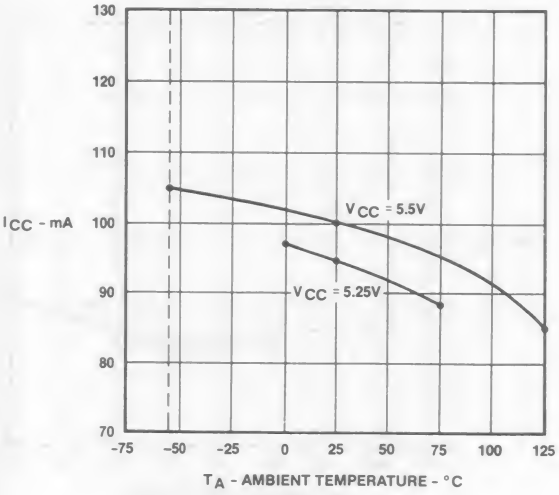
Typical T_{AA} vs Temperature



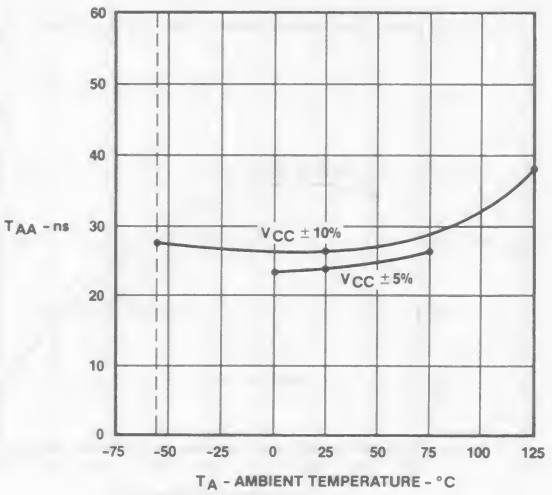
3

53/63S441
53/63S441A

Typical I_{CC} vs Temperature

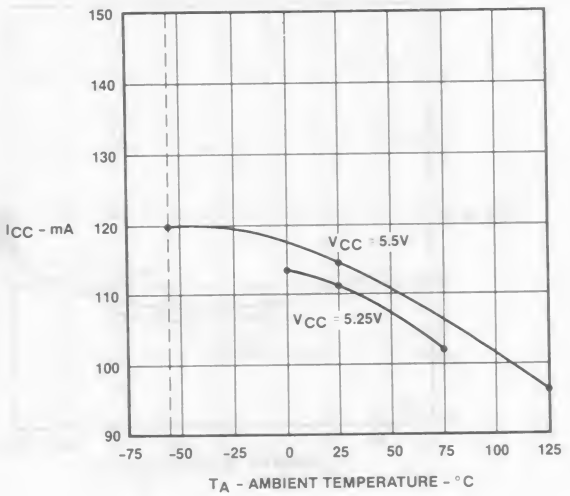


Typical T_{AA} vs Temperature

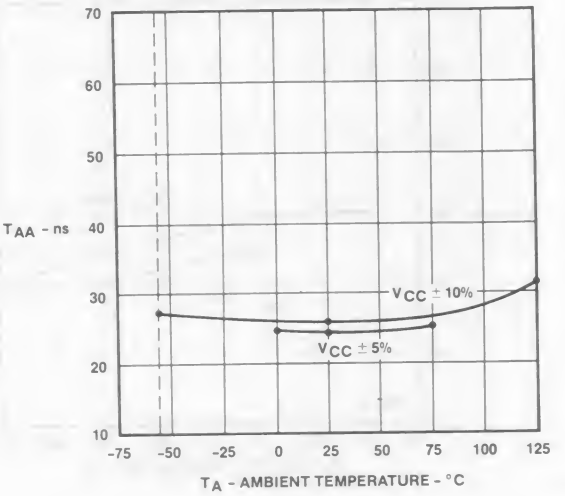


53/63S841
53/63S841A

Typical I_{CC} vs Temperature

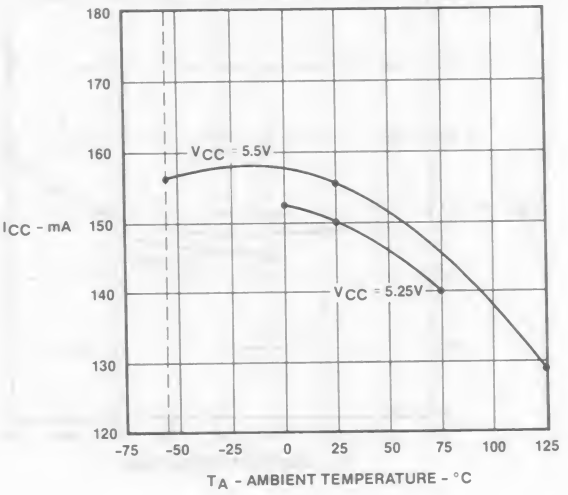


Typical T_{AA} vs Temperature

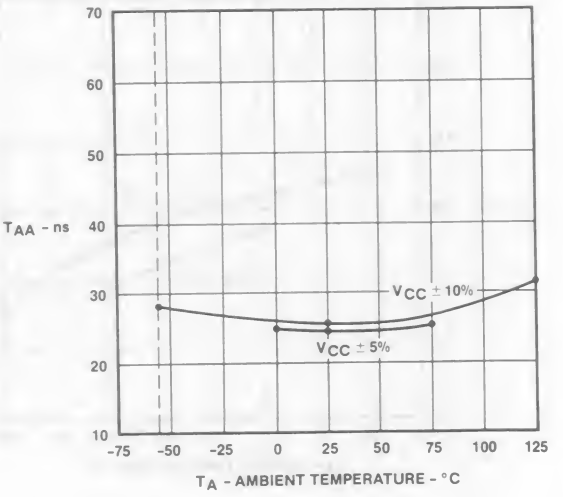


53/63S1641
53/63S1641A

Typical I_{CC} vs Temperature

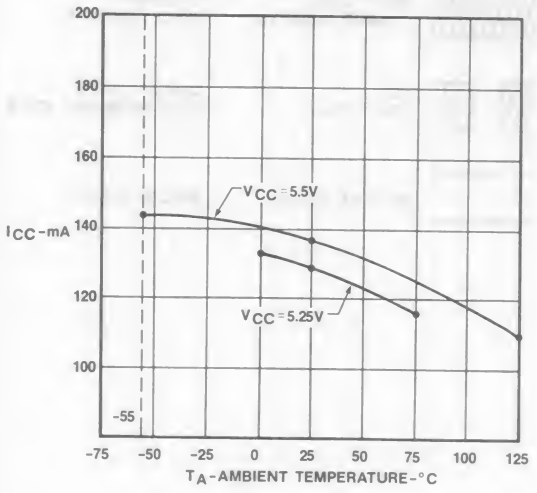


Typical T_{AA} vs Temperature

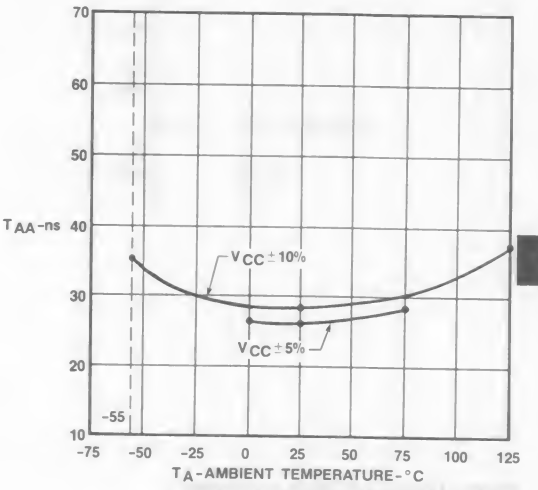


53/63S1681
53/63S1681A

Typical I_{CC} vs Temperature



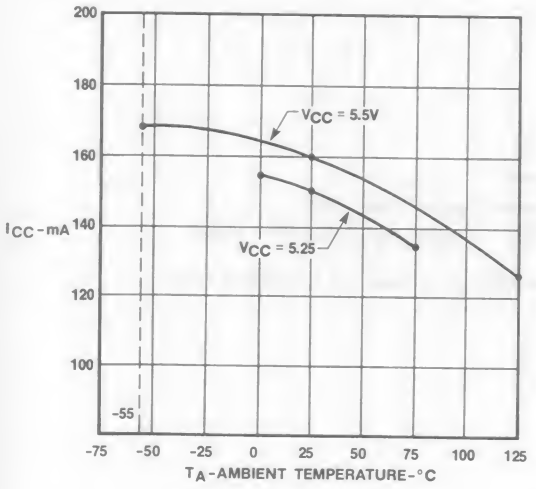
Typical T_{AA} vs Temperature



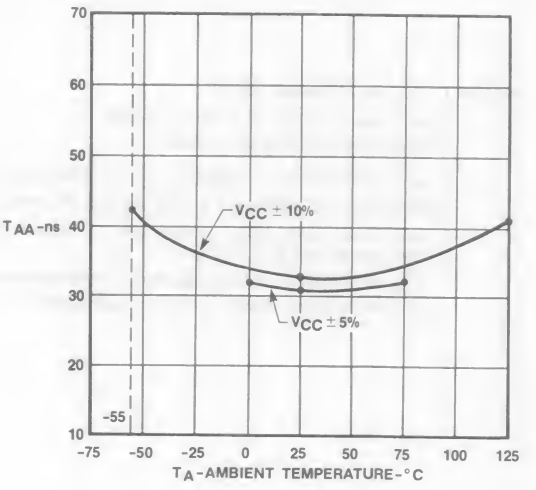
3

53/63S3281
53/63S3281A

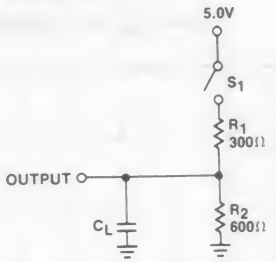
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



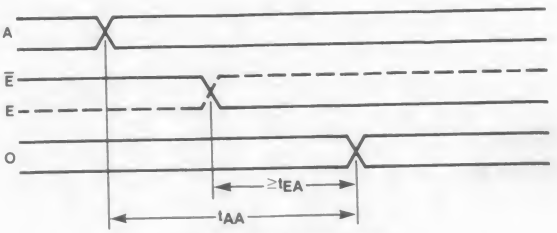
Switching Test Load



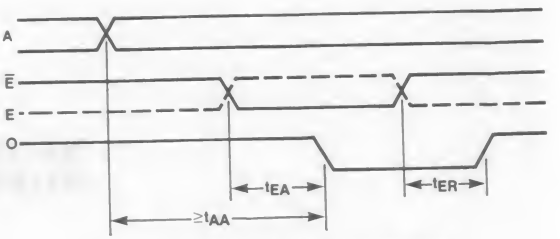
Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

NOTES:
1. Input pulse amplitude 0V to 3.0V.
2. Input rise and fall times 2-5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_l = 30pF and measured at 1.5V output level.
5. For open collector devices. TEA and TER are measured at the 1.5V output level with S_1 closed and C_L = 30pF.
6. For three-state devices, TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   TER is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Ultra Fast 32x8 Ti-W PROM

53S081A 63S081A

Features/Benefits

- 17 ns maximum access time
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current

Applications

- Programmable logic element (PLE™)
- Address decoder
- Priority encoder
- Random logic replacement

Description

The 53/63S081A features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

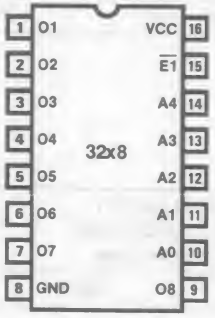
The 53/63S081A is programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Selection Guide

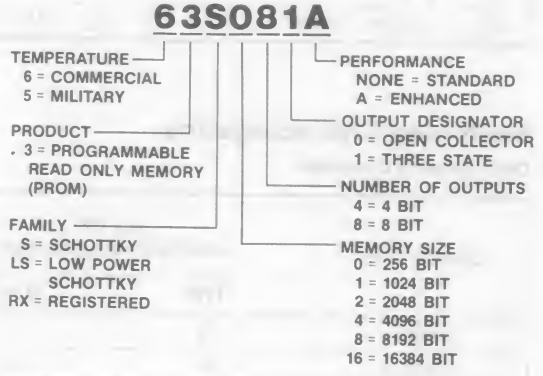
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	-55°C to +125°C
1/4K	32x8	T.S.	16	N, J, F, W	63S081A	53S081A

Pin Configuration

53/63S081A



Part Numbering System



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Monolithic Memories MMI

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... -65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA				-1.5	V
V_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				-0.25	mA
V_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = -2mA		2.4			V
			COM I_{OH} = -3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V				-40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded. All outputs open.			90	125	mA

Switching Characteristics

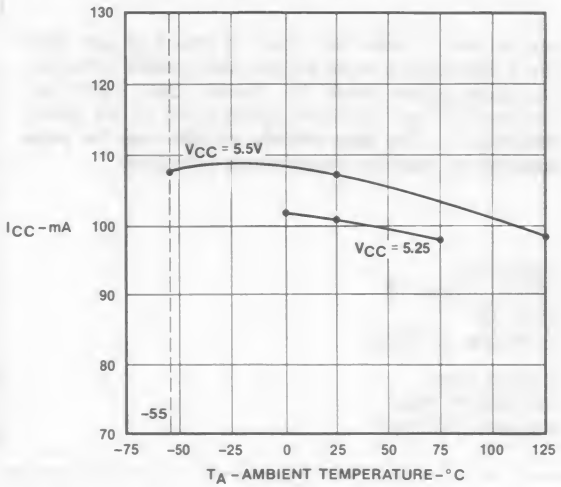
Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME MAX	UNIT
63S081A	9	17	9	17	ns
53S081A	9	25	9	20	

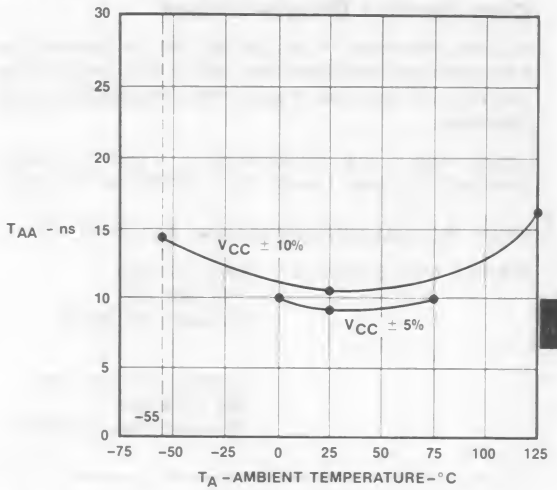
† Typical at 5.0V V_{CC} and 25°C TA.

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Typical I_{CC} vs Temperature

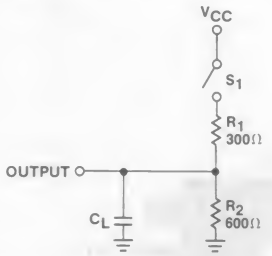


Typical T_{AA} vs Temperature



3

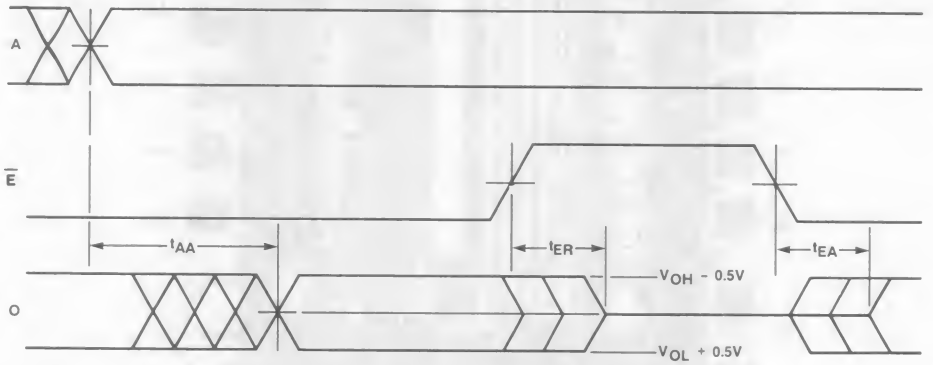
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.
5. TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test. TER is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} –0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Commercial Programmers

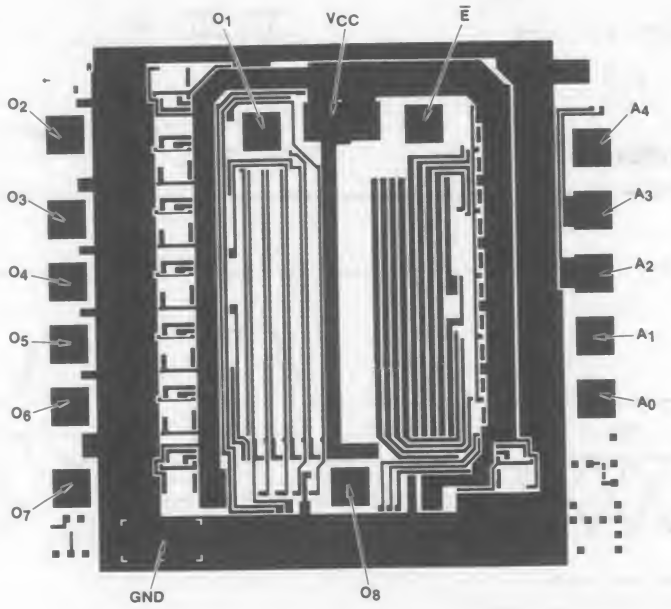
Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device. **Remember — The best PROMs available can be made unreliable by improper programming techniques.**

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION		
	Date I/O Corp. P.O. Box 308 Issaquah, WA 98027	Digelec Inc. 7335 E. Acoma DR Suite 103 Scottsdale, AZ 85260
	Kontron Electronic, Inc. 630 Price Ave. Redwood City, CA 94036	Pro-Log Corp. 2411 Garden Road Monterey, CA 93940

Metal Mask Layout



High Performance Registered 1024x4 PROM
53/63RA441

Features/Benefits

- Edge triggered "D" registers
- Advanced Schottky processing
- 4-bit-wide in 18 pin for high board density
- Lower system package counts
- Lower system power
- Faster cycle times
- 16mA I_{OL} output drive capability

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register which holds the micro-instruction during execution, is now incorporated into the PROM chip.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION	PINS	TYPE	MIL	COM
4K	1024x4	18	J, N	53RA441	63RA441

3

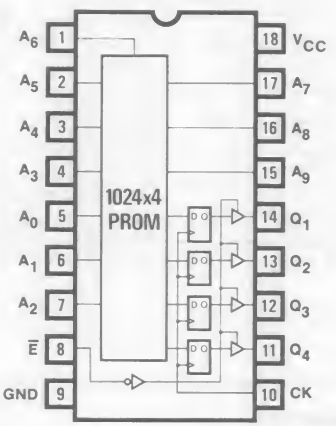
Edge Triggered Register

The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard.

Pin Configuration

53/63RA441



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Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
t_{su}	Address set-up time	60	30		50	30		
t_h	Address hold time	0	–10		0	–10		
t_w	Clock pulse width	25	8		20	8		
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA		2.4			V
			COM I_{OH} = –3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V				–40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded	MIL		120	175	mA
			All outputs open	COM		120	165	

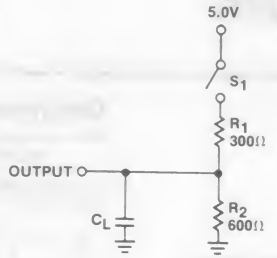
*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†Typicals at 5.0V V_{CC} and 25°C T_A

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Clock to output access time		20	35		20	30	ns
t_{ER}/t_{EA}	Enable to output access and recovery time		19	35		19	30	ns

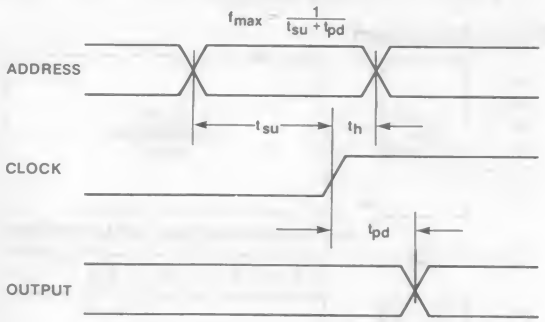
Standard Test Load

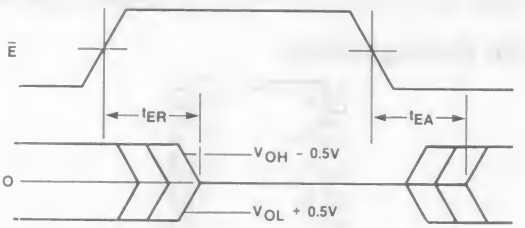


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms





ENABLE ACCESS TIME AND RECOVERY TIME

NOTES:
1. Input pulse amplitude 0V to 3.0V.
2. Input rise and fall times 2-5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed; C_L = 30pF and measured at 1.5V output level.
5. TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
6. TER is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

High Performance 1024x8 Registered PROM

53/63RS881
53/63RS881A

Features/Benefits

- Edge triggered "D" registers
- Synchronous and Asynchronous enables
- Versatile 1:16 initialization words
- 8-bit-wide in 24 pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti-W)

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

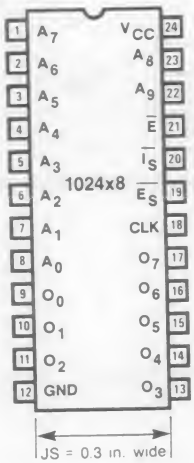
The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{E_S}$) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a high or if $\overline{E_S}$ is high when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{I_S}$) pin low, one of the 16 column words (A_3-A_0) will be set in the output registers independent of the row addresses (A_9-A_4). The unprogrammed state of $\overline{I_S}$ words are low, presenting a CLEAR with $\overline{I_S}$ pin low. With all $\overline{I_S}$ column words (A_3-A_0) programmed to the same pattern, the $\overline{I_S}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I_S}$ words programmed high a PRESET function is performed.

Pin Configuration

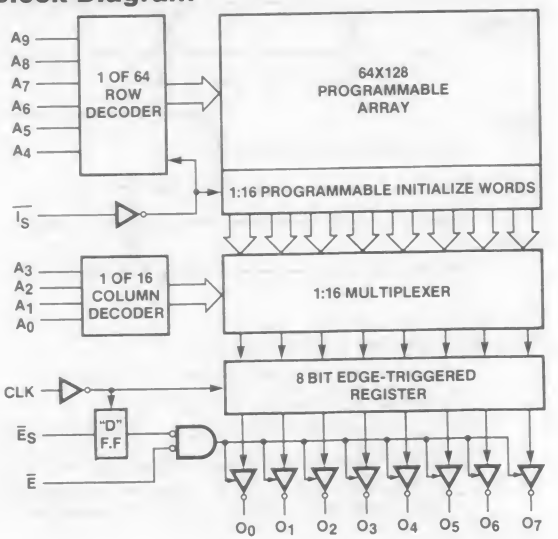


Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
8K	Standard	24	JS, F	53RS881	63RS881
	Enhanced	28	L	53RS881A	63RS881A

* Flat-pack — contact the factory

Block Diagram



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Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 to 7V	12V
Input voltage	-1.5 to 7V	7V
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP	MILITARY				COMMERCIAL				UNIT
			53RS881A		53RS881		63RS881A		63RS881		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	25	40		45		30		35		ns
$t_{s(\overline{E_S})}$	Setup time from $\overline{E_S}$ to clock	8	15		15		15		15		ns
$t_{s(\overline{I_S})}$	Setup time from $\overline{I_S}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	-5	0		0		0		0		ns
$t_{h(\overline{E_S})}$	Hold time ($\overline{E_S}$)	-3	5		5		5		5		ns
$t_{h(\overline{I_S})}$	Hold time ($\overline{I_S}$)	-5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

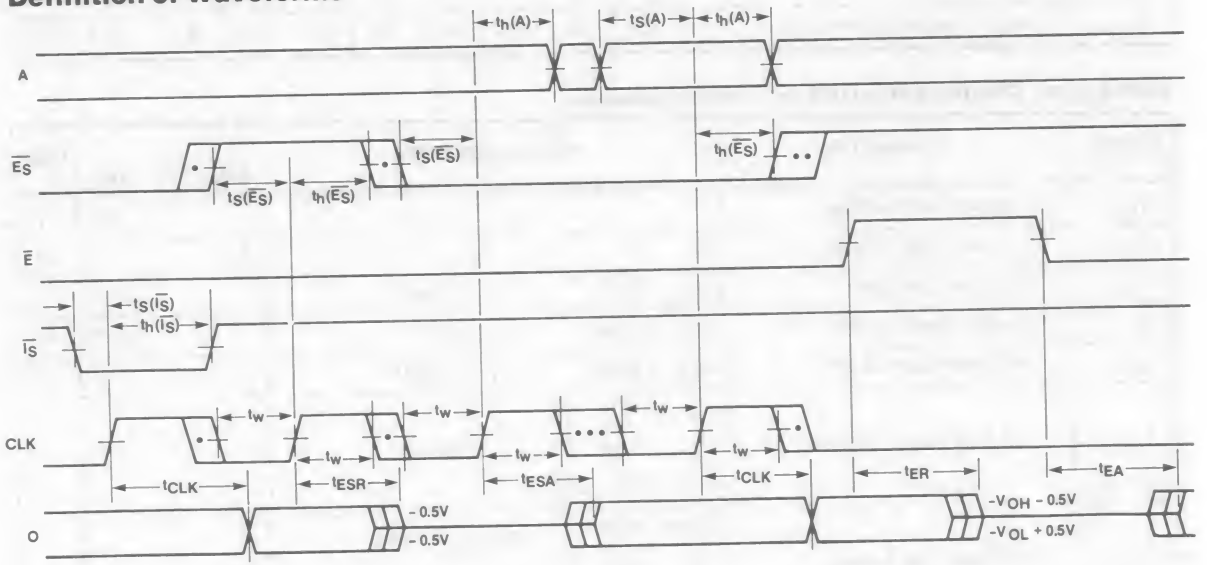
SYMBOL	PARAMETER	TEST CONDITIONS		t			UNIT
				MIN	TYP	MAX	
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA COM I_{OH} = -3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			-40	μA
I_{OZH}			V_O = 2.4V			40	
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs TTL; all outputs open.		130	180	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at 5.0V, V_{CC} and 25°C TA.

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP	MILITARY				COMMERCIAL				UNIT
			53RS881A		53RS881		63RS881A		63RS881		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{E_S}$)	18		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{E_S}$)	17		30		35		25		30	ns
t_{EA}	Enable to output access time ($\overline{E}$)	18		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	17		30		35		25		30	ns

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

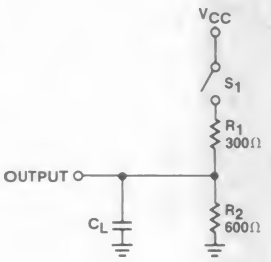
3. Input access measured at the 1.5V level.

4. t_{AA} is tested with switch S_1 closed. C_L = 30pF and measured at 1.5V output level.

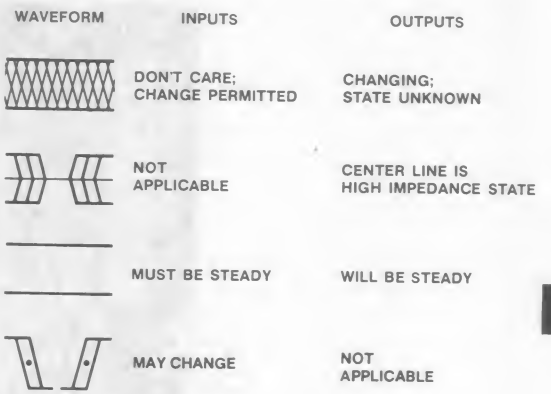
5. t_{EA} and t_{ESA} are measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{ER} and t_{ESA} are measured C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.

Switching Test Load

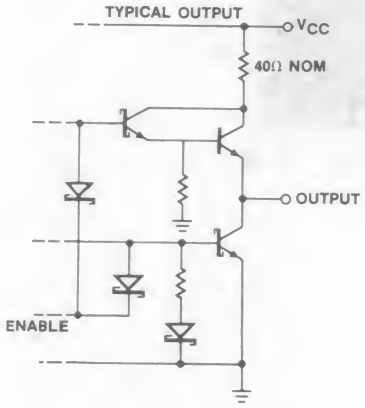


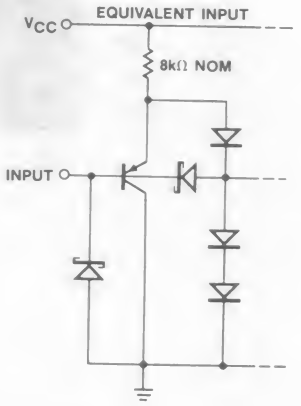
Definition of Timing Diagram



3

Schematic of Inputs and Outputs





Commercial Programmers

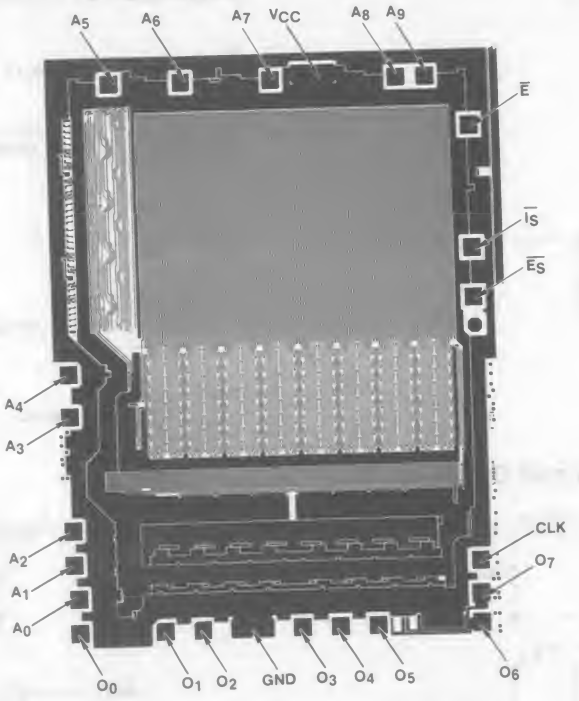
Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-L Unipack2 Rev-V04	Family Code 18	Pinout Code 86

Metal Mask Layout



2048x8 Registered Prom with Asynchronous Enable

53/63RA1681
53/63RA1681A

Features/Benefits

- Asynchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24 pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti-W)

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS1681 and 53/63RS1681A are 2 K x 8 PROMs with on chip "D" type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
16K	Standard	24	JS	53RA1681	63RA1681
	Enhanced		(28)(L)	53RA1681A	63RA1681A

Flat-pack — contact the factory ( ) = Military Product

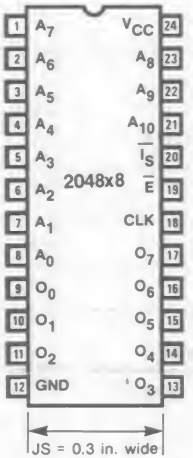
3

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.

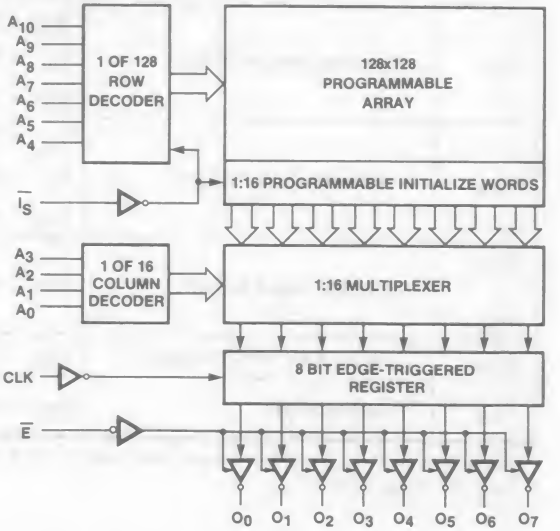
Memory expansion and data control is made flexible with asynchronous enable input. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a HIGH.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{I_S}$) pin LOW, one of the 16 column words (A_3-A_0) will be set in the output registers independent of the row addresses (A_{10}-A_4). With all $\overline{I_S}$ column words (A_3-A_0) programmed to the same pattern, the $\overline{I_S}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I_S}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{I_S}$ words are LOW, presenting a CLEAR with $\overline{I_S}$ pin LOW.

Pin Configuration



Block Diagram



SKINNYDIP® is a registered trademark of Monolithic Memories

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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 to 7V	12V
Input voltage	−1.5 to 7V	7V
Off-state output voltage	−0.5V to 5.5V	12V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{IS})}$	Hold time ($\overline{IS}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA COM I_{OH} = −3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−40	μA
I_{OZH}			V_O = 2.4V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs TTL; all outputs open.		140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25° C T_A.

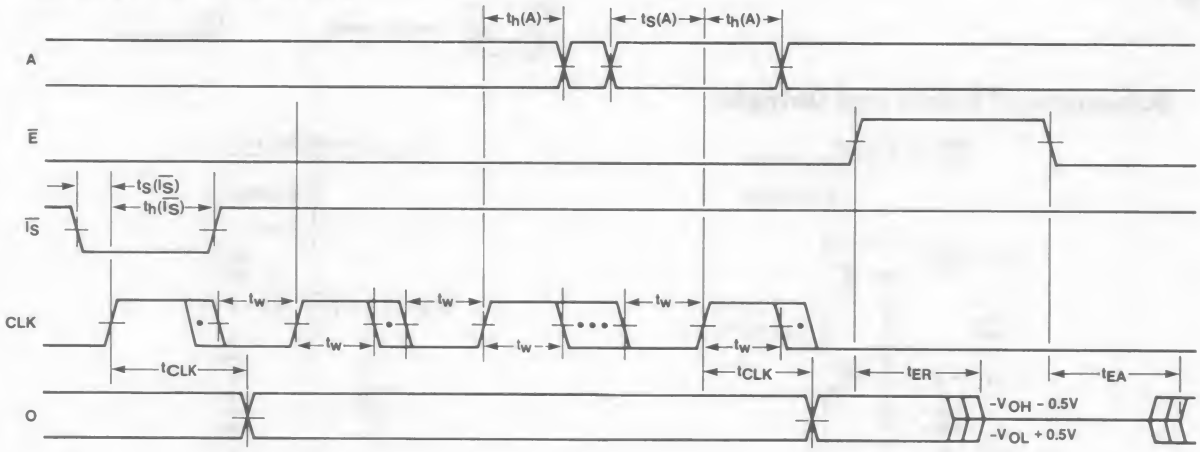
Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{EA}	Enable to output access time ($\overline{E}$)	15		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	15		30		35		25		30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

3

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

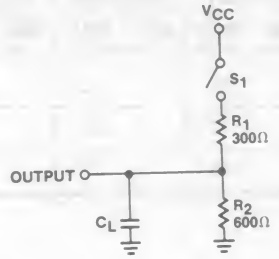
3. Input access measured at the 1.5V level.

4. Switch S_1 is closed, C_L = 30pF and outputs measured at 1.5V level for all tests except t_{EA} and t_{ER}.

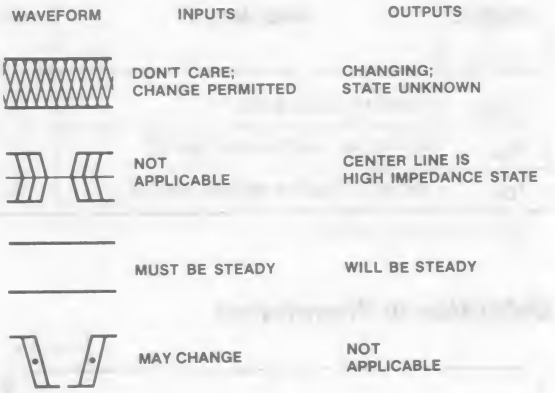
5. t_{EA} is measured at the 1.5V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{ER} is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.

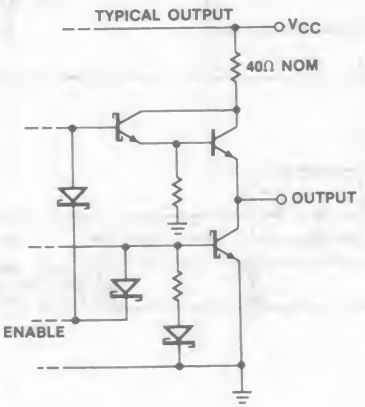
Switching Test Load

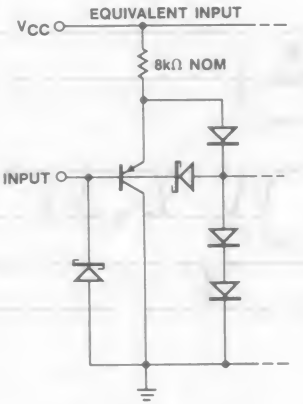


Definition of Timing Diagram



Schematic of Inputs and Outputs





Commercial Programmers

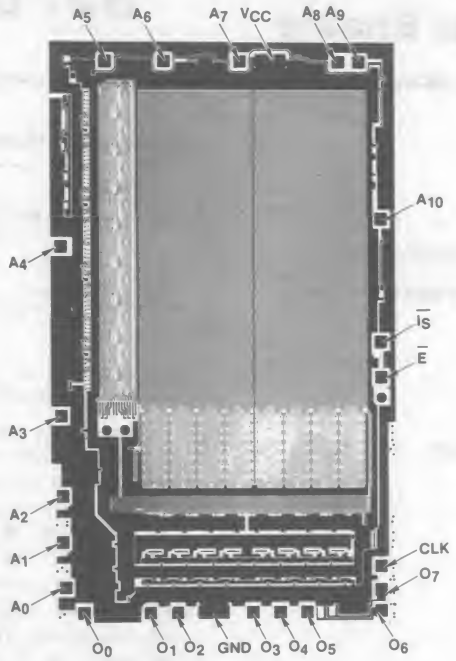
Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-006 Unipack2 Rev-V05	Family Code 18	Pinout Code A3

Metal Mask Layout



2048x8 Registered Prom with Synchronous Enable

53/63RS1681 53/63RS1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24 pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti-W)

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS1681 and 53/63RS1681A are 2 K x 8 PROMs with on chip "D" type registers, versatile output enable control through synchronous enable input and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous ($\overline{E_S}$) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with the synchronous enable input. Outputs may be set to the high impedance state by setting $\overline{E_S}$ HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

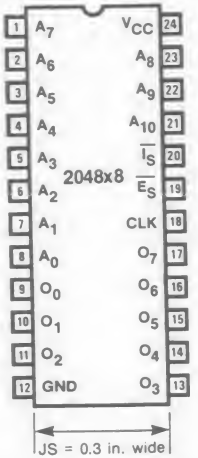
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{I_S}$) pin LOW, one of the 16 column words (A_3-A_0) will be set in the output registers independent of the row addresses (A_{10}-A_4). With all $\overline{I_S}$ column words (A_3-A_0) programmed to the same pattern, the $\overline{I_S}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I_S}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{I_S}$ words are LOW, presenting a CLEAR with $\overline{I_S}$ pin LOW.

Ordering Information

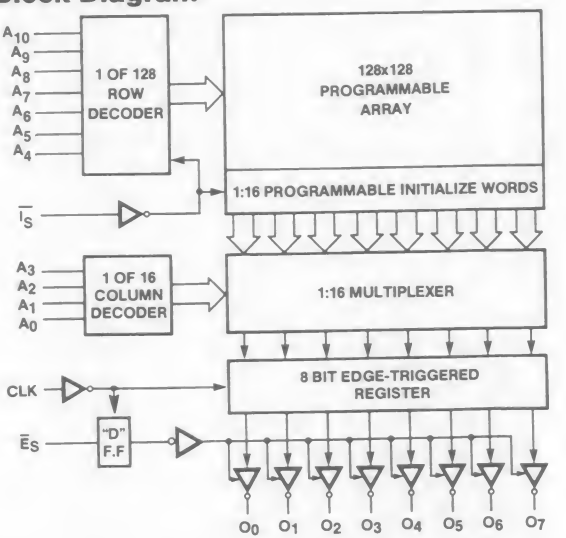
MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
16K	Standard	24	JS	53RS1681	63RS1681
	Enhanced		(28)(L)	53RS1681A	63RS1681A

Flat-pack — contact the factory ( ) = Military Product

Pin Configuration



Block Diagram



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Monolithic Memories MMI

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 to 7V	12V
Input voltage	−1.5 to 7V	7V
Off-state output voltage	−0.5V to 5.5V	12V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{E_S})}$	Setup time from $\overline{E_S}$ to clock	7	15		15		15		15		ns
$t_{s(\overline{I_S})}$	Setup time from $\overline{I_S}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{E_S})}$	Hold time ($\overline{E_S}$)	−3	5		5		5		5		ns
$t_{h(\overline{I_S})}$	Hold time ($\overline{I_S}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA COM I_{OH} = −3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−40	μA
I_{OZH}			V_O = 2.4V			40	
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs TTL; all outputs open.		140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

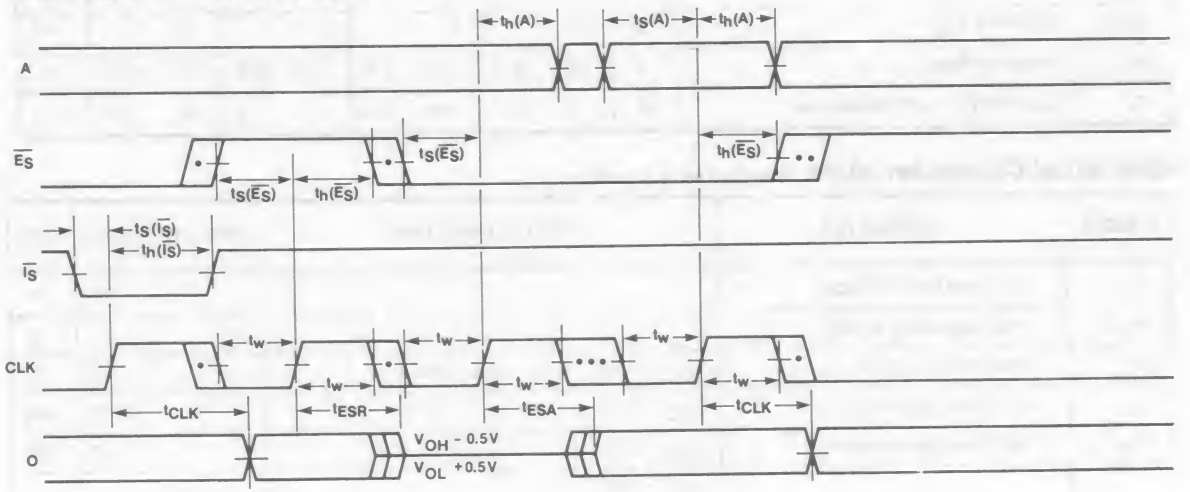
† Typical at 5.0 V V_{CC} and 25°C T_A

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{E_S}$)	15		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{E_S}$)	15		30		35		25		30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

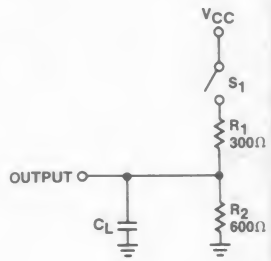
3. Input access measured at the 1.5V level.

4. Switch S_1 is closed, C_L = 30pF and outputs measured at 1.5V level for all tests except t_{ESA} and t_{ESR}.

5. t_{ESA} is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   t_{ESR} is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5V output level.

Switching Test Load

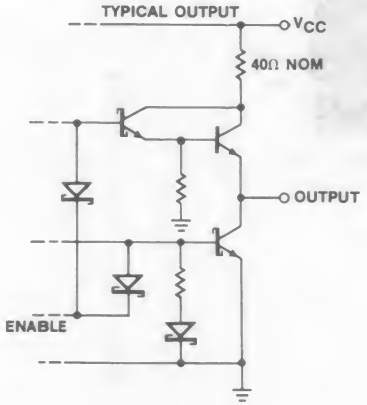


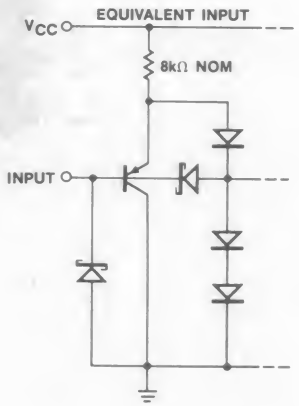
Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

3

Schematic of Inputs and Outputs





Commercial Programmers

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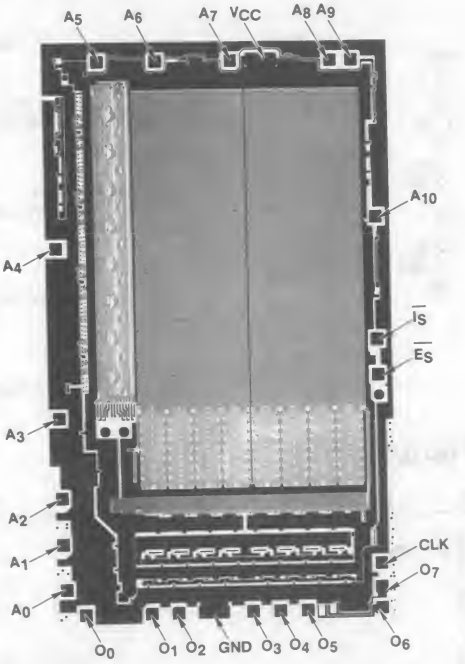
Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-006 Unipack2 Rev-V05	Family Code 18	Pinout Code A3

Metal Mask Layout



4096x4 Diagnostic Registered PROM with Asynchronous Enable

53D1641
63D1641

Patent Pend.

Features/Benefits

- Asynchronous output enable
- Provides system diagnostic testing for system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Casadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- 24 mA output drive capability
- Replaces embedded diagnostic code

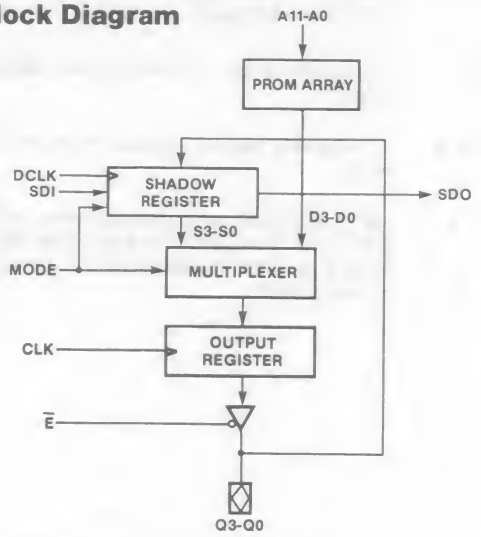
Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63D1641 is a 4Kx4 PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

Block Diagram



SKINNYDIP® is a registered trademark of Monolithic Memories.

Ordering Information

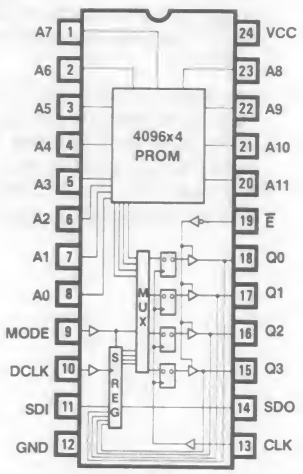
MEMORY		TEMP.	PACKAGE		PART NO.
SIZE	ORG.		PINS	TYPE	
16K	4096x4	MIL	24	JS	53D1641
		COM		(28) (L)	63D1641

Flat-pack — contact the factory ( ) = Military Product

3

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

Logic Symbol



2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q_3-Q_0	S_3-S_0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S_3	Load output register from PROM array
L	X	*	↑	HOLD	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	$Q_n \leftarrow S_n$	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	$S_n \leftarrow Q_n$	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The clock pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q_3-Q_0 — Q_n represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.

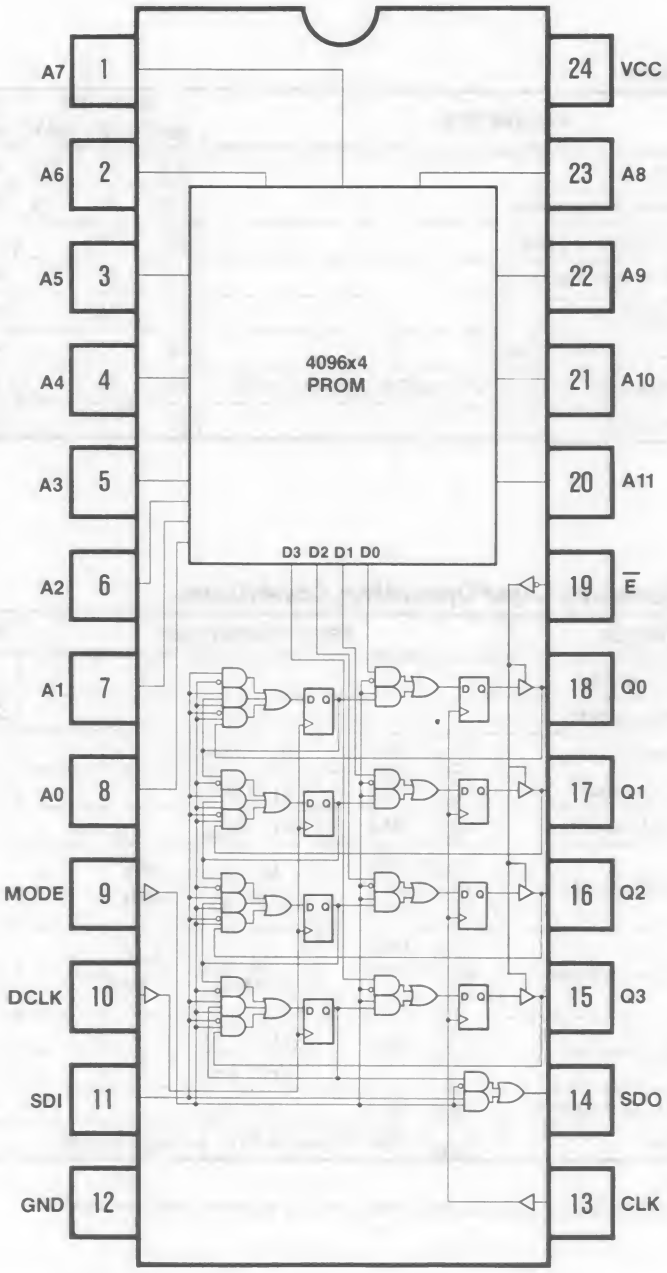
S_3-S_0 — S_n represents the internal shadow register outputs.

A_{11}-A_0 — A_n represents the address inputs to the PROM array.

$\overline{E}$ — The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high impedance state.

Logic Diagram

4096x4 Diagnostic PROM with Asynchronous Enable



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5V to 7V	12V
Input voltage	-1.5V to 7V	7V
Input current	-30mA to +5mA	
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	uA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 16mA COM I_{OL} = 24mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA COM I_{OH} = -3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			-100	uA
I_{OZH}			V_O = 2.4V			40	uA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs TTL; All outputs open			140	190	mA

† Typical at 5.0V V_{CC} and 25°C T_A.

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

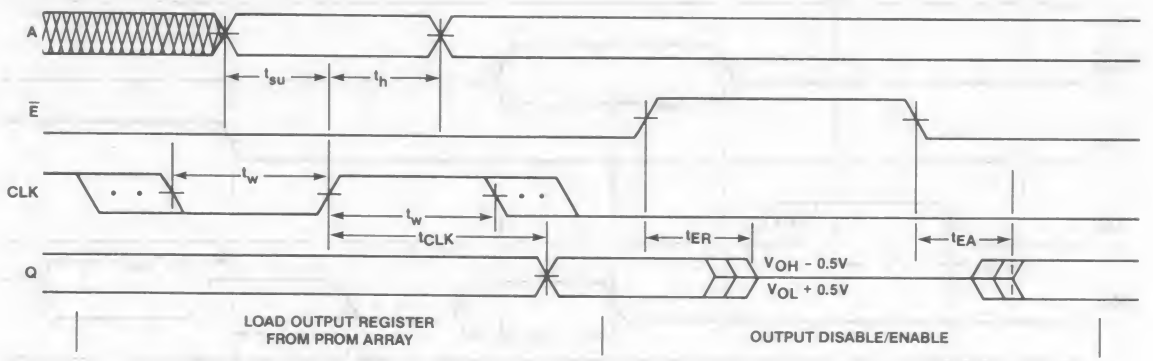
Switching Characteristics Over Operating Conditions and Using Standard Test Load

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{ER}	Disable time		16	30		16	25	ns
t_{EA}	Enable time		16	30		16	25	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

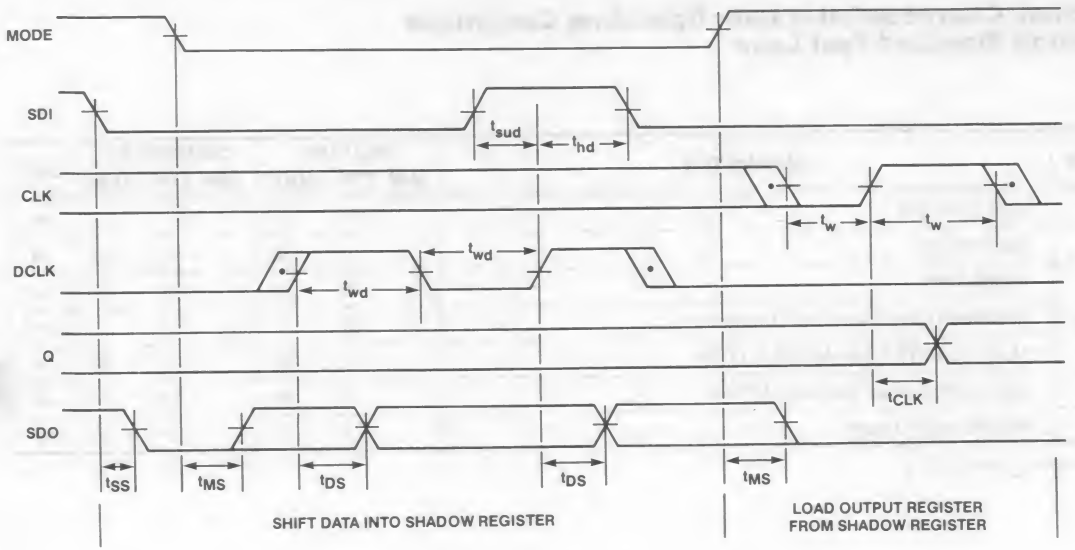
† Typical at 5.0V V_{CC} and 25° C T_A.

3

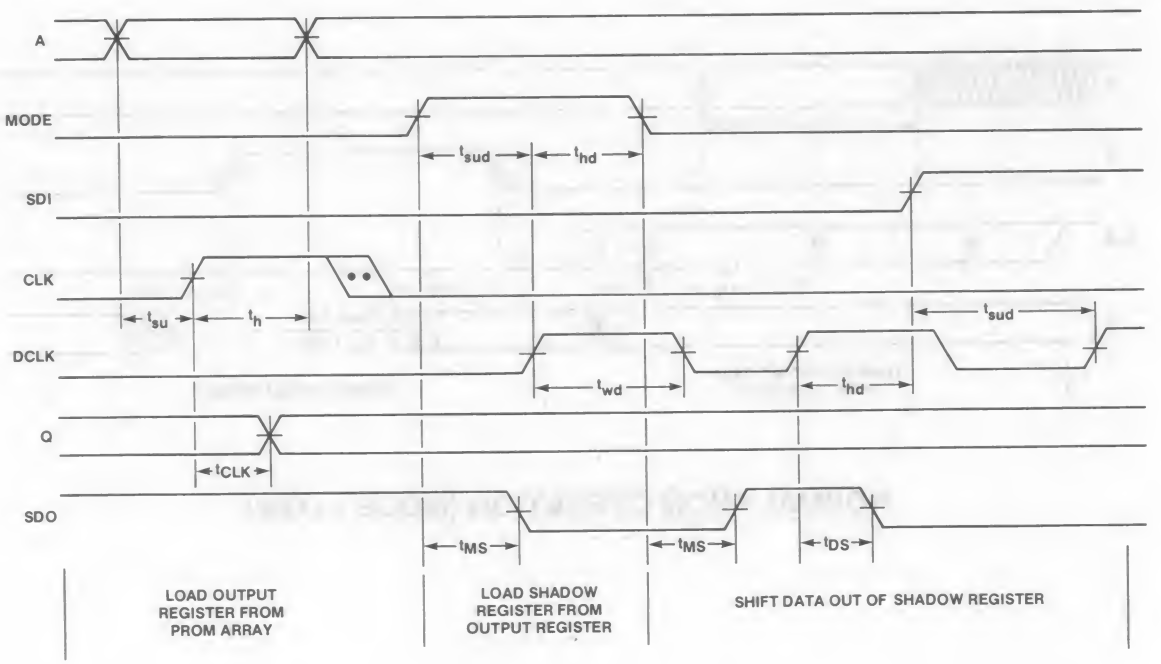
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)

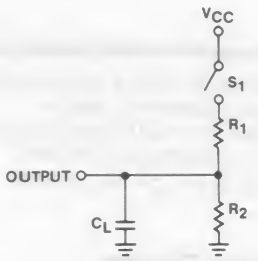


SYSTEM CONTROL



SYSTEM OBSERVATION

Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

3

NOTES: 1. For commercial operating range $R_1 = 200\Omega$, $R_2 = 390\Omega$.
For military operating range $R_1 = 300\Omega$, $R_2 = 600\Omega$.

2. Input pulse amplitude 0V to 3.0V.

3. Input rise and fall times 2-5ns from 1.0V to 2.0V.

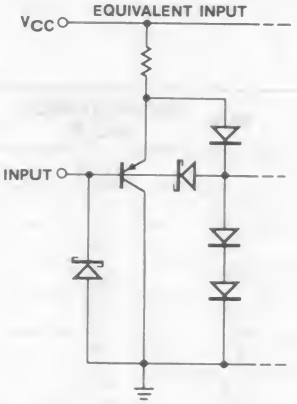
4. Input access measured at the 1.5V level.

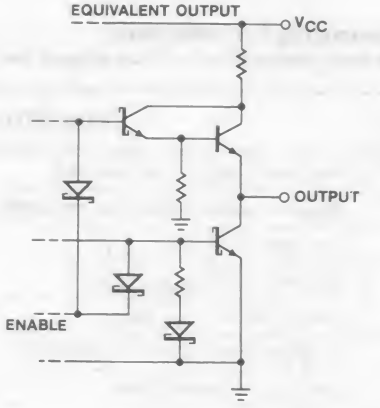
5. Data delay is tested with switch S_1 closed. $C_L = 30_pF$ and measured at 1.5V output level.

6. t_{EA} is measured at the 1.5V output level with $C_L = 30pF$. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

t_{ER} is measured $C_L = 5pF$. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.

Schematic of Inputs and Outputs





53/63D1641
Programming Instructions

Device Description

All of the High Performance Generic Ti-W PROM Families are manufactured with all outputs LOW in all storage locations. To produce a HIGH at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PROM only one output at a time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5KΩ resistors.

Unless specified, Inputs should be at V_{IL}.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100ns or greater must be allowed between steps. The enabling pulse must not occur less than 100ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

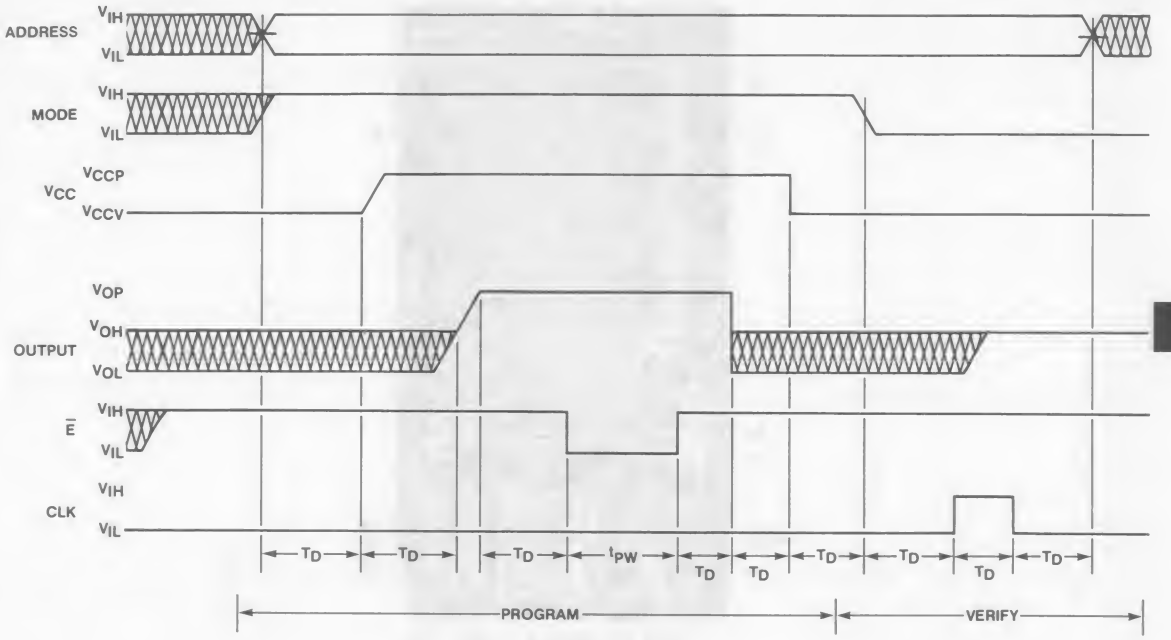
Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. Following verification, apply five additional programming pulses to the bit being programmed.

Programming Parameters

Do not test these parameters or you may program the device.

SYMBOL	PARAMETER	MIN	RECOMMENDED VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	11.5	11.75	12.0	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μs
I_{CCP}	Current limit of V_{CCP} supply	800	1200		mA
I_{OP}	Current limit of V_{OP} supply	15	20		mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μs
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}		25	25	%
t_D	Delay time between programming steps	100	120		ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

Programming Waveforms



Commercial Programmers

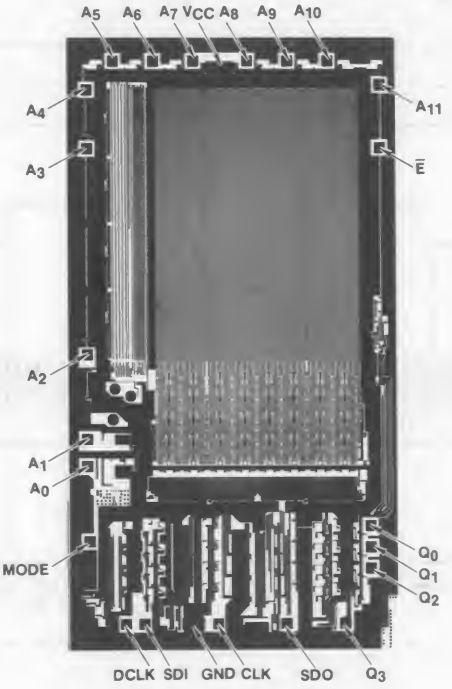
Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-5/M Unipack2 Rev-V04	Family Code B2	Pinout Code 80

Metal Mask Layout



Ti-W PROM Family Programming Instructions

Device Description

All of the High Performance Generic Ti-W PROM Families are manufactured with all outputs low in all storage locations. To produce a high at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PROM only one output at time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5K Ω resistors.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

3

Programming Timing

In order to insure the proper sequence, a delay of 100ns or greater must be allowed between steps. The enabling pulse must not occur less than 100ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Programming Parameters

Do not test these parameters or you may program the device.

SYMBOL	PARAMETER	MIN	RECOMMENDED VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	11.5	11.75	12.0	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μs
I_{CCP}	Current limit of V_{CCP} supply	800	1200	—	mA
I_{OP}	Current limit of V_{OP} supply	15	20	—	mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μs
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}	—	25	25	%
t_D	Delay time between programming steps	100	120	—	ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. Following verification, apply five additional programming pulses to the bit being programmed.

Board Level Programming

Board level programming is easily accomplished since only an enabled PROM is programmed. At the board level only the desired PROM and output should be enabled.

Programming Registered PROMs

The registered PROMs are programmed in the same manner as standard devices with the addition of a clock pulse during verification.

Programming Waveforms

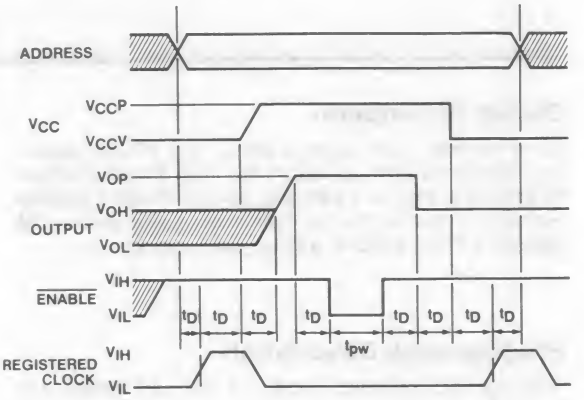


Figure 1.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated. (See Figure 1).

Programming is final manufacturing—it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
P.O. Box 308
Issaquah, WA 98027

Kontron Electronic, Inc.
630 Price Ave.
Redwood City, CA 94036

Di Galec Inc.
7335 E. Acoma DR
Suite 103
Scottsdale, AZ 85260

Pro-Log Corp.
2411 Garden Road
Monterey, CA 93940

Generic
NiCR PROM Family
53/63XXX-1 53/63XXX-2

Features/ Benefit

- From 256 Bit to 8192 Bit memory
- 4-bit-wide and 8-bit-wide for byte oriented applications
- -1 series for standard performance
- -2 series for enhanced performanced
- Reliability proven nichrome fusible links (qualified for MIL-M-38510)
- PNP inputs for low input current
- Compatible pin configurations for upward expansion

Application

- Microprogram store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63XX series generic PROM family offers a wide selection of size and organizations. The 4-bit wide PROMs range from 256x4 to 2048x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit wide PROMs range from 32x8 to 1024x8 in a wide selection of package size including the space saving SKINNYDIP™ 24-pin .300 inch wide package. ALL PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

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Generic PROM Selection Guide

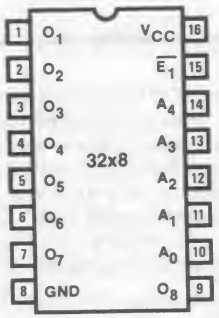
MEMORY			PACKAGE		DEVICE TYPE		OUTPUT
SIZE	ORGANIZATION		PINS	TYPE	COMMERCIAL	MILITARY	WIDTH
1K	256x4	OC TS	16	N, J, F, W	6300-1 6301-1	5300-1 5301-1	
2K	512x4	OC TS	16	N, J, F, W	6305-1 6306-1	5305-1 5306-1	4-bit-wide
4K	1024x4	OC TS	18	N, J	6352-1 6353-1, -2	5352-1 5353-1, -2	
8K	2048x4	OC TS	18	J	6388-1 6389-1, -2	5388-1 5389-1, -2	
¼K	32x8	OC TS	16	N, J, F, W	6330-1 6331-1	5330-1 5331-1	
2K	256x8	OC TS	20	N, J, F	6308-1 6309-1	5308-1 5309-1	
		TS	24	J	6336-2		8-bit-wide
4K	512x8	OC TS	24 (28)	N,JS*,F(L)	6340-1 6341-1, -2	5340-1 5341-1, -2	
		OC TS	20	N, J	6348-1 6349-1, -2	5348-1 5349-1, -2	
8K	1024x8	OC TS	24	N,J,JS*,F	6380-1, -2 6381-1, -2	5380-1, -2 5381-1, -2	

* JS is the .300 inch wide SKINNYDIP™ package.

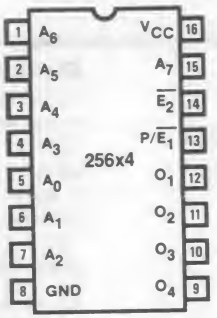
2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Pin Configurations

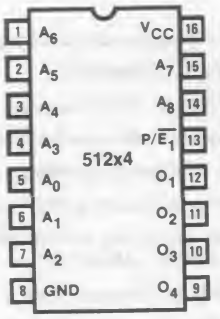
53/6330-1
53/6331-1



53/6300-1
53/6301-1



53/6305-1
53/6306-1



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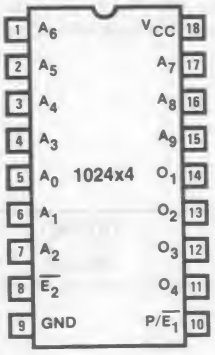

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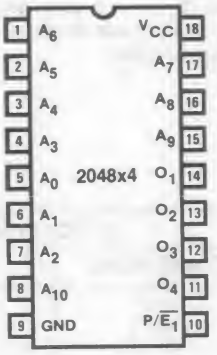

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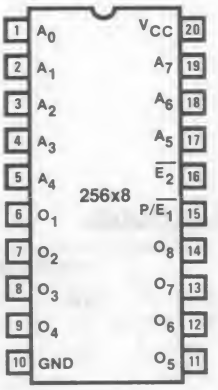

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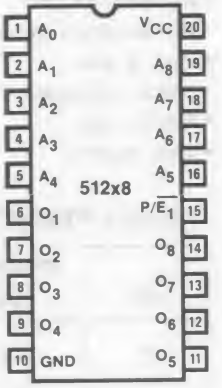
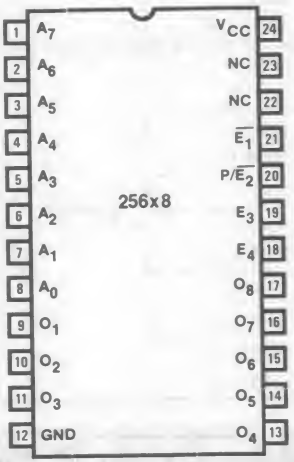


6336-2



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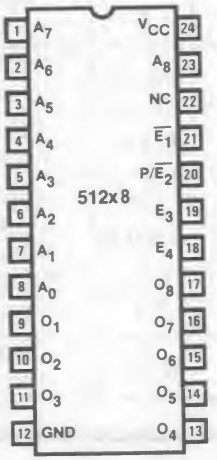

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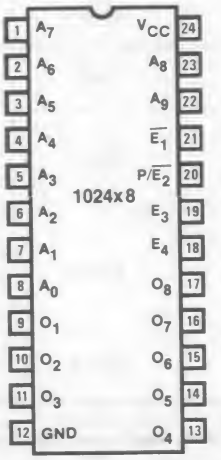
53/6381-1, -2



Absolute Maximum Ratings

Supply voltage V_{CC} ..... −0.5V to 7V
Input voltage ..... −1.5V to 7V
Off-state output voltage ..... −0.5V to 5.5V
Storage temperature range ..... −65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

3

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			-1 SERIES MIN	-1 SERIES MAX	-2 SERIES MIN	-2 SERIES MAX	UNIT
V_{IL}	Low-level input voltage					0.8		0.8	V
V_{IH}	High-level input voltage				2		2		V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5		−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			−0.25		−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other pins)			40		40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA			0.5		0.5	V
			COM I_{OL} = 16mA						
V_{OH}	High-level output voltage *	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA		2.4		2.4		V
			COM I_{OH} = −3.2mA						
I_{OZL}	Off-state output current *	V_{CC} = MAX	V_O = 0.5V			−100		−40	μA
I_{OZH}			V_O = 2.4V			100		40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			100		40	μA
			V_O = 5.5V					100	
I_{OS}	Output short-circuit current*†	V_{CC} = 5V	V_O = 0V		−20	−90	−20	−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open	'30. '31.			125			mA
			'00. '01.			130			
			'05. '06.			130			
			'08. '09. '36.			155		155	
			'40, '41, '48, '49	MIL		155		175	
				COM		155		155	
			'52, '53			175		140	
			'88, '89	MIL		170		170	
				COM		170		155	
			80, 81	MIL		175		175	
				COM		175		170	

* Thre-state only.
† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics

Over Commercial Operating Conditions

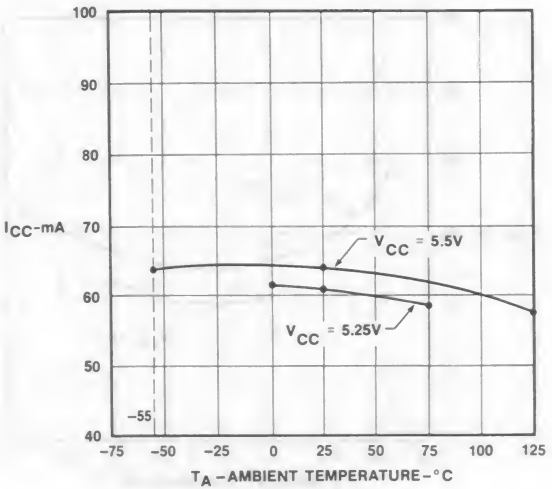
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1 (Ω)	R2 (Ω)
6300-1, 6301-1	55	30		
6305-1, 6306-1	60	30		
6308-1, 6309-1	70	30		
6330-1, 6331-1	50	30		
6336-2	70	30		
6340-1, 6341-1	70	30		
6341-2	55	30		
6348-1, 6349-1	70	30		
6349-2	55	30	300	600
6352-1, 6353-1	60	30		
6353-2	50	30		
6388-1, 6389-1	70	30		
6389-2	55	30		
6380-1, 6381-1	90	40		
6380-2	70	30		
6381-2	55	30		

Over Military Operating Conditions

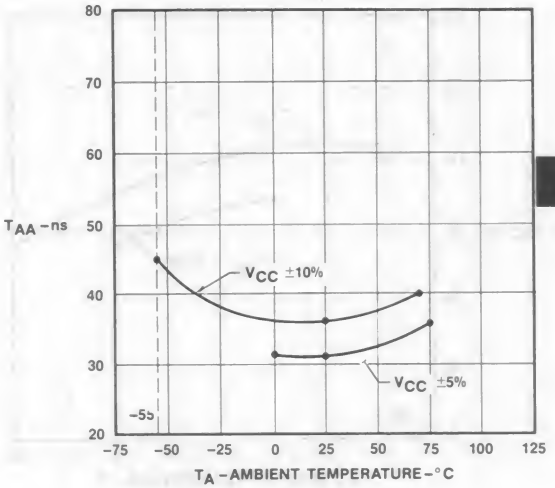
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1 (Ω)	R2 (Ω)
5300-1, 5301-1	75	40		
5305-1, 5306-1	75	40		
5308-1, 5309-1	80	40		
5330-1, 5331-1	60	40		
5336-2	80	40		
5340-1, 5341-1	80	40		
5341-2	70	40		
5348-1, 5349-1	80	40		
5349-2	70	40	375	750
5352-1, 5353-1	75	40		
5353-2	65	30		
5388-1, 5389-1	100	40		
5389-2	70	40		
5380-1, 5381-1	125	40		
5380-2	90	40		
5381-2	70	40		

53/6331

Typical I_{CC} vs Temperature

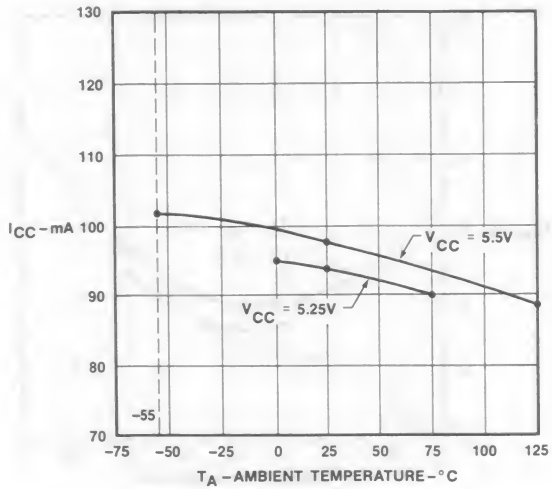


Typical T_{AA} vs Temperature

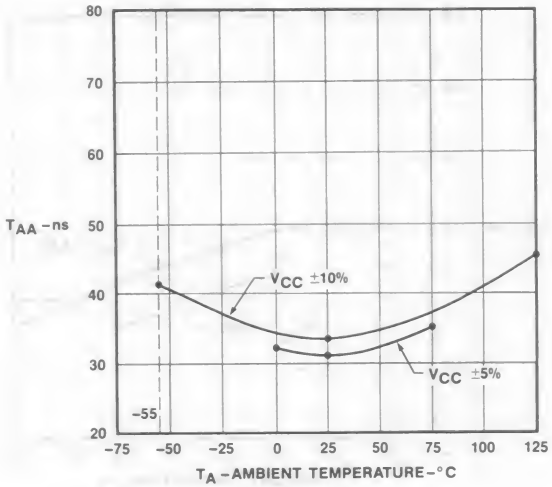


53/6301

Typical I_{CC} vs Temperature

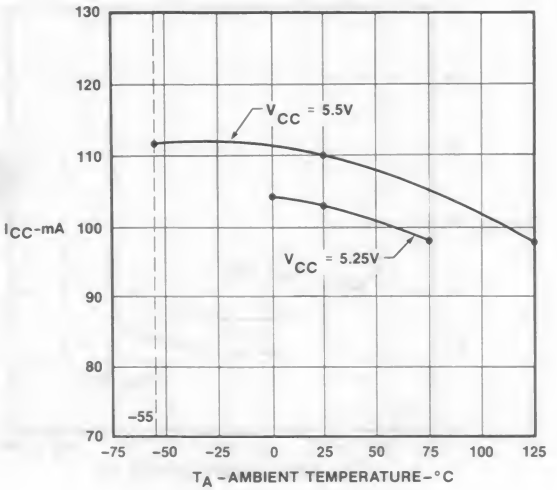


Typical T_{AA} vs Temperature

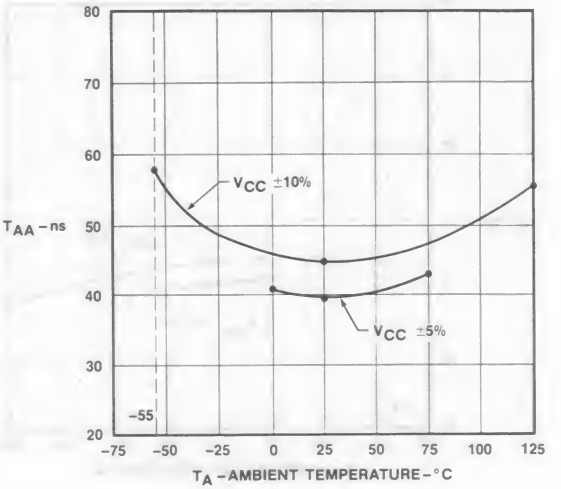


53/6306

Typical I_{CC} vs Temperature

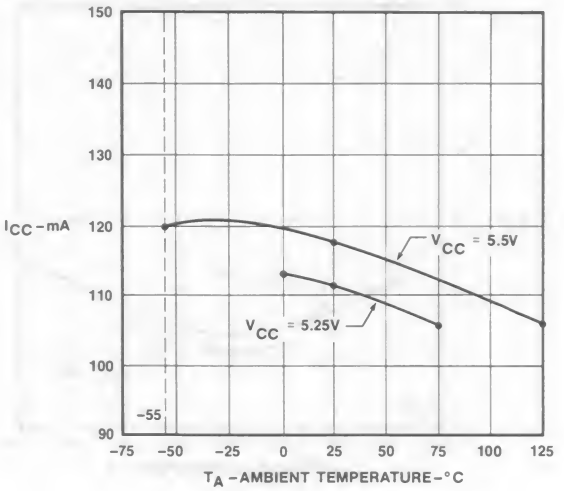


Typical T_{AA} vs Temperature

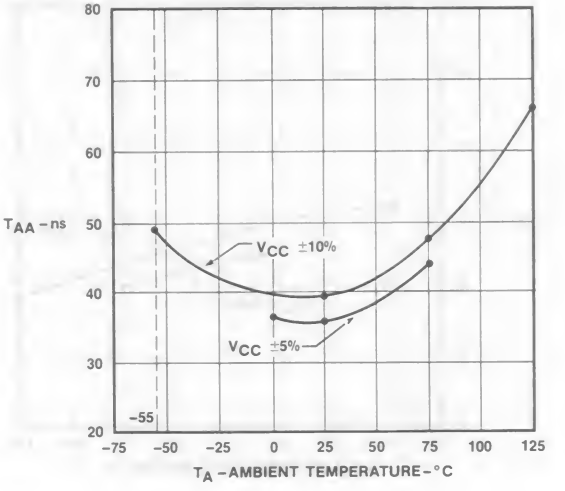


53/6309

Typical I_{CC} vs Temperature

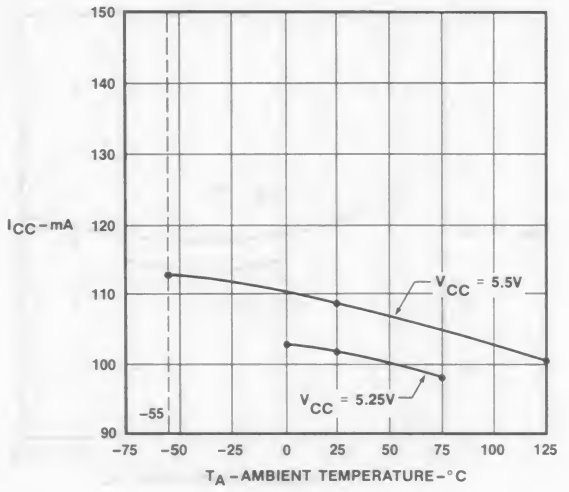


Typical T_{AA} vs Temperature

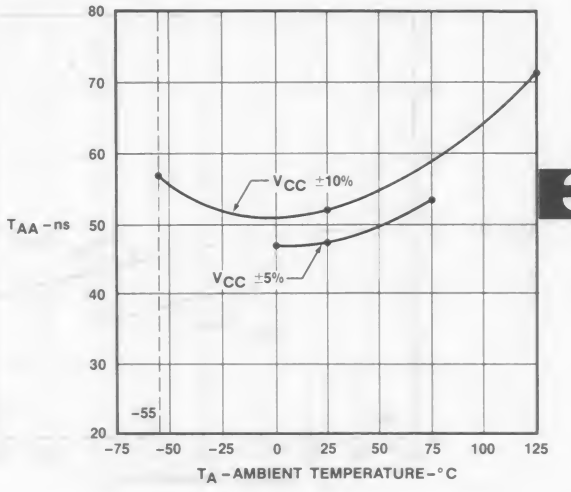


53/6336
53/6341
53/6349

Typical I_{CC} vs Temperature



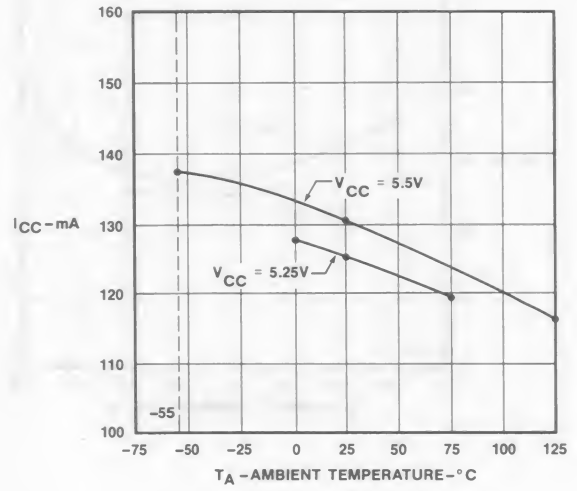
Typical T_{AA} vs Temperature



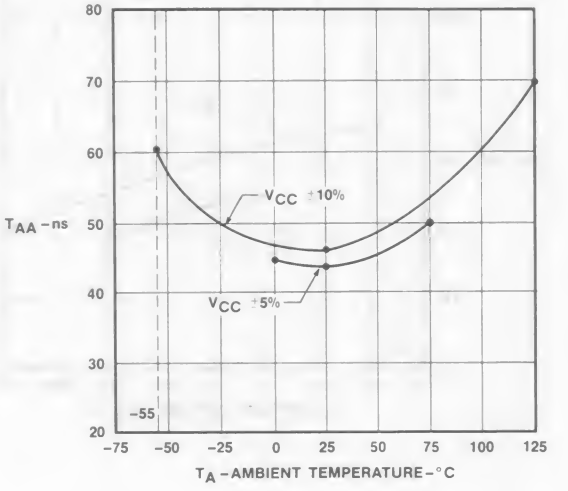
3

53/6353

Typical I_{CC} vs Temperature

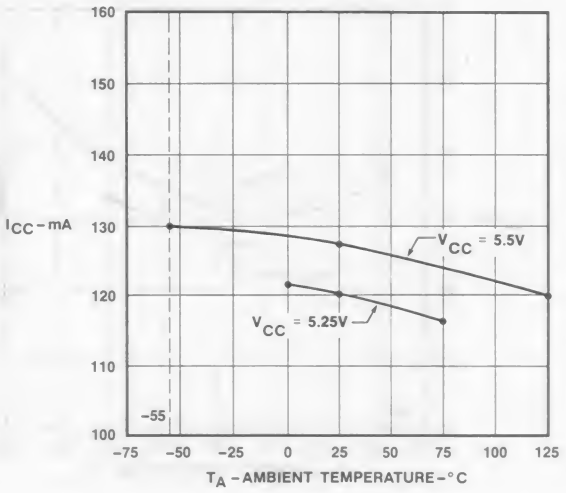


Typical T_{AA} vs Temperature

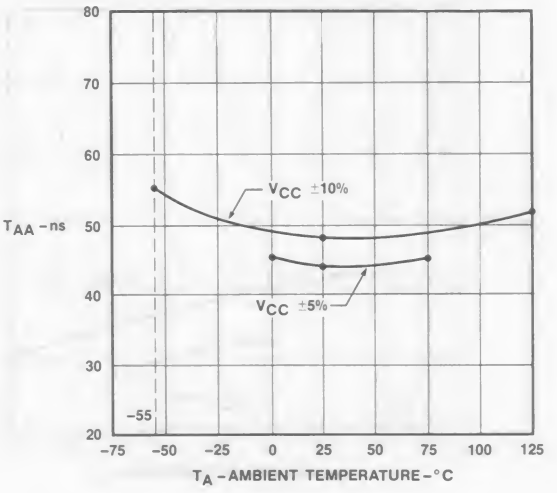


53/6389

Typical I_{CC} vs Temperature

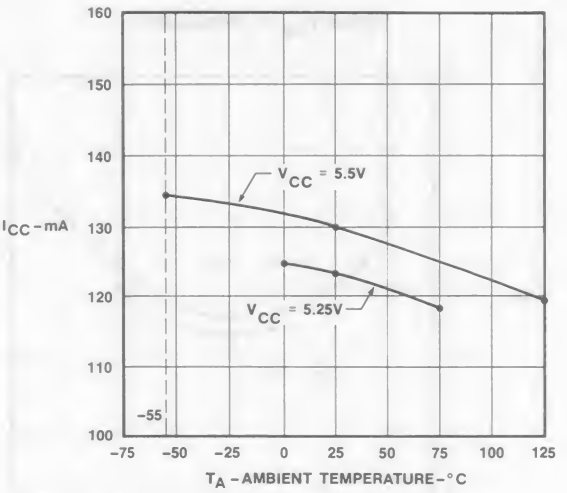


Typical T_{AA} vs Temperature

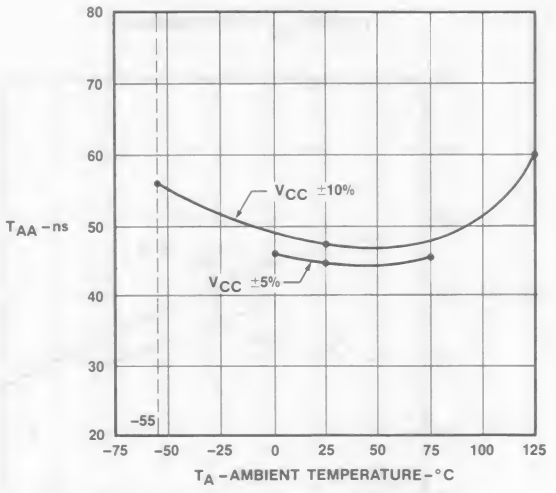


53/6381

Typical I_{CC} vs Temperature

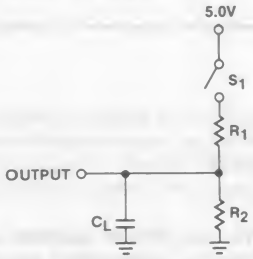


Typical T_{AA} vs Temperature



NOTE: Typical characteristic curves are for three-state devices. Equivalent open collector devices decrease in I_{CC} approximately 10 mA and increase in T_{AA} approximately 6 ns.

Switching Test Load

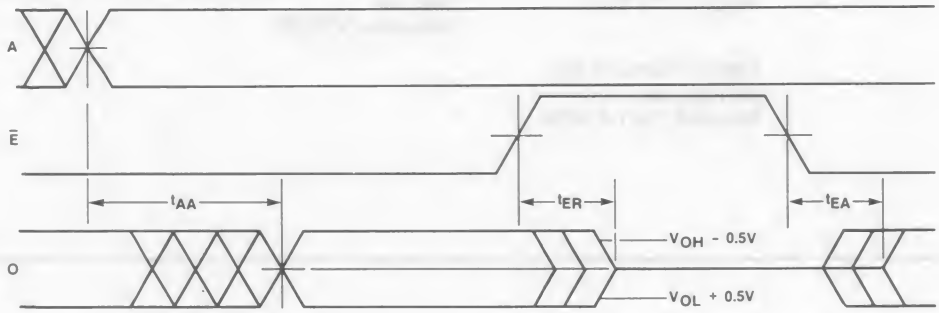


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

3

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

3. Input access measured at the 1.5V level.

4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.

5. For open collector devices. TEA and TER are measured at the 1.5V output level with S_1 closed and C_L = 30pF.

6. For three-state devices, TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   TER is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 97%. If your programming yield is lower, check you programmer. It may not be properly calibrated. (See Figure 1).

Programming is final manufacturing—it must be quality-controlled. Eqùipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION		
	Data I/O Corp. P.O. Box 308 Issaquah, WA 98027	Digelec Inc. 7335 E. Acoma DR Suite 103 Scottsdale, AZ 85260
	Kontron Electronic, Inc. 630 Price Ave. Redwood City, CA 94036	

NiCr PROM
Programming Instructions
53/63XX

Description

The 53/63XX Generic PROM Family is manufactured with outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be opened. This procedure is called programming.

Programming Procedure (See Figure 1)

1. Apply the desired address to the inputs.
2. Enable Inputs may be left at any state. *
3. Apply 5.5V to V_{CC}.
4. Apply V_{PP} to the program pin. (This step is not used on the 32x8 PROM) *
5. Apply V_{OUT} to the output to be programmed.
6. Remove V_{OUT}.
7. Remove V_{PP}.
8. Verification may be performed after each bit or word or after completing the programming of all memory locations.

In order to avoid misprogramming the PROM only one output at time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5K Ω resistors.

* The 5330/1 and 6330/1 do not have a program pin. For these devices the output only is used in programming a particular selected bit and the device must be in the disabled state.

Verification Procedure (See Figure 2)

1. Enable the device.
2. To verify low-state:
   - 2A. Apply an address where the output should be low.
   - 2B. Apply 4.2V to V_{CC}.
   - 2C. Load the output with I_{OL} = 12 mA.
   - 2D. Check that the output is less than 0.8V.
3. To verify High-state:
   - 3A. Apply an address where the output should be high.
   - 3B. Apply 6V to V_{CC}.
   - 3C. Load the output with I_{OH} = -0.3 mA.
   - 3D. Check that the output is higher than 4.5V.

3

Programming Parameters Do not test these parameters or you will program the device.

SYMBOL	PARAMETER	CONDITIONS TA = +25° C	FIGURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_R	Slew rate of Programming Pulses †			0.3		0.5	V/μs
V_{CCP}	VCC During Programming			5.4	5.5	5.6	V
	Maximum Duty Cycle					25	%
V_{PP}	Programming Voltage on Program Pin *		1	27		33	V
V_{OUT}	Programming Voltage on Output Pin *		1	20		26	V
t_{D1}	Delay between VPP and VOUT		1	0	10	20	μs
t_{D2}				0	0.5	1	
t_p	Pulse width of V_{OUT}		1	10		40	μs
V_{OLV}	VOL during verification	Chip enabled IOL = 12 mA VCC = 4.2V	2			0.8	V
V_{OHV}	VOH during verification	Chip enabled IOH = 0.3 mA VCC = 6V	2	4.5			V

*Voltage supply must be capable of supplying at least 240 mA.

†Leading edge of VPP and VOUT

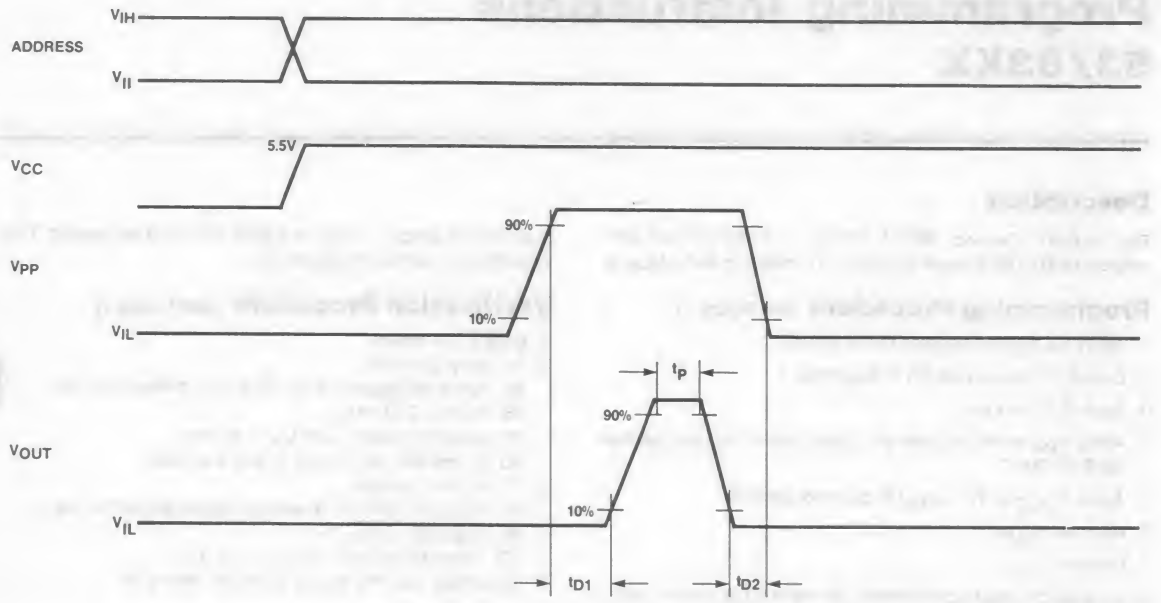


Figure 1. Programming Timing Diagram

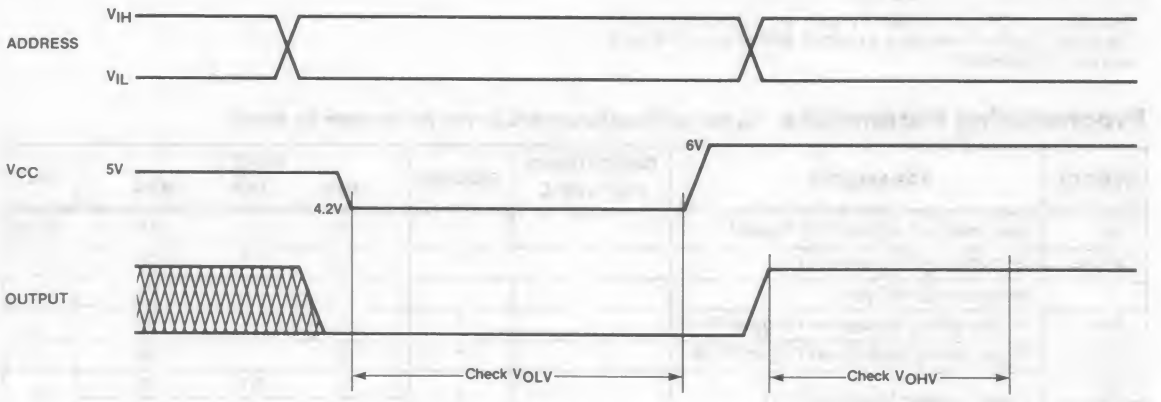
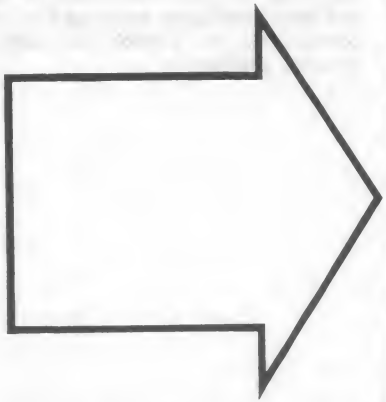


Figure 2. Verification Timing Diagram

Optimized Programming Algorithm

1. Pulse all fuses to be programmed with single, minimum voltage programming pulses (line 1 in the table).
2. Verify all fuses at low V_{CC} (4.2V). During this step, unprogrammed fuses are pulsed up to eight more times (see table).
3. Re-verify at low V_{CC} (4.2V) and high V_{CC} (6V).

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V



Generic ROM
52/62XX-1 52/62XX-2

Features/Benefits

- High bit density up to 16K
- PNP inputs for low input current
- High speed Schottky technology
- Open collector or three state outputs

Applications

- Character generator
- Look up table
- Microprocessor program store
- Microprogram store
- Random logic
- Code converter

Description

The 52/6200 series generic ROM family is available in sizes from 8K through 16K bits. The 8-bit-wide ROMs are available as 1Kx8 and 2Kx8 organization. Additional 9-bit and 10-bit-wide output configurations are available for custom logic or character generator applications.

Generic ROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION				COMMERCIAL	MILITARY
8192	1024x8	OC	J24	F24	6280-1	5280-1
		TS		F24	6281-1	5281-1
		OC		F4-24	6280-2	5280-2
		TS		F4-24	6281-2	5281-2
		OC		F24	6282-1	5282-1
		TS		F24	6283-1	5283-1
9216	1024x9	OC	J24		6260-1	5260-1
		TS			6261-1	5261-1
10240	1024x10	OC	J24		6255-1	5255-1
		TS			6256-1	5256-1
10368	1152x9	OC	J24		6290*	5290*
		TS			6291*	5291*
16384	2048x8	OC	J24		6275-1	5275-1
		TS			6276-1	5276-1

*Detailed information in section 5 (character generators)

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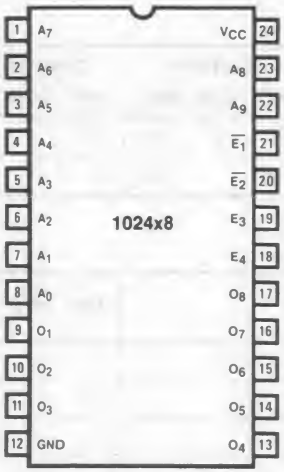
Monolithic Memories MMI

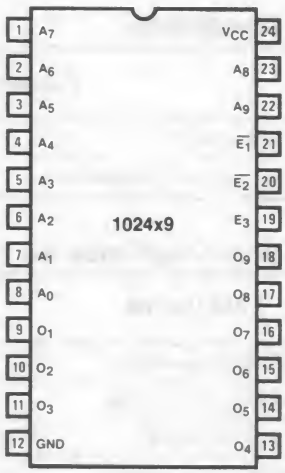
Pin Configurations

52/6280-1 52/6280-2 *52/6282-1
52/6281-1 52/6281-2 *52/6283-1

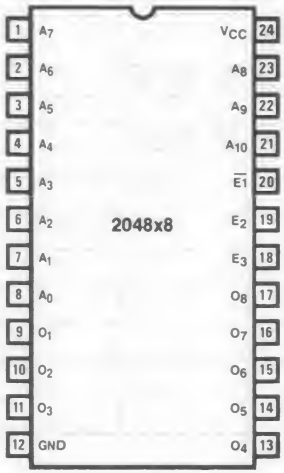


*"OR" ENABLE = $\overline{E1}$ $\overline{E2}$ + E3 E4

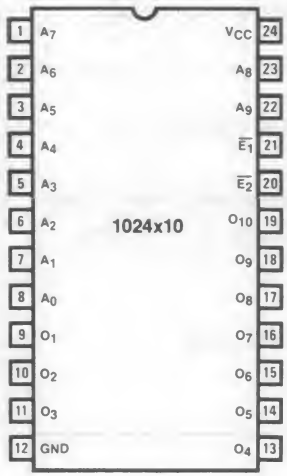
52/6260-1
52/6261-1



52/6275-1
52/6276-1



52/6255-1
52/6256-1



4

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1.0	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 8mA	'75, '76, '80, '81, '82, '83		0.5	V
			COM	I_{OL} = 10mA				
			MIL, COM	I_{OL} = 6mA	'55, '56, '60, '61			
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = –1mA		2.4		V
			COM	I_{OH} = –2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_O = 0.5V	'80, '81, '82, '83, '55, '56, '60, '61				–50	μA
			'75, '76				–100	
I_{OZH}		V_{CC} = MAX, V_O = 2.4V	'80, '81, '82, '83, '55, '56, '60, '61				50	μA
			'75, '76				100	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5.0V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded, All outputs open	'55, '60				165	mA
			'56, '61				175	
			'82 '83			113	155	
			'80, '81			113	155	
			'75, '76				190	

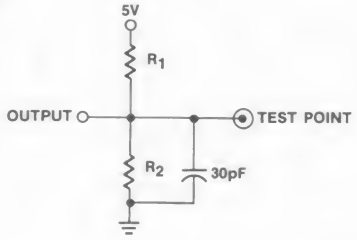
Switching Characteristics

Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} (ns) ENABLE ACCESS TIME	t_{ER} (ns) ENABLE RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	MAX	R1Ω	R2Ω
6255-1, 6256-1	100	70	40	750	1500
5255-1, 5256-1	150	80	45		
6260-1, 6261-1	100	70	40		
5260-1, 5261-1	150	80	45		
6275-1, 6276-1	110	40	40	560	1110
5275-1, 5276-1	120	50	50		
6280-1, 6281-1	80	70	45		
5280-1, 5281-1	140	90	50		
6280-2, 6281-2	55	30	30		
5280-2, 5281-2	75	35	35		
6282-1, 6283-1	80	70	45		
5282-1, 5283-1	140	90	50		

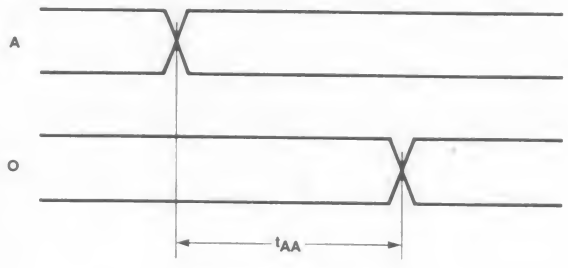
4

Standard Test Load

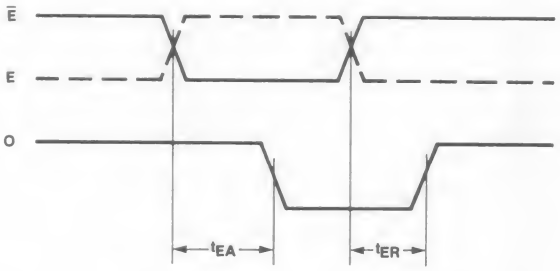


Input Pulse Amplitude
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements made at 1.5V

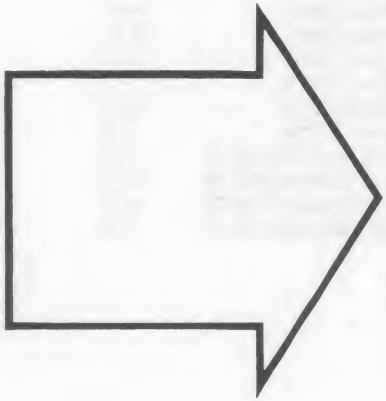
Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time



CHARACTER GENERATORS

High Speed Character Generators

Features/Benefits

- 100 ns max. access time
- Low power dissipation—500 mW
- Standard packaging—18 pin dip/24 pin dip
- Single 5 volt supply
- 64/128 characters in one package
- Open collector or three-state

Applications

- CRT displays
- Printing calculators
- LED arrays
- Typesetting

Description

The intended application for these devices is the generation of 64 or 128 ASCII alpha-numeric characters utilizing a read out system which generates the characters either horizontally or vertically, one word line at a time.

5

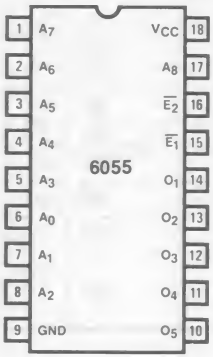
Character Generator Selection Guide

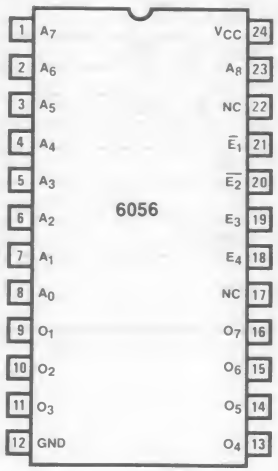
GENERIC PART NO.	CHARACTERS NO.	CHARACTERS TYPE	MATRIX	SCAN	COMMERCIAL OC	COMMERCIAL TS	MILITARY OC	MILITARY TS	PKG
6055	64	ASCII	5 x 7	Row	6055	6155	5055	5155	J18
6056 †			5 x 7	Column	6056	6156	*	*	J24
6071			7 x 9	Row	6071	6171	*	*	J24
6061 †	128	ASCII	5 x 7	Row	6061	6161	*	*	J24
6062 †			5 x 7	Column	6062	6162	*	*	
6072			7 x 9	Row	6072	6172	*	*	
6290	128	Custom	7 x 9	Row	6290	6291	5290	5291	J24
6292			9 x 9	Row/Column	6292	6293	5292	5293	

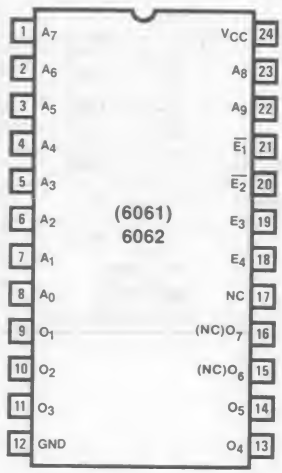
* For military versions of these Character Generators contact the factory.

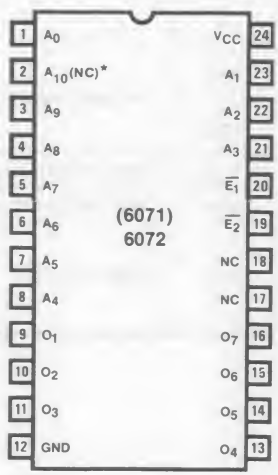
† "OR" enable = $\overline{E1}$ $\overline{E2}$ + E3 E4

Pin Configurations









* NC = no connection

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Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

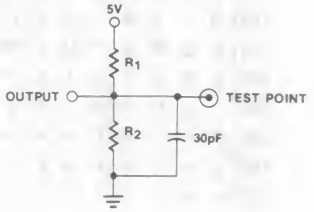
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 8mA	'55, '56, '61, '62			0.5	V
			COM I_{OL} = 10mA					
			I_{OL} = 6mA	'71, '72				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = –1mA		2.4			V
			COM I_{OH} = –2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX, V_O = 0.5V	'55, '56, '61, '62				–50	μA
			'71, '72				–100	
I_{OZH}		V_{CC} = MAX, V_O = 2.4V	'55, '56, '61, '62				50	μA
			'71, '72				100	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded, All outputs open	Open collector				170	mA
			Three state				180	

Switching Characteristics

Over Operating Conditions

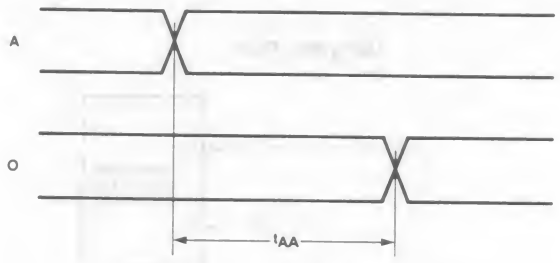
DEVICE TYPE	tAA(ns) ADDRESS ACCESS TIME	tEA(ns) ENABLE ACCESS TIME	tER(ns) ENABLE RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	MAX	R1Ω	R2Ω
6X55, 6X56, 6X61, 6X62	100	70	45	560	1100
5055, 5155	175	90	50		
6X71, 6X72	125	75	40	750	1500

Standard Test Load

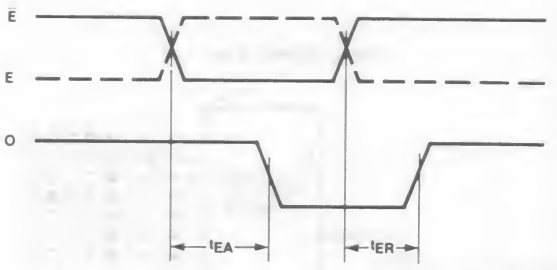


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Tabulation by Octal Select-Code

64 ASCII Characters

Row Scan 6055, 6071
Column Scan 6056

	0	1	2	3	4	5	6	7
0	@	A	B	C	D	E	F	G
10	H	I	J	K	L	M	N	O
20	P	Q	R	S	T	U	V	W
30	X	Y	Z	[	\	]	↑	←
40		!	"	#	$	%	&	'
50	(	)	*	+	,	—	.	/
60	0	1	2	3	4	5	6	7
70	8	9	:	;	<	=	>	?

Example:

The Character $ is addressed by the octal code 44

128 ASCII Characters

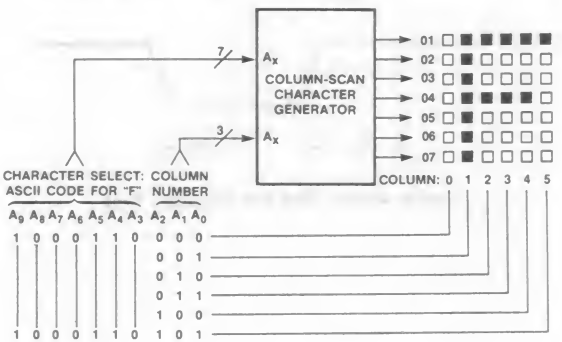
Row Scan 6061, 6072
Column Scan 6062

	0	1	2	3	4	5	6	7
0	△	△	△	△	△	△	△	△
10	△	△	△	△	△	△	△	△
20	△	△	△	△	△	△	△	△
30	△	△	△	△	△	△	△	△
40		!	"	#	$	%	&	'
50	(	)	*	+	,	—	.	/
60	0	1	2	3	4	5	6	7
70	8	9	:	;	<	=	>	?
100	@	A	B	C	D	E	F	G
110	H	I	J	K	L	M	N	O
120	P	Q	R	S	T	U	V	W
130	X	Y	Z	[	\	]	↑	←
140	'	a	b	c	d	e	f	g
150	h	i	j	k	l	m	n	o
160	p	q	r	s	t	u	v	w
170	x	y	z	{	|	}	~	△

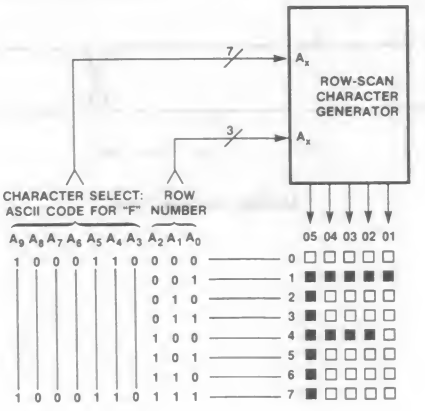
△ This ASCII code represents a control character.
For the corresponding display character see the detailed data sheet.

Generation of the Letter "F"

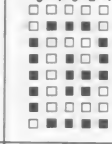
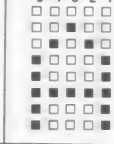
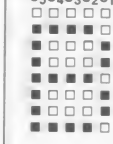
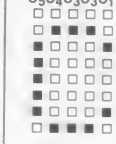
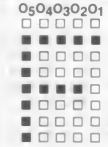
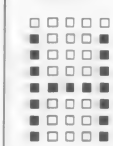
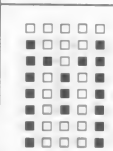
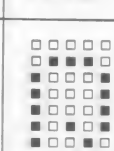
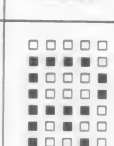
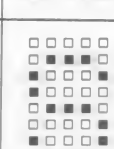
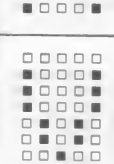
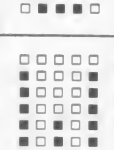
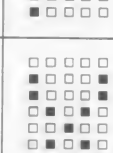
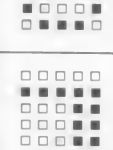
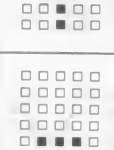
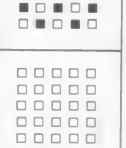
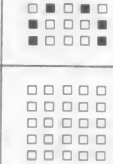
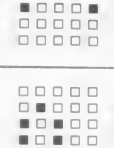
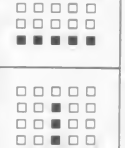
Using Column Scan



Using Row Scan

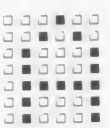
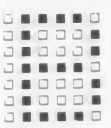
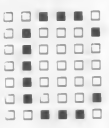
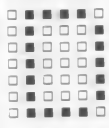
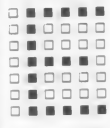
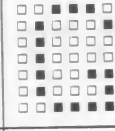
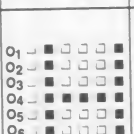
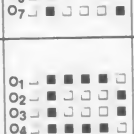
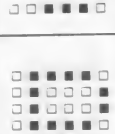
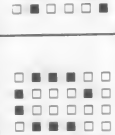
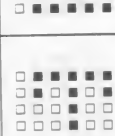
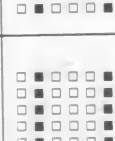
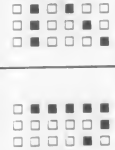
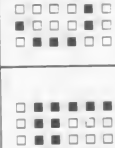
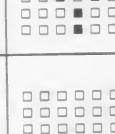
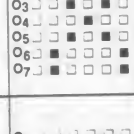
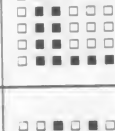
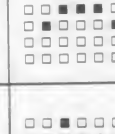
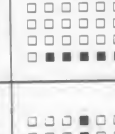


A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_8 A_7 A_6 0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

5

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_8 A_7 A_6 0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

A "Filled In" Square Represents a Low Memory Output

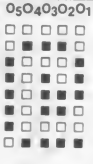
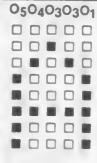
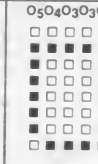
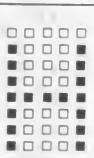
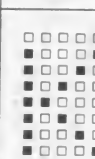
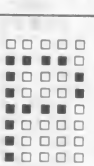
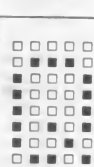
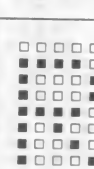
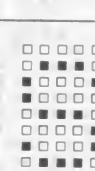
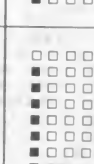
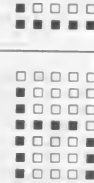
ASCII INPUT ADDRESS	A_6 A_5 A_4 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$
A_9 A_8 A_7 0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_9 A_8 A_7 A_6 0 0 0 0	$O_5O_4O_3O_2O_1$ (NUL)*	$O_5O_4O_3O_2O_1$ (SOH)*	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$ (ETX)*	$O_5O_4O_3O_2O_1$ (EOT)*	$O_5O_4O_3O_2O_1$ (ENQ)*	$O_5O_4O_3O_2O_1$ (ACK)*	$O_5O_4O_3O_2O_1$ (BEL)*
0 0 0 1	(BS)*	(HT)*	(LF)*	(VT)*	(FF)*	(CR)*	(SO)*	(SI)*
0 0 1 0	(DLE)*	(DC1)*	(DC2)*	(DC3)*	(DC4)*	(NAK)*	(SYN)*	(ETB)*
0 0 1 1	(CAN)*	(EM)*	(SUB)*	(ESC)*	(FS)*	(GS)*	(RS)*	(US)*
0 1 0 0								
0 1 0 1								
0 1 1 0								
0 1 1 1								

* The letters in parenthesis identify the control code corresponding to the appropriate pictorial represention. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_9 A_8 A_7 A_6 1 0 0 0	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 	$O_5O_4O_3O_2O_1$ 
1 0 0 1								
1 0 1 0								
1 0 1 1								
1 1 0 0								
1 1 0 1								
1 1 1 0								
1 1 1 1								(DEL)*

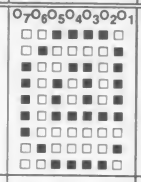
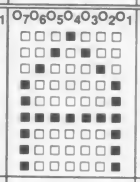
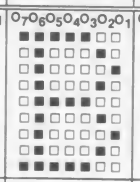
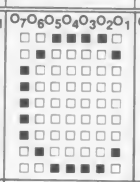
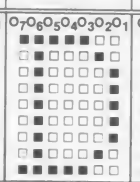
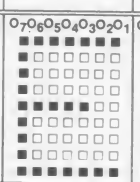
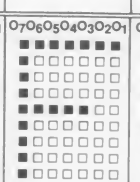
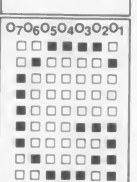
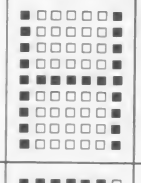
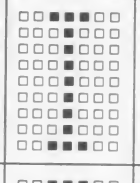
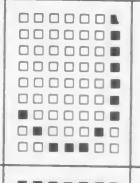
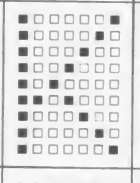
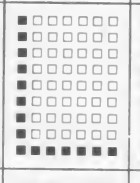
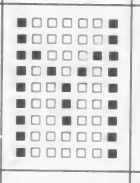
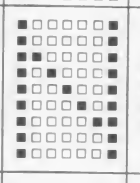
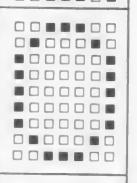
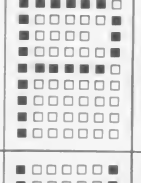
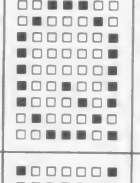
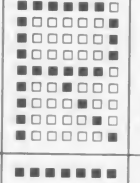
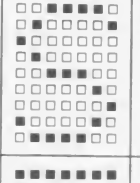
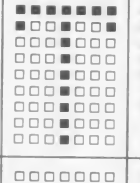
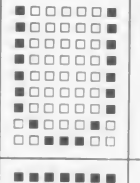
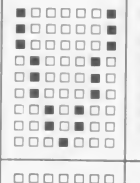
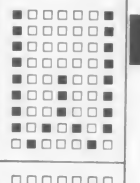
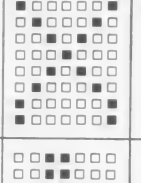
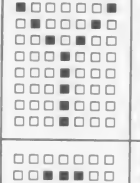
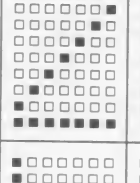
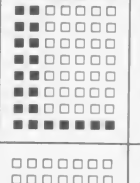
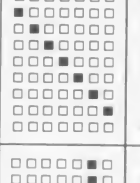
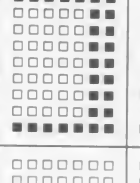
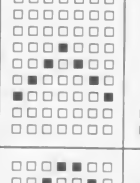
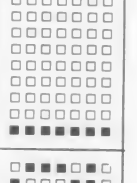
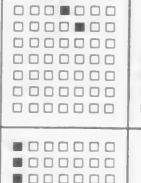
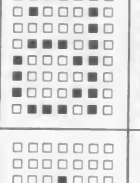
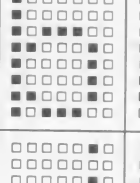
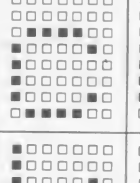
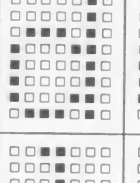
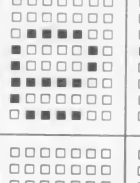
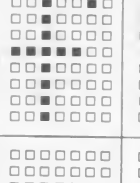
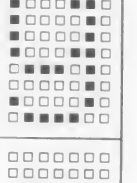
5

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_6 A_5 A_4 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_{10} A_9 A_8 A_7 0 0 0 0	$O_7O_6O_5O_4O_3O_2O_1$ (NUL)*	$O_7O_6O_5O_4O_3O_2O_1$ (SOH)*	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$ (ETX)*	$O_7O_6O_5O_4O_3O_2O_1$ (EOT)*	$O_7O_6O_5O_4O_3O_2O_1$ (ENQ)*	$O_7O_6O_5O_4O_3O_2O_1$ (ACK)*	$O_7O_6O_5O_4O_3O_2O_1$ (BEL)*
0 0 0 1	(BS)*	(HT)*	(LF)*	(VT)*	(FF)*	(CR)*	(SO)*	(SI)*
0 0 1 0	(DLE)*	(DC1)*	(DC2)*	(DC3)*	(DC4)*	(NAK)*	(SYN)*	(ETB)*
0 0 1 1	(CAN)*	(EM)*	(SUB)*	(ESC)*	(FS)*	(GS)*	(SX)*	(US)*
0 1 0 0								
0 1 0 1								
0 1 1 0								
0 1 1 1								

*The letters in parenthesis identify the control code corresponding to the appropriate pictorial represention.
These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_6 A_5 A_4 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$
$A_{10}A_9A_8A_7$ 1 0 0 0								
1 0 0 1								
1 0 1 0								
1 0 1 1								
1 1 0 0								
1 1 0 1								
1 1 1 0								
1 1 1 1								(DEL)*

5

High Speed Custom Character Generators

52/6290 52/6291 52/6292 52/6293

Features/Benefits

- Schottky—high speed 10MHz
- Specifically designed for custom 7 x 9 row scan and 9 x 9 font character generators
- Up to 128 characters in one package
- Low power dissipation—500mW
- Standard packaging—24 pin dip
- Single 5 volt supply
- 125 ns max. access time

Applications

- A single package high speed bipolar replacement for slow multiple package MOS character generators
- CRT displays
- Printing calculators
- LED arrays
- Typesetting
- Navigation systems

Description

A 7 x 9 font row scan character has 7 outputs and 9 rows per character. The character is formed one row at a time. 9 words of a ROM with 7 outputs per word are required for each character. 128 characters required on 1152 x 7 ROM which is the size of the 5290/1, 6290/1. For custom column scan 7 x 9 characters consult the standard bipolar 7 x 9 character generator data sheet.

A 9 x 9 font character has 9 outputs and 9 rows of columns per character depending upon whether we are forming a row or column scan. 9 words of a ROM with 9 outputs per row are required for each character. 128 characters require an 1152 x 9 ROM which is the 5292/3, 6292/3.

A_3, A_2, A_1, and A_0 pins are used to scan through the 9 ROM words per character. This is usually implemented by "short counting" a 4-bit binary counter so that it counts from 0000 to 1000 (9 counts) continuously (See applications section). A_4 thru A_{10} are used to pick one of the 128 characters. A_4 is the least significant binary digit and A_{10} is the most significant binary digit. The enable E_1, and E_2 must both be low to activate the part. A disabled part (E_1 or E_2 high) has high memory outputs permitting wire ORing or blanking.

Custom Font

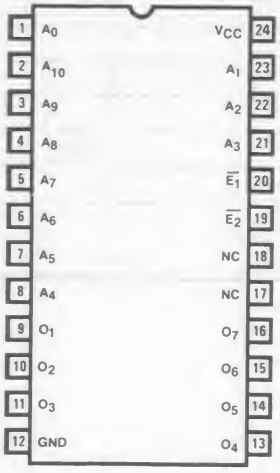
It's easy to go from custom font to the punched card or tape format preferred by Monolithic Memories Inc. Several examples are shown. We have arbitrarily assumed that a character is formed by a series of low memory outputs in a background of high memory outputs. The assumption, of course can be reversed.

Selection Guide

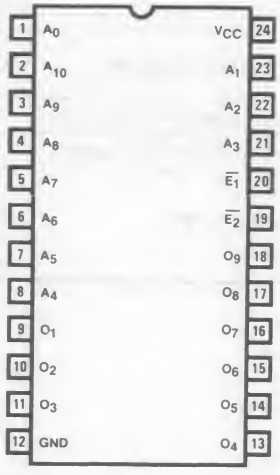
COMMERCIAL		MILITARY		MATRIX	SCAN	CHARACTERS	
OC	TS	OC	TS			NO.	TYPE
6290	6291	5290	5291	7 x 9	Row	128	Custom
6292	6293	5292	5293	9 x 9	Row/ Column		

Pin Configuration

5290/1, 6290/1 (7 x 9 Row Scan)



5292/3, 6292/3 (9 x 9 Row or Column Scan)



Note 1): A_0, A_1, A_2, A_3 are used for the character scan.
2): Both enables must be low to advance the device.

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature . . . . . –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

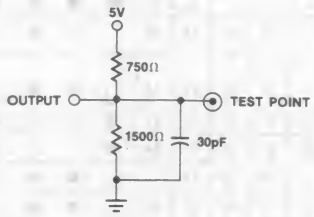
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 6mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –1mA	2.4			V
			COM I_{OH} = –2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			–100	μA
I_{OZH}		V_{CC} = MAX	V_O = 2.4V			100	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V	V_O = 0V	–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded All outputs open	Open collector			170	mA
			Three state			180	

Switching Characteristics

Over Operating Conditions

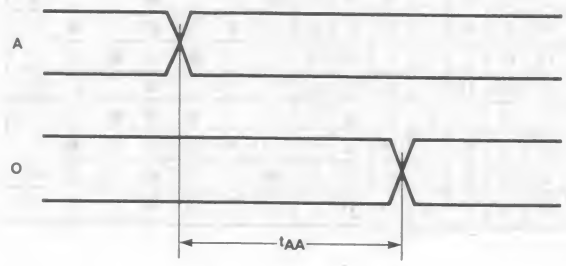
DEVICE TYPE	tAA(ns) ADDRESS ACCESS TIME	tEA(ns) ENABLE ACCESS TIME	tER(ns) ENABLE RECOVERY TIME
	MAX	MAX	MAX
6290/1, 6292/3	125	75	40
5290/1, 5292/3	150	85	50

Standard Test Load

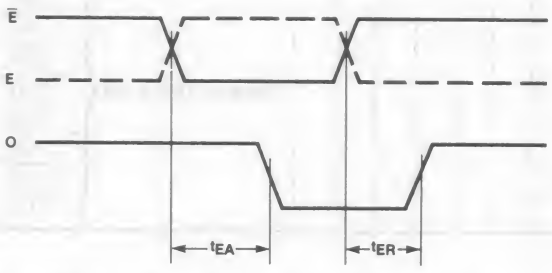


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Custom Truth Table Coding—5290/1, 6290/1

7 x 9 ROW SCAN

The characters $, &, *, are shown below along with the ROM coding. A "filled in" dot is arbitrarily coded with a low (L)

CHARACTER SELECT								A_3	A_2	A_1	A_0	ROM WORD (DECIMAL)	OUTPUTS							FONT						
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4							O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1
L	L	L	L	L	L	L	CHARACTER #1	0	0	0	0	0	H	H	L	H	L	H	H	□	□	■	□	■	□	□
								0	0	0	1	1	H	L	L	L	L	L	L	□	■	■	■	■	■	■
								0	0	1	0	2	L	H	L	H	L	H	H	■	□	■	□	■	□	□
								0	0	1	1	3	L	H	L	H	L	H	H	■	□	■	□	■	□	□
								0	1	0	0	4	H	L	L	L	L	L	H	□	■	■	■	■	■	□
								0	1	0	1	5	H	H	L	H	L	H	L	□	□	■	□	■	□	■
								0	1	1	0	6	H	H	L	H	L	H	L	□	□	■	□	■	□	■
								0	1	1	1	7	L	L	L	L	L	L	H	■	■	■	■	■	■	□
								1	0	0	0	8	H	H	L	H	L	H	H	□	□	■	□	■	□	□
L	L	L	L	L	L	H	CHARACTER #2					9	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												10	L	H	H	L	H	H	H	■	□	□	■	□	□	□
												11	L	H	H	L	H	H	H	■	□	□	■	□	□	□
												12	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												13	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												14	L	H	H	L	H	L	H	■	□	□	■	□	■	□
												15	L	H	H	H	L	L	H	■	□	□	□	■	■	□
												16	L	H	H	H	H	L	H	■	□	□	□	□	■	□
												17	H	L	L	L	L	H	L	□	■	■	■	■	□	■
H	H	H	H	H	H	H	CHARACTER #128					1143	H	H	H	L	H	H	H	□	□	□	■	□	□	□
												1144	L	H	H	L	H	H	L	■	□	□	■	□	□	■
												1145	H	L	H	L	H	L	H	□	■	□	■	□	■	□
												1146	H	H	L	L	L	H	H	□	□	■	■	■	□	□
												1147	H	H	H	L	H	H	H	□	□	□	■	□	□	□
												1148	H	H	L	L	L	H	H	□	□	■	■	■	□	□
												1149	H	L	H	L	H	L	H	□	■	□	■	□	■	□
												1150	L	H	H	L	H	H	L	■	□	□	■	□	□	■
												1151	H	H	H	L	H	H	H	□	□	□	■	□	□	□

Use of Custom Truth Table Form—5290/1, 6290/1

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 7 x 9 Row Scan example:

WORD NUMBER	PIN	OUTPUTS						
		16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		H	H	L	H	L	H	H
1		H	L	L	L	L	L	L
•		•	•	•	•	•	•	•
•		•	•	•	•	•	•	•
•		•	•	•	•	•	•	•
1151		H	H	H	L	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

Custom Truth Table Coding—5292/3, 6292/3

9 x 9 COLUMN SCAN

The characters $, &, *, can be seen in the font if this page is rotated 90° clockwise. A "filled in" dot is arbitrarily coded with a low (L).

9 x 9 ROW SCAN

The 9 x 9 row scan translation would be similar to the 7 x 9 row scan previously shown except that there would be a 9 x 9 font for each character and outputs 8 and 9 in the ROM would be used and coded.

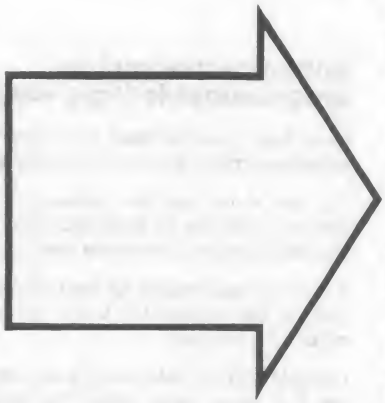
CHARACTER SELECT								ROM WORD (DECIMAL)	OUTPUTS									FONT							
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4			O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
L	L	L	L	L	L	L	CHARACTER #1	8	H	L	H	H	H	L	L	H	H	□	■	□	□	□	■	■	□	□
								7	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								6	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								5	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								4	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								3	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								2	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								1	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								0	H	H	L	L	H	H	H	L	H	□	□	■	■	□	□	□	■	□
L	L	L	L	L	L	H	CHARACTER #2	17	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
								16	H	H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■
								15	H	H	H	H	H	H	L	L	H	□	□	□	□	□	□	■	■	□
								14	H	H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■
								13	H	L	L	L	L	L	H	H	L	□	■	■	■	■	■	□	□	■
								12	L	H	H	L	L	H	H	H	L	■	□	□	■	■	□	□	□	■
								11	L	H	H	L	L	H	H	H	L	■	□	□	■	■	□	□	□	■
								10	L	H	H	L	L	H	H	L	H	■	□	□	■	■	□	□	■	□
								9	H	L	L	H	H	L	L	H	H	□	■	■	□	□	■	■	□	□
H	H	H	H	H	H	H	CHARACTER #128	1151	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
								1150	H	L	H	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□
								1149	H	H	L	H	H	H	L	H	H	□	□	■	□	□	□	■	□	□
								1148	H	H	H	L	H	L	H	H	H	□	□	□	■	□	■	□	□	□
								1147	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								1146	H	H	H	L	H	L	H	H	H	□	□	□	■	□	■	□	□	□
								1145	H	H	L	H	H	H	L	H	H	□	□	■	□	□	□	■	□	□
								1144	H	L	H	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□
								1143	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□

Use of Custom Truth Table Form—5292/3, 6292/3

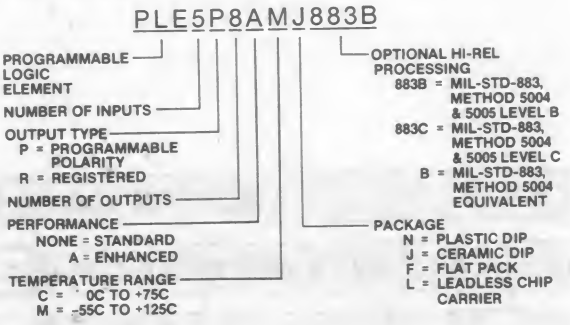
Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 9 x 9 column scan example:

WORD NUMBER	PIN	OUTPUTS								
		18 O_9	17 O_8	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		H	H	L	L	H	H	H	L	H
1		H	L	H	H	L	H	H	L	H
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
1151		H	H	H	H	H	H	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.



Ordering Information



The PLE family part numbering is a unique method of keying important attributes of the device. For example, a PLE5P8CN would be a 5 input, 8 output, programming output polarity PLE, with a commercial temperature range and packaged in a plastic dip.

PLE™ means Programmable Logic Element.

Joining the world of IdeaLogic™ is a new generation of high speed PROMs which the designer can use as *programmable logic elements*. The combination of PLEs as logic elements with PALs can greatly enhance system speed while providing almost unlimited design freedom.

By making the OR array programmable instead of the AND array as in PALs, PLEs complement PAL devices.

Basically, PLEs are ideal when a large number of product terms is required. On the other hand, a PAL is best suited for situations when many inputs are needed.

PRODUCT TERM AND INPUT LINES

	PLE	PAL
Product Terms	32 to 4096	2 to 8
Input Lines	5 to 12	10 to 20

Like PAL software, PLE assembly software is available in the form of PLEASM™. This software tool assembles the designer's equations into a PROM truth table, which in turn is used to program the device.

PLE FUNCTION CHART

PART NUMBER	IN-PUTS	OUT-PUTS	PRODUCT TERMS	TYP. T_{AA}
PLE5P8A	5	8	32	9 ns
PLE10P4	10	4	1024	23 ns
PLE11P4	11	4	2048	28 ns
PLE12P4	12	4	4096	28 ns

With PLEs the designer can form logic where any possible combination of input variables (addresses) can be transferred to any output variable.

Software that makes programmable logic easy.

Monolithic Memories offers two forms of assembler software to facilitate chip design quickly, simply, and cost-effectively.

PALASM is the dedicated software for PAL. PLEASM is the dedicated software for PLEs. Each offers the designer an easy and reliable path to achieve his exact logic design.

The design specification for both programs is similar, thus the designer can go from a PLE to a PAL, or vice versa with only minor code changes.

PLEASM is a FORTRAN IV computer program which assembles the PLE design specification by translating the designer's Boolean equations into a PLE fuse pattern. The fuse pattern may be generated in a format compatible with either a PAL or PROM programmer.

PLEASM also contains a simulator which exercises the function table vectors in the logic equation. Several benefits result. First, errors are quickly spotted as inconsistencies between the vectors and the equations. Secondly, the simulator reports how completely the function table tests the device. Finally, the simulator translates the function table vectors to a set of test vectors, which allows functional testing after the device has been fabricated.

Programmable Logic Element
PLE™ Family

Features/Benefits

- **Programmable replacement for conventional TTL logic**
- **Reduces IC inventories and simplifies their control**
- **Expedites and simplifies prototyping and board layout**
- **Saves space with .3 in SKINNYDIP® packages**
- **Programmed on standard PROM programmers**
- **Test and simulation made simple with PLEASM function table**
- **Low current PNP inputs**
- **Three state outputs**

PLE Selection Guide

PART NUMBER	PKG	DESCRIPTION
PLE5P8A	J,N,F,W(20L)	5 input, 8 output, 32 term
PLE10P4	J,N,F(20L)	10 input, 4 output, 1024 term
PLE11P4	J,N,F (28L)	11 input, 4 output, 2048 term
PLE12P4	J,N,F(28L)	12 input, 4 output, 4096 term

( ) = Military Product

The entire PAL family is programmed on conventional PROM programmers with the appropriate personality cards and socket adaptors.

Description

The PLE family features common electrical parameters and programming algorithm, low current PNP inputs, full Schottky clamping and three state outputs.

Unused inputs are tied directly to V_{CC} or GND. Terms with fuses blown assume the logical high state and terms connected to the outputs (unprogrammed fuse) assume the logic low state.

The PLE transfer function is the familiar OR of products. Like the PAL, the PLE has a single array of fusible links. Unlike the PAL, the PLE circuits have a programmable OR array driven by a fixed AND array (the PAL is a programmed AND array driving a fixed OR array).

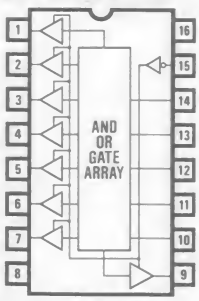
PLEASM Software

The PLEASM software is a powerful tool used for designing with PROMs as Programmable Logic Elements. PLEASM software is a computer program which assembles and simulates PLE design specifications. It also generates PLE truth tables in formats compatible with standard PROM programmers. The PLEASM software also provides these key features:

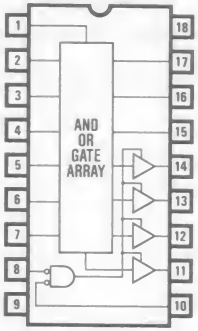
- Assembles Logic or Arithmetic equations into a PROM truth table.
- Provides HEX, BHLF and BNPF programming formats along with the hex check sum.
- Programming formats can be directly downloaded to standard PROM programmers.
- Reports design errors.

Pin Configurations

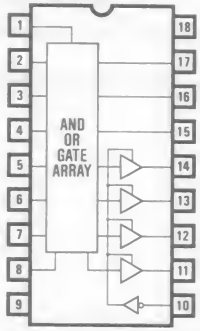
PLE5P8A



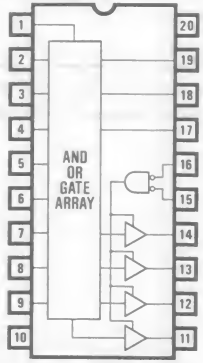
PLE10P4



PLE11P4



PLE12P4



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Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5V to 7V
Input voltage ..... -1.5V to 7V
Off-state output voltage ..... -0.5V to 5.5V
Storage temperature range ..... -65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA		2.4			V
			COM I_{OH} = -3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V				-40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current *	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.	PLE5P8			90	125	mA
			PLE10P4			95	140	
			PLE11P4			110	150	
			PLE12P4			130	175	

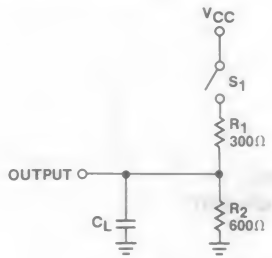
† Typical at 5.0 V_{CC} and 25°C TA.
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics

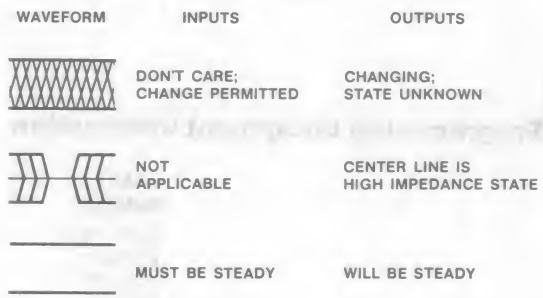
DEVICE TYPE	COMMERCIAL				MILITARY			
	t_{AA}(ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME		t_{AA}(ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME	
	TYP†	MAX	TYP†	MAX	TYP†	MAX	TYP†	MAX
PLE5P8A	9	17	9	17	9	20	9	25
PLE10P4	23	35	12	25	23	50	12	30
PLE11P4	28	35	12	25	28	50	12	30
PLE12P4	28	35	12	25	28	50	12	50

†Typicals at 5.0 V_{CC} and 25° C TA.

Switching Test Load

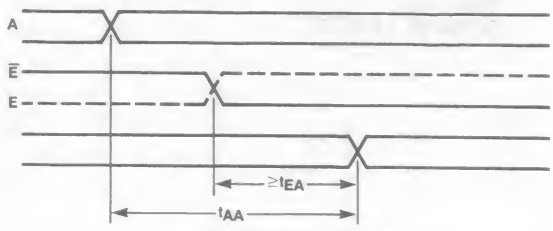


Definition of Timing Diagram

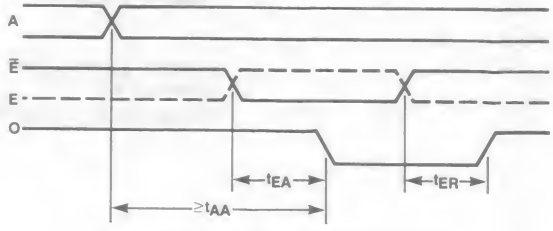


6

Definition of Waveforms



ADDRESS ACCESS TIME

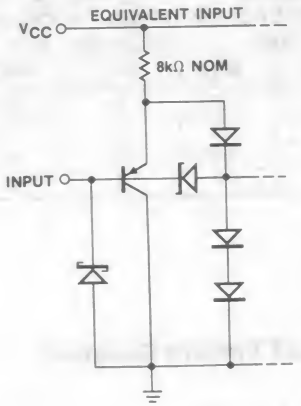


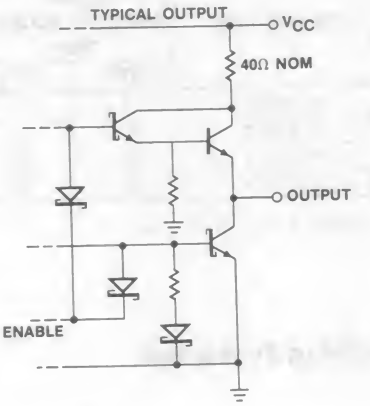
ENABLE ACCESS TIME AND RECOVERY TIME

NOTES:
1. Input pulse amplitude 0V to 3.0V.
2. Input rise and fall atimes 2-5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_l = 30pF and measured at 1.5V output level.
5. TEA and TER are measured at the 1.5V output level with S_1 closed at C_L = 30pF.
6. TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   TER is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 ouptut level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Schematic of Inputs and Outputs





Programming Equipment Information

PART NUMBER	REQUIRED PROM PROGRAMMING EQUIPMENT
PLE5P8A	63S081/A
PLE10P4	63S441/A
PLE11P4	63S841/A
PLE12P4	63S1641/A

Source and Location

Data I/O Corp.
P.O. Box 308
Issaquah, WA 98027

Kontron Electronic, Inc.
630 Price Ave.
Redwood City, CA 94036

Digelec Inc.
7335 E. Acoma DR
Suite 103
Scottsdale, AZ 85260

Programming Instructions

Device Description

All of the PLE circuits are manufactured with all outputs low in all storage locations. To produce a high at a particular location, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PROM only one output at a time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5K Ω resistors.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100ns or greater must be allowed between steps. The enabling pulse must not occur less than 100ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Programming Parameter

Do not test these parameters or you may program the device.

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

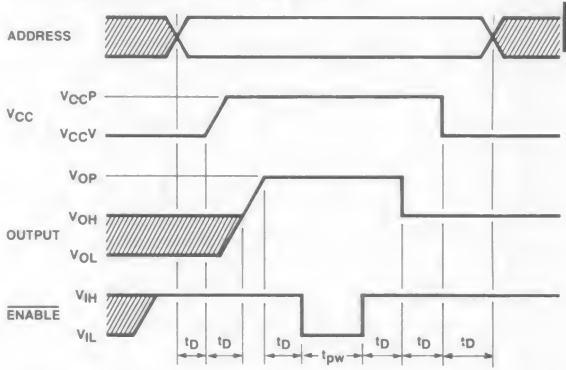
Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. Following verification, apply five additional programming pulses to the bit being programmed.

Board Level Programming

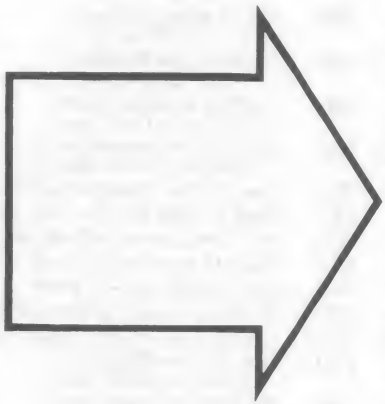
Board level programming is easily accomplished since only an enabled PLE is programmed. At the board level only the desired PLE and output should be enabled.

Programming Waveforms



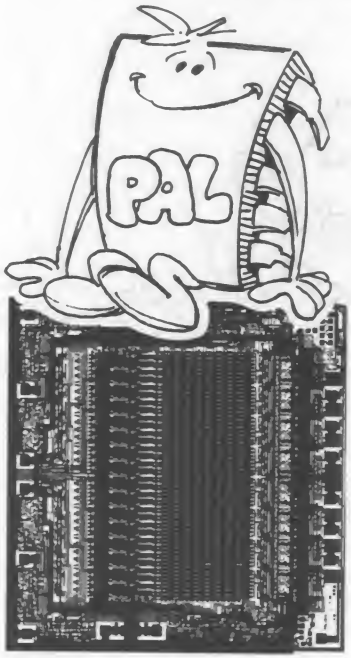
t_D = 100ns min
t_{pw} = 9μs min 11μs max

SYMBOL	PARAMETER	MIN	RECOMMENDED VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	11.5	11.75	12.0	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μs
I_{CCP}	Current limit of V_{CCP} supply	800	1200	—	mA
I_{OP}	Current limit of V_{OP} supply	15	20	—	mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μs
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}	—	25	25	%
t_D	Delay time between programming steps	100	120	—	ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V



PAL/HAL CIRCUITS

PAL/HAL LOGIC DIAGRAMS



The PAL® Concept

Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a low to medium complexity product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turn around on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL family offers a fresh approach to using fuse programmable logic. PAL circuits are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PAL devices can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL a circuit designer's best friend.

The PAL—Teaching Old PROMs New Tricks

MMI developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, MMI has the proven technology and high volume production capability required to manufacture and support the PAL.

The PAL is an extension of the fusible link technology pioneered by Monolithic Memories for use in bi-polar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon." In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to quickly and easily customize the chip to fit his unique requirements. The PAL extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. Using PAL circuits the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL implements the familiar sum of products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL circuit uses are only limited by the number of terms available in the AND – OR arrays. PAL devices come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL structure for a two input, one output logic segment. The general logic equation for this segment is

$$\text{Output} = (I_1+\overline{f_1})(\overline{I_1}+\overline{f_2})(I_2+\overline{f_3})(\overline{I_2}+\overline{f_4}) + (I_1+\overline{f_5})(\overline{I_1}+\overline{f_6})(I_2+\overline{f_7})\ (\overline{I_2}+\overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL AND array. An unblown link represents a logic 1. Thus,

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL has all fuses intact.

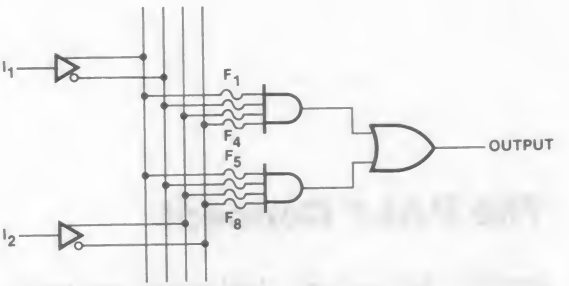


Figure 1

PAL Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL logic easy to understand and use. In the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PAL circuits. The two input - one output example from Figure 1 redrawn using the new logic convention is shown in Figure 3.

Figure 2

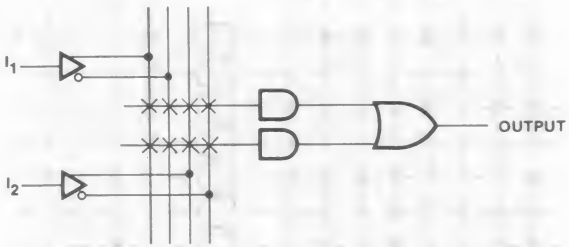


Figure 3

As a simple PAL example, consider the implementation of the transfer function:

$$\text{Output} = I_1\overline{I_2} + \overline{I_1}I_2$$

The normal combinatorial logic diagram for this function is shown in figure 4, with the PAL logic equivalent shown in figure 5.

Figure 4

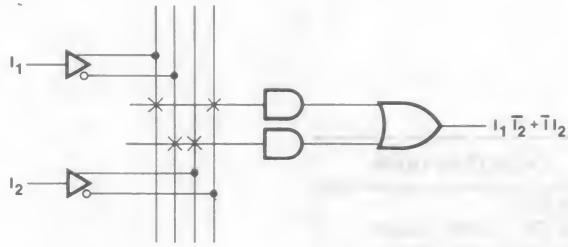


Figure 5

Using this logic convention it is now possible to compare the PAL structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

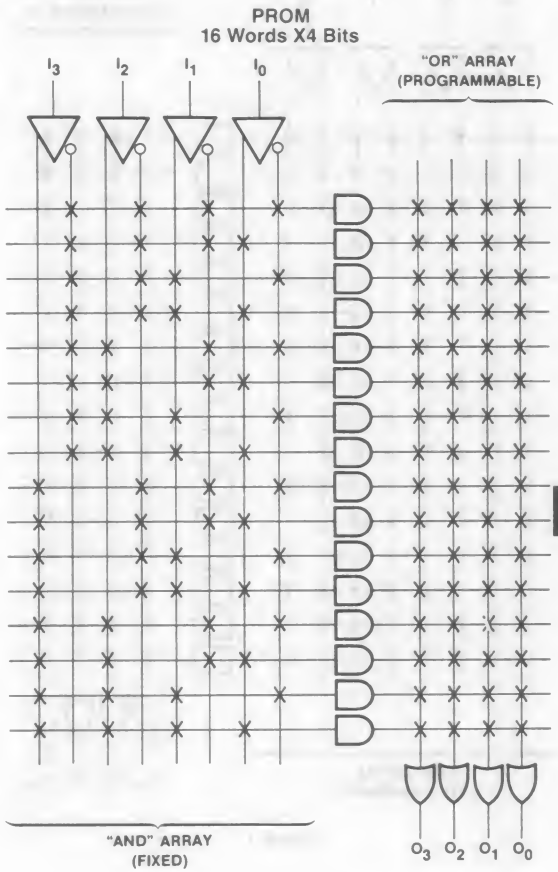


Figure 6

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality makes PLAs expensive, quite formidable to understand, and costly to program (they require special programmers).

The basic logic structure of the PAL, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL logic families.

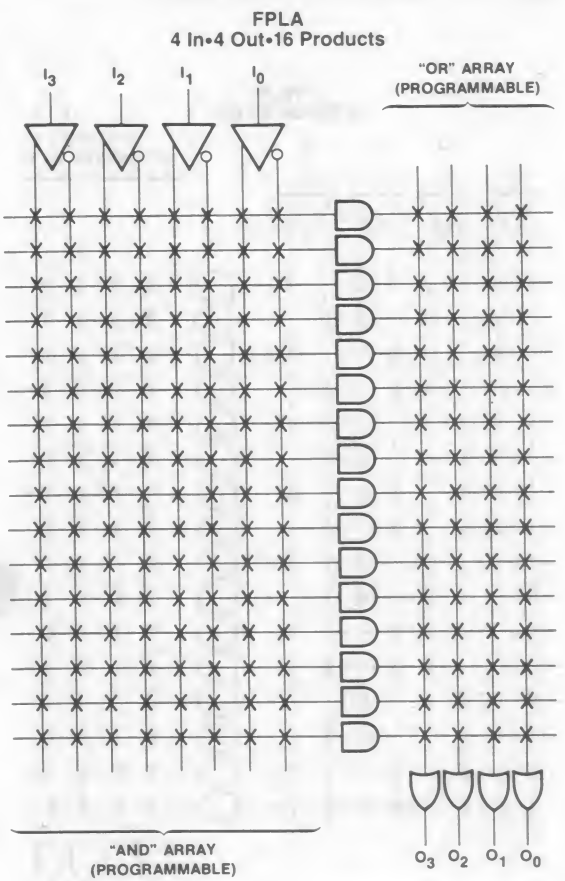


Figure 7

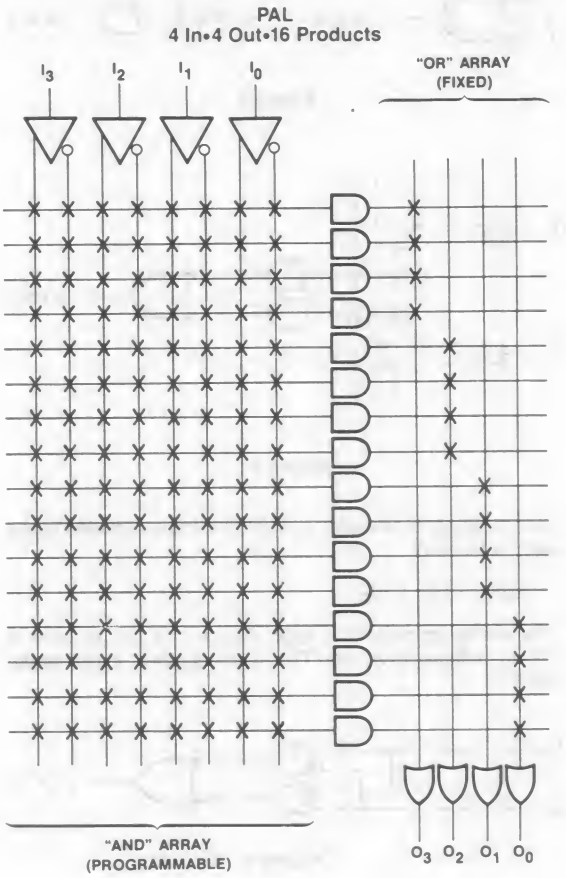


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS, OC
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL	Prog	Fixed	TS, Registered Feedback, I/O

Table 1

PAL Input/Output/Function/Performance Chart

PART NO.	INPUT	OUTPUT	PROGRAMMABLE I/O'S	FEEDBACK REGISTER	OUTPUT POLARITY	FUNCTIONS	PERFORMANCE			
							STD	A	-2	-4
10H8	10	8			AND-OR	AND-OR Gate Array	X		X	
12H6	12	6			AND-OR	AND-OR Gate Array	X		X	
14H4	14	4			AND-OR	AND-OR Gate Array	X		X	
16H2	16	2			AND-OR	AND-OR Gate Array	X		X	
16C1	16	2			BOTH[1]	AND-OR Gate Array	X		X	
20C1	20	2			BOTH[1]	AND-OR Gate Array	X			
10L8	10	8			AND-NOR	AND-OR Invert Gate Array	X		X	
12L6	12	6			AND-NOR	AND-OR Invert Gate Array	X		X	
14L4	14	4			AND-NOR	AND-OR Invert Gate Array	X		X	
16L2	16	2			AND-NOR	AND-OR Invert Gate Array	X		X	
12L10	12	10			AND-NOR	AND-OR Invert Gate Array	X			
14L8	14	8			AND-NOR	AND-OR Invert Gate Array	X			
16L6	16	6			AND-NOR	AND-OR Invert Gate Array	X			
18L4	18	4			AND-NOR	AND-OR Invert Gate Array	X			
20L2	20	2			AND-NOR	AND-OR Invert Gate Array	X			
16L8	10	2	6		AND-NOR	AND-OR Invert Gate Array	X	X	X	X
20L8	14	2	6		AND-NOR	AND-OR Invert Gate Array		X		
20L10	12	2	8		AND-NOR	AND-OR Invert Gate Array	X			
16R8	8	8		8	AND-NOR	AND-OR Invert Gate Array w/Reg's	X	X	X	X
16R6	8	6	2	6	AND-NOR	AND-OR Invert Array w/Reg's	X	X	X	X
16R4	8	4	4	4	AND-NOR	AND-OR Invert Array w/Reg's	X	X	X	X
20R8	12	8		8	AND-NOR	AND-OR Invert w/Reg's		X		
20R6	12	6	2	6	AND-NOR	AND-OR Invert w/Reg's		X		
20R4	12	4	4	4	AND-NOR	AND-OR Invert w/Reg's		X		
20X10	10	10		10	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
20X8	10	8	2	8	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
20X4	10	4	6	4	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
16X4	8	4	4	4	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
16A4	8	4	4	4	AND-NOR	AND-CARRY-OR-XOR Invert w/Reg's	X			

Table 2

[1] Simultaneous AND-OR and AND-NOR outputs

PAL Circuits For Every Task

The members of the PAL family and their characteristics are summarized in Table 2. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL that best fits his application. PAL units come in the following basic configurations:

Gate Arrays

PAL gate arrays are available in sizes from 12x10 (12 input terms, 10 output terms) to 20x2, with both active high and active low output configurations available (figure 9). This wide variety of input/output formats allows the PAL to replace many different sized blocks of combinatorial logic with single packages.

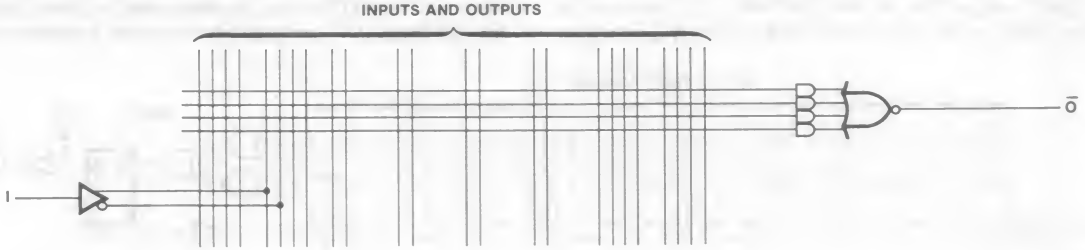


Figure 9

Programmable I/O

A feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus the PAL drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

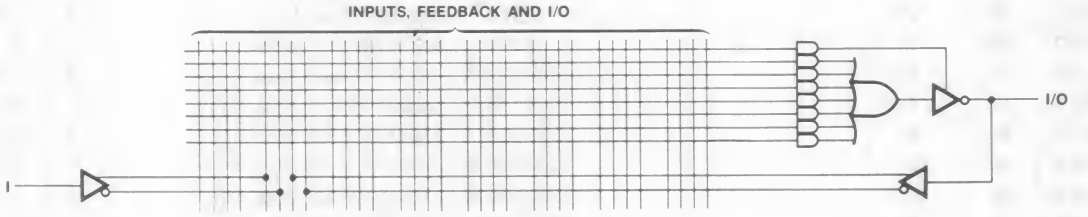


Figure 10

Registered Outputs with Feedback

Another feature of the high end members of the PAL family is registered data outputs with registered feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 11). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL at rates of up to 25 MHz.

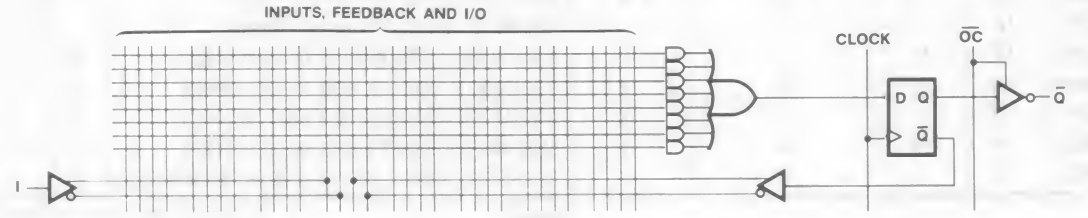


Figure 11

XOR PALs

These PAL devices feature an exclusive OR function. The sum of products is segmented into two sums which are then exclusive ORed (XOR) at the input of the D-type flip-flop (Figure 12). All of the features of the Registered PALs are included in the XOR PAL unit. The XOR function provides an easy implementation of the HOLD operation used in counters and other state sequencers.

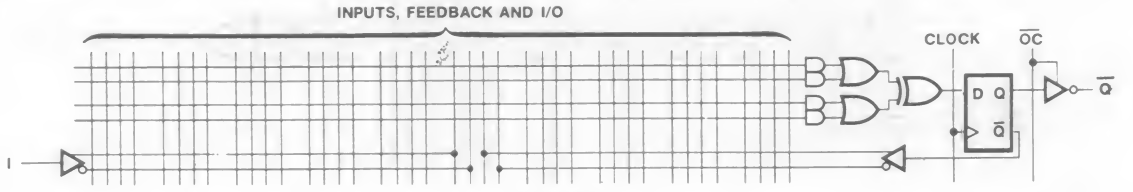


Figure 12

Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL array. The flip-flop Q output is fed back to be gated with input terms A (Figure 13). This gated feedback provides any one of the 16 possible Boolean combinations which are mapped in the Karnaugh map (Figure 15). Figure 14 shows how the PAL array can be programmed to perform these 16 operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

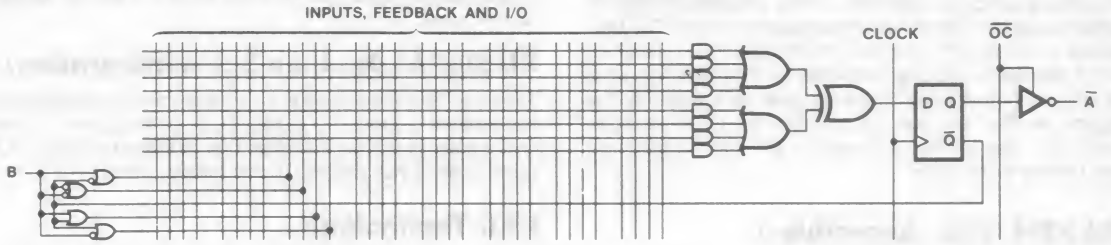


Figure 13

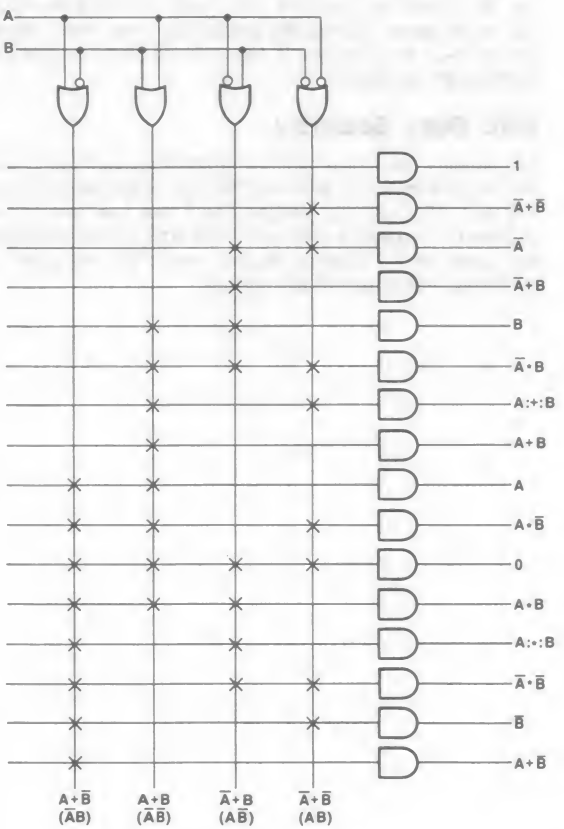


Figure 14

$(\overline{A}+B),(\overline{A}+\overline{B})$ / $(A+\overline{B}),(A+B)$	--	-x	xx	x-
--	1	$\overline{A}+\overline{B}$	$\overline{A}$	$\overline{A}+B$
-x	A+B	A:+:B	$\overline{A}\cdot B$	B
xx	A	$A\cdot\overline{B}$	0	A · B
x-	$A+\overline{B}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$	A:•:B

Figure 15

It should now be clear that the PAL family can replace most Small-Scale Integrated Logic (SSI) logic in use today, thereby lowering product cost and giving the designer even greater flexibility in implementing logic functions.

PAL Programming

PAL devices can be programmed in most standard PROM programmers with the addition of a PAL personality card. The PAL appears to the programmer as a PROM. During programming half of the PAL outputs are selected for programming while the other outputs and the inputs are used for addressing. The outputs are then switched to program the other locations. Verification uses the same procedure with the programming lines held in a low state.

PALASM (PAL Assembler)

PALASM is the software used to define, simulate, build, and test PAL units. PALASM accepts the PAL Design Specification as an input file. It verifies the design against an optional function table and generates the fuse plot which is used to program the PAL devices. PALASM is available upon request for many computers and is documented in the PAL Design Concepts section.

HAL (Hard Array Logic)

The HAL family is the mask programmed version of a PAL. The HAL is to a PAL just as a ROM is to a PROM. A standard wafer is fabricated to the 6th mask. Then a custom metal mask is used to fabricate Aluminum links for a HAL instead of the programmable Ti-W fuse array used in a PAL.

The HAL is a cost-effective solution for large quantities and is unique in that it is a gate array with a programmable prototype.

HMSI (HAL Medium Scale Integration)

The HMSI family is derived from the PAL using HAL technology. These devices perform predetermined functions which are not available in the existing TTL family. Because they are produced in volume, the user receives the benefit of volume pricing. HMSI PAL designs are given in the Applications section with their industry standard 74LS part number in line 2 of the PAL Design Specification.

PMSI (PAL Medium Scale Integration)

The PMSI family is derived in a similar fashion to HMSI except this product is produced entirely from a PAL circuit. A HAL circuit mask is not generated and an industry standard 74LS part number is not assigned unless sales warrant it.

PAL Technology

PAL circuits are manufactured using the proven TTL Schottky bipolar Ti-W fuse process to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high-impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors. Typical PAL propagation delay time is 25 ns, and all PALs are packaged in space saving 20-pin and 24-pin SKINNYDIP® packages.

PAL Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL array. For security, the PAL has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to effectively protect proprietary designs.

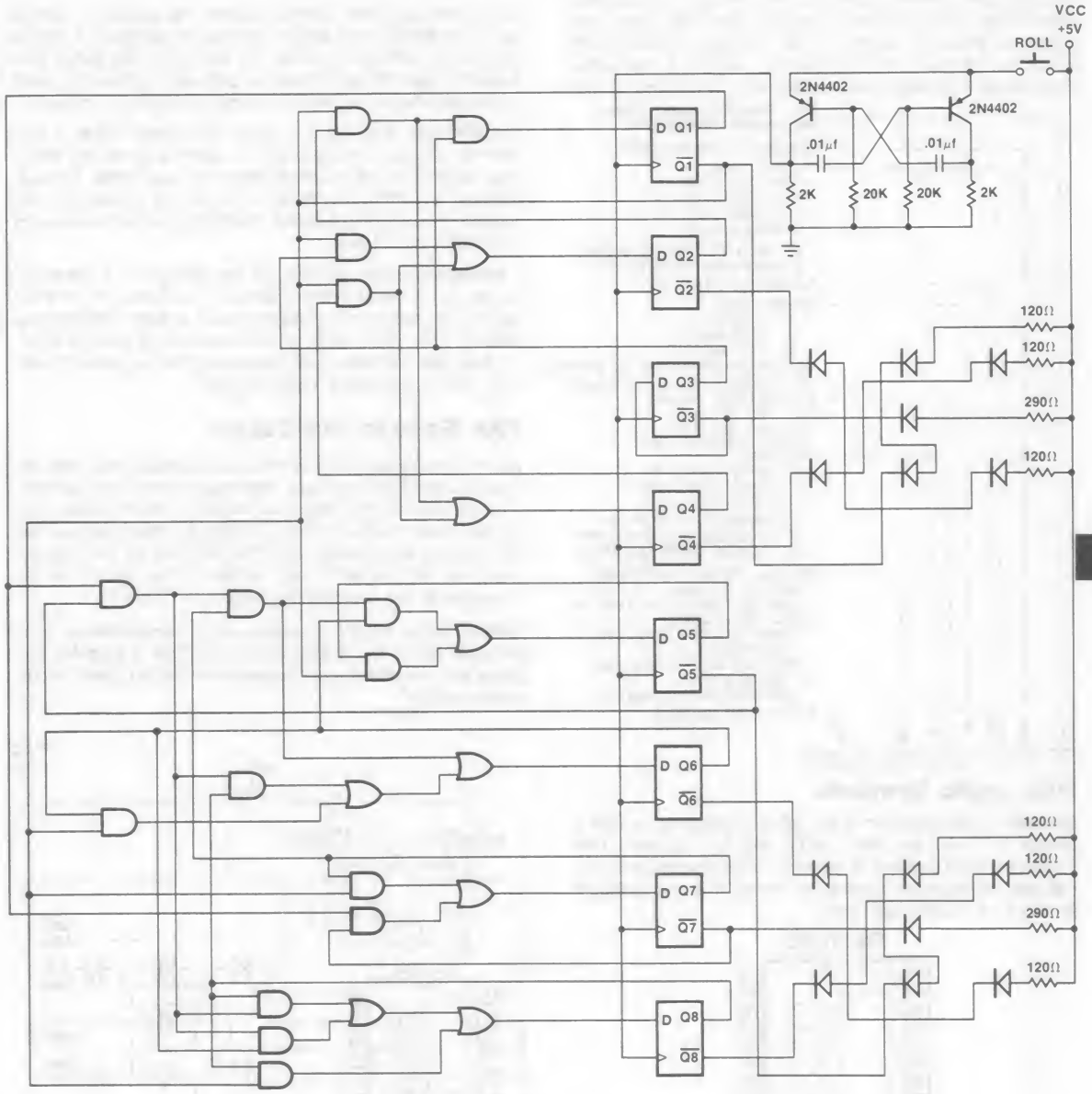
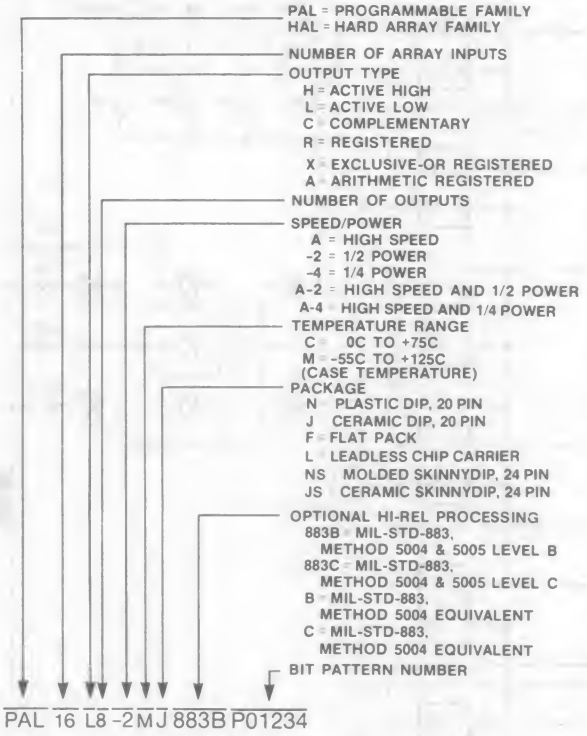

VCC
+5V
ROLL
2N4402
2N4402
.01μf
.01μf
2K
20K
20K
2K
D Q1
Q1
D Q2
Q2
D Q3
Q3
D Q4
Q4
D Q5
Q5
D Q6
Q6
D Q7
Q7
D Q8
Q8
120Ω
120Ω
290Ω
120Ω
120Ω
120Ω
290Ω
120Ω

Figure 16

PAL Part Numbers

The PAL part number is unique in that the part number code also defines the part's logic operation. The PAL parts code system is shown in Figure 17. For example, a PAL14L4CN would be a 14 input term, 4 output term, active-low PAL with a commercial temperature range packaged in a 20-pin plastic dip.



PAL Logic Symbols

The logic symbols for each of the individual PAL devices gives a concise functional description of the PAL logic function. This symbol makes a convenient reference when selecting the PAL that best fits a specific application. Figure 18 shows the logic symbol for a PAL10H8 gate array.

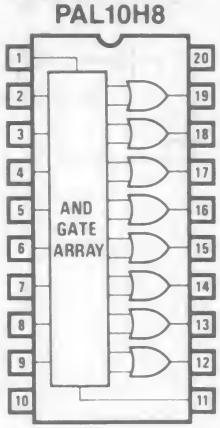


Figure 18

A PAL Example

As an example of how the PAL enables the designer to reduce costs and simplify logic design, consider the design of a simple, high volume consumer product: an electronic dice game. This type of product will be produced in extremely high volume, so it is essential that every possible production cost be minimized.

The electronic dice game is simply constructed using a free running oscillator whose output is used to drive two asynchronous modulo six counters. When the user "rolls" the dice (presses a button), the current state of the counters is decoded and latched into a display resembling the pattern seen on an ordinary pair of dice.

A conventional logic diagram for the dice game is shown in Figure 16. (A detailed logic derivation is shown in the PAL applications section of this handbook). It is implemented using standard TTL, SSI and MSI parts, with a total I.C. count of eight: six quad gate packages and two quad D-latches. Looks like a nice, clean logic design, right? Wrong!!

PAL Goes to the Casino

A brief examination of Figure 16 reveals two basic facts: first, the circuit contains mostly simple, combinatorial logic, and second, it uses a clocked state transition sequence. Remembering that the PAL family contains ample provision for these features, the PAL catalog is consulted. The PAL16R8 has all the required functions, and the entire logic content of the circuit can be programmed into a single PAL shown in Figure 19.

In this example, the PAL effected an eight to one package count reduction and a significant cost savings. This is typical of the power and cost effective performance that the PAL family brings to logic design.

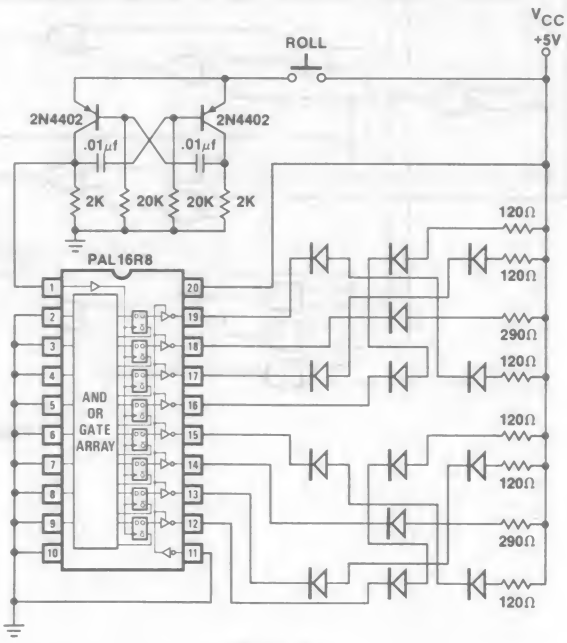
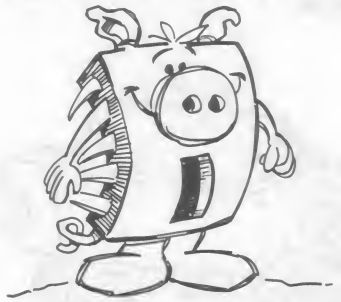


Figure 19

Advantages of Using PALs



The PAL has a unique place in the world of logic design. Not only does it offer many advantages over conventional logic, it also provides many features not found anywhere else. The PAL family:

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by at least 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin and 24-pin Skinny DIP packages.
- High speed: 15ns typical propagation delay.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature eliminates possibility of copying by competitors.

All of these features combine together to lower product development costs and increase product cost effectiveness. The bottom line is that PAL units save money.

Direct Logic Replacement

In both new and existing designs the PAL can be used to replace various logic functions. This allows the designer to optimize a circuit in many ways never before possible. The PAL is particularly effective when used to provide interfaces required by many LSI functions. PAL flexibility combined with LSI function density makes a powerful team.

Design Flexibility

The PAL offers the systems logic designer a whole new world of options. Until now, the decision on logic system implementation was usually between SSI/MSI logic functions on one hand and microprocessors on the other. In many cases the function required is too awkward to implement the first way and too simple to justify the second. Now the PAL offers the designer high functional density, high speed, and low cost. Even better, PAL devices come in a variety of sizes and functions, thereby further increasing the designer's options.

Space Efficiency

By allowing designers to replace many simple logic functions with single packages, the PAL allows more compact P.C. board layouts. The PAL space saving 20-pin and 24-pin "SKINNYDIP" helps to further reduce board area while simplifying board layout and fabrication. This means that many multi-card systems can now be reduced to one or two cards, and that can make the difference between a profitable success or an expensive disaster.

Smaller Inventory

The PAL family can be used to replace up to 90% of the conventional TTL family with just 29 parts. This considerably lowers both shelving and inventory cataloging requirements. Even better, small custom modifications to the standard functions are easy for PAL users, not so easy for standard TTL users.

High Speed

The PAL family runs faster or equal to the best of bipolar logic circuits. This makes the PAL the ideal choice for most logical operations or control sequence which requires a medium complexity and high speed. Also, in many microcomputer systems, the PAL can be used to handle high speed data interfaces that are not feasible for the microprocessor alone. This can be used to significantly extend the capabilities of the low-cost, low-speed NMOS microprocessors into areas formerly requiring high-cost bipolar microprocessors.

Easy Programming

The members of the PAL family can be quickly and easily programmed using standard PROM programmers. This allows designers to use PALs with a minimum investment in special equipment. Many types of programmable logic, such as the FPLA, require an expensive, dedicated programmer.

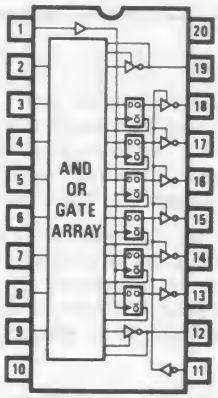
Secure Data

The PAL verification logic can be completely disabled by blowing out a special "last link." This prevents the unauthorized copying of valuable data, and makes the PAL perfect for use in any application where data integrity must be carefully guarded.

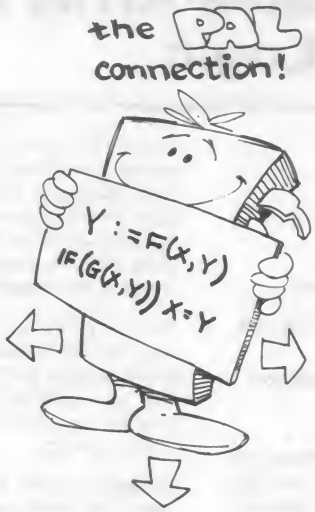
Summary

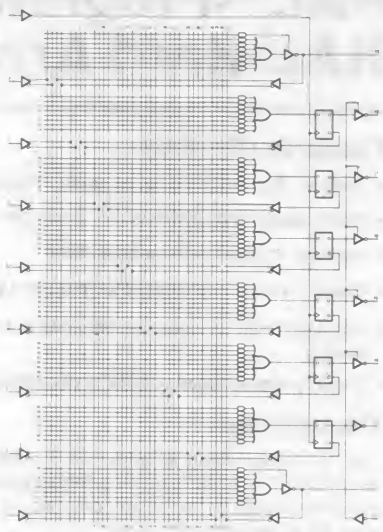
The 29 member PAL family of logic devices offer logic designers new options in the implementation of sequential and combinatorial logic designs. The family is fast, compact, flexible, and easy to use in both new and existing designs. It promises to reduce costs in most areas of design and production with a corresponding increase in product profitability.

A Great Performer!

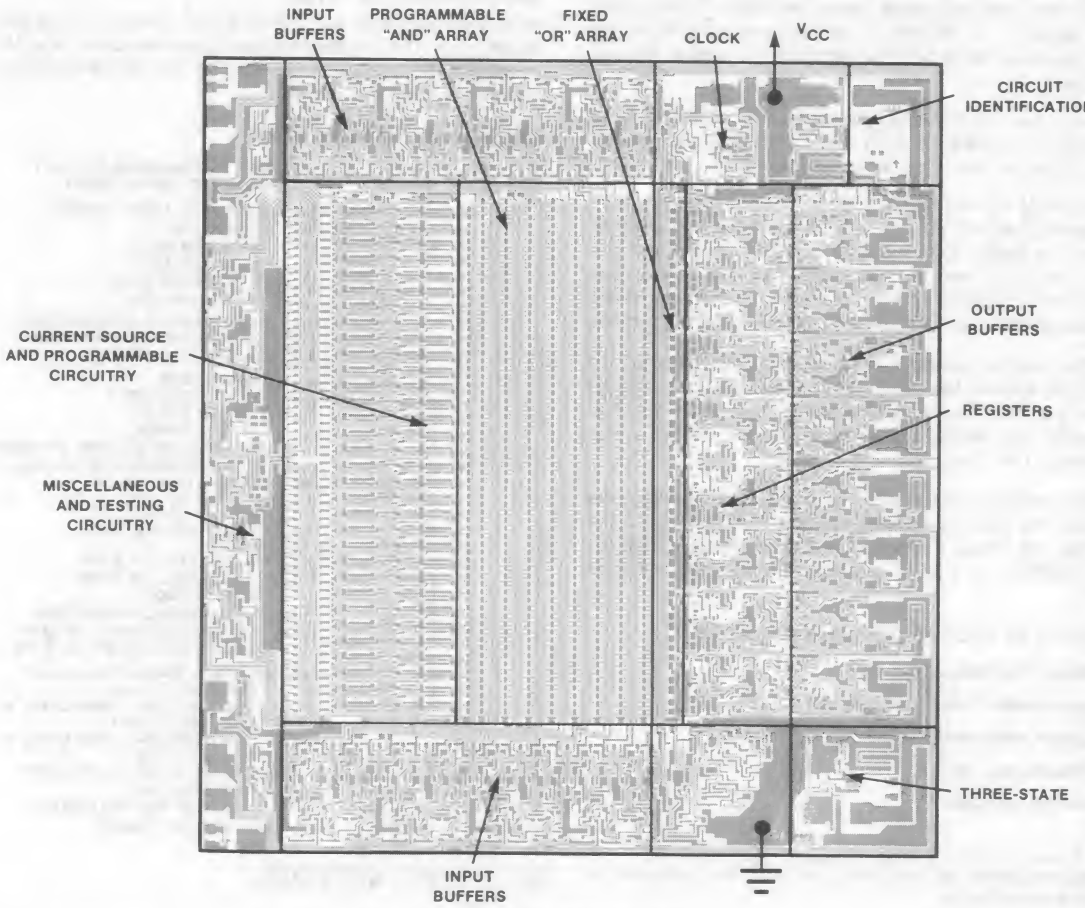


PAL16R6 Logic Symbols





PAL16R6 Logic Diagram



PAL 16R6 Metalization

7

PAL®-Programmable Array Logic
HAL®-Hard Array Logic

Features/Benefits

- **Reduces SSI/MSI chip count greater than 5 to 1**
- **Saves space with SKINNYDIP® packages**
- **Reduces IC inventories substantially**
- **Expedites and simplifies prototyping and board layout**
- **PALASM™ silicon compiler provides auto routing and test vectors**
- **Security fuse reduces possibility of copying by competitors**

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The HAL family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

There are four different speed/power families offered. Choose from either the standard, high speed, half power, or quarter power family to maximize design performance.

The PAL/HAL lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

The HAL transfer function is the familiar sum of products. Like the ROM, the HAL has a single array of selectable gates. Unlike the ROM, the HAL is a selectable AND array driving a fixed OR array (the ROM is a fixed AND array driving a selectable OR array).

In addition the PAL/HAL provides these options:

- **Variable input/output pin ratio**
- **Programmable three-state outputs**
- **Registers with feedback**
- **Arithmetic capability**
- **Exclusive-OR gates**

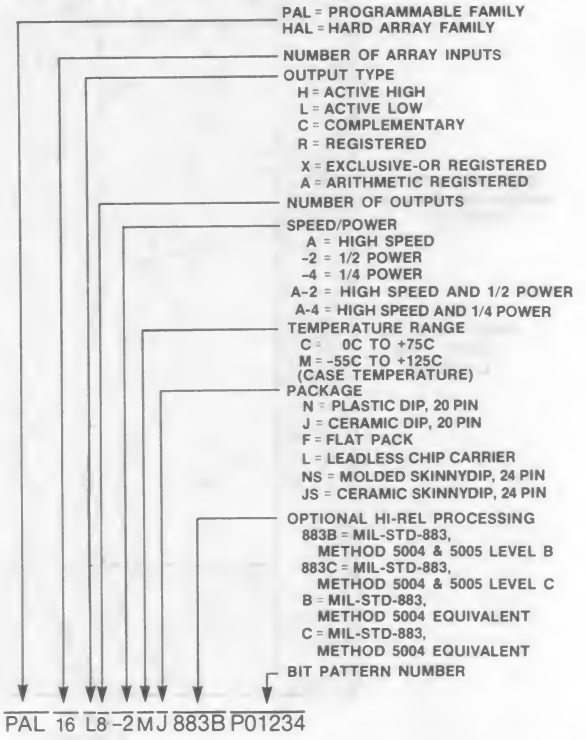
Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

To design a HAL, the user first programs and debugs a PAL using PALASM and the "PAL DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, e.g., P01234.

Monolithic Memories will provide a PAL sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 P01234. See Ordering Information below.

Ordering Information

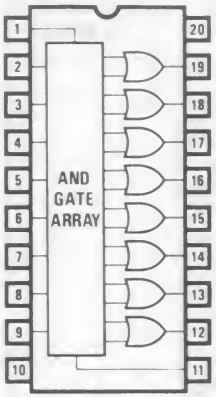


Monolithic Memories

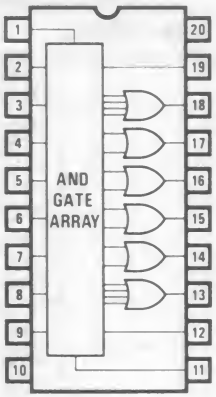
GENERIC LOGIC	PINS	PACKAGE	DESCRIPTION	PART NUMBER			
				STANDARD	HIGH SPEED		1/4 POWER
10H8	20	N, J, F, L	Octal 10 Input And-Or Gate Array	PAL10H8 HAL10H8		PAL10H8-2 HAL10H8-2	
12H6	20	N, J, F, L	Hex 12 Input And-Or Gate Array	PAL12H6 HAL12H6		PAL12H6-2 HAL12H6-2	
14H4	20	N, J, F, L	Quad 14 Input And-Or Gate Array	PAL14H4 HAL14H4		PAL14H4-2 HAL14H4-2	
16H2	20	N, J, F, L	Dual 16 Input And-Or Gate Array	PAL16H2 HAL16H2		PAL16H2-2 HAL16H2-2	
16C1	20	N, J, F, L	16 Input And-Or/And-Or-Invert Gate Array	PAL16C1 HAL16C1		PAL16C1-2 PAL16C1-2	
10L8	20	N, J, F, L	Octal 10 Input And-Or-Invert Gate Array	PAL10L8 HAL10L8		PAL10L8-2 HAL10L8-2	
12L6	20	N, J, F, L	Hex 12 Input And-Or-Invert Gate Array	PAL12L6 HAL12L6		PAL12L6-2 HAL12L6-2	
14L4	20	N, J, F, L	Quad 14 Input And-Or-Invert Gate Array	PAL14L4 HAL14L4		PAL14L4-2 HAL14L4-2	
16L2	20	N, J, F, L	Dual 16 Input And-Or-Invert Gate Array	PAL16L2 HAL16L2		PAL16L2-2 HAL16L2-2	
16L8	20	N, J, F, L	Octal 16 Input And-Or-Invert Gate Array	PAL16L8 *HAL16L8	PAL16L8A HAL16L8A	PAL16L8A-2 HAL16L8A-2	PAL16L8A-4 HAL16L8A-4
16R8	20	N, J, F, L	Octal 16 Input Registered And-Or Gate Array	PAL16R8 *HAL16R8	PAL16R8A HAL16R8A	PAL16R8A-2 HAL16R8A-2	PAL16R8A-4 HAL16R8A-4
16R6	20	N, J, F, L	Hex 16 Input Registered And-Or Gate Array	PAL16R6 *HAL16R6	PAL16R6A HAL16R6A	PAL16R6A-2 HAL16R6A-2	PAL16R6A-4 HAL16R6A-4
16R4	20	N, J, F, L	Quad 16 Input Registered And-Or Gate Array	PAL16R4 *HAL16R4	PAL16R4A HAL16R4A	PAL16R4A-2 HAL16R4A-2	PAL16R4A-4 HAL16R4A-4
16X4	20	N, J, F, L	Quad 16 Input Registered And-Or-Xor Gate Array	PAL16X4 HAL16X4			
16A4	20	N, J, F, L	Quad 16 Input Registered And-Carry-Or-Xor Gate Array	PAL16A4 HAL16A4			
12L10	24 (28)	NS,JS,F (L)	Deca 12 Input And-Or-Invert Gate Array	PAL12L10 HAL12L10			
14L8	24 (28)	NS,JS,F (L)	Octal 14 Input And-Or-Invert Gate Array	PAL14L8 HAL14L8			
16L6	24 (28)	NS,JS,F (L)	Hex 16 Input And-Or-Invert Gate Array	PAL16L6 HAL16L6			
18L4	24 (28)	NS,JS,F (L)	Quad 18 Input And-Or-Invert Gate Array	PAL18L4 HAL18L4			
20L2	24 (28)	NS,JS,F (L)	Dual 20 Input And-Or-Invert Gate Array	PAL20L2 HAL20L2			
20C1	24 (28)	NS,JS,F (L)	20 Input And-Or/And-Or Invert Gate Array	PAL20C1 HAL20C1			
20L10	24 (28)	NS,JS,F (L)	Deca 20 Input And-Or-Invert Gate Array	PAL20L10 HAL20L10			
20X10	24 (28)	NS,JS,F (L)	Deca 20 Input Registered And-Or-Xor Gate Array	PAL20X10 HAL20X10			
20X8	24 (28)	NS,JS,F (L)	Octal 20 Input Registered And-Or-Xor Gate Array	PAL20X8 HAL20X8			
20X4	24 (28)	NS,JS,F (L)	Quad 20 Input Registered And-Or-Xor Gate Array	PAL20X4 HAL20X4			
20L8	24 (28)	NS,JS,F (L)	Octal 20 Input And-Or-Invert Gate Array		PAL20L8A HAL20L8A		
20R8	24 (28)	NS,JS,F (L)	Octal 20 Input Registered And-Or Gate Array		PAL20R8A HAL20R8A		
20R6	24 (28)	NS,JS,F (L)	Hex 20 Input Registered And-Or Gate Array		PAL20R6A HAL20R6A		
20R4	24 (28)	NS,JS,F (L)	Quad 20 Input Registered And-Or Gate Array		PAL20R4A HAL20R4A		

HAL available in "W" package. ( ) = Military Product Standard.

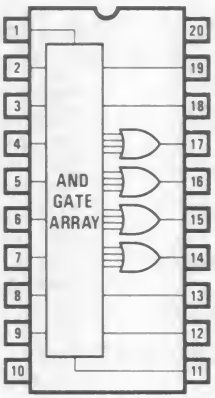
10H8



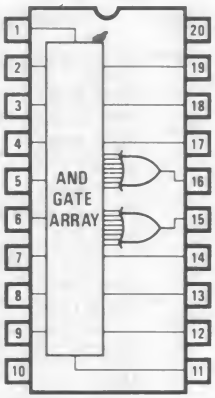
12H6



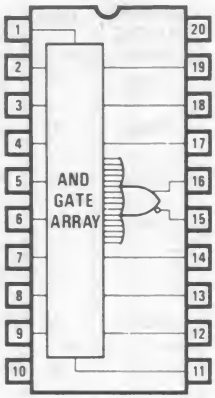
14H4



16H2



16C1



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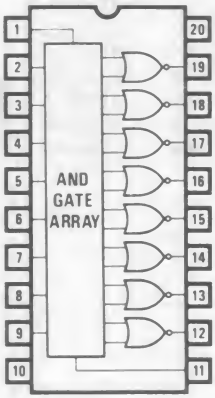

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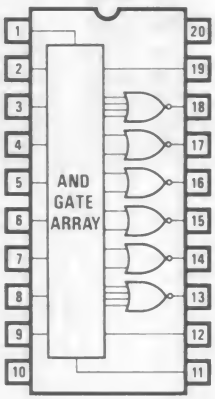

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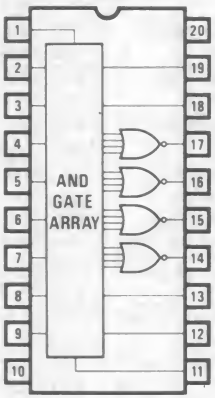

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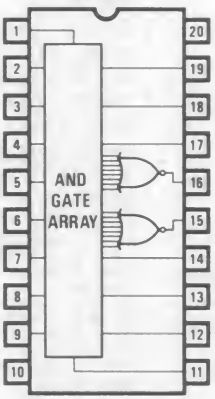

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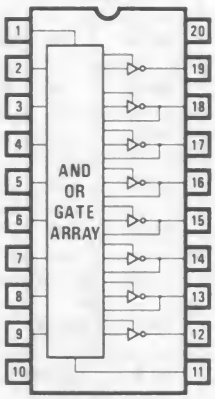

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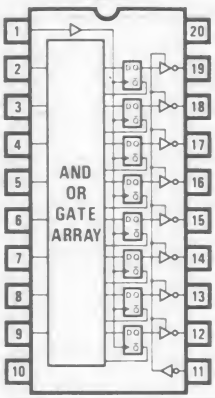

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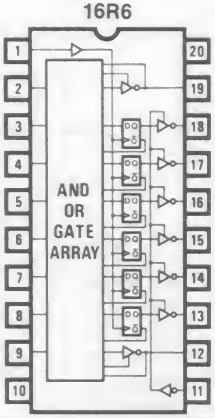

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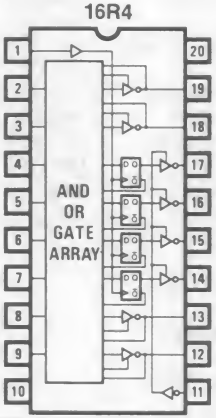

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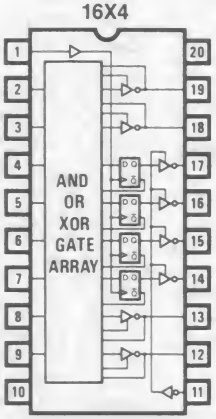
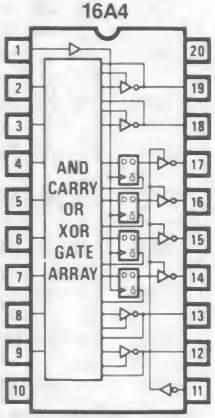
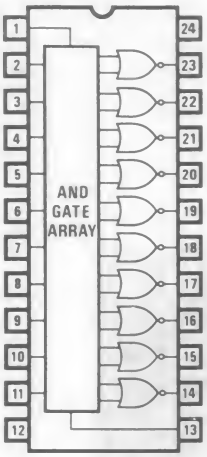


16A4



12L10



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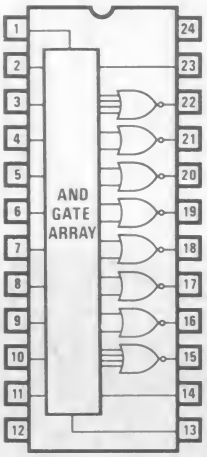
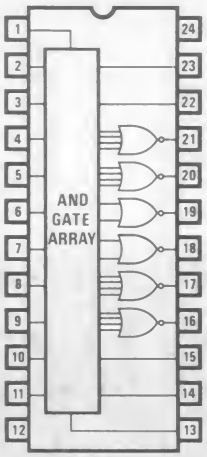


16L6



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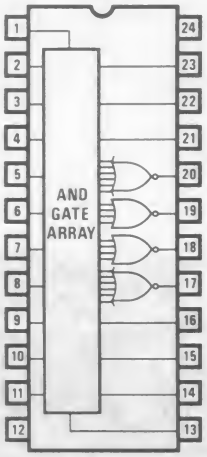

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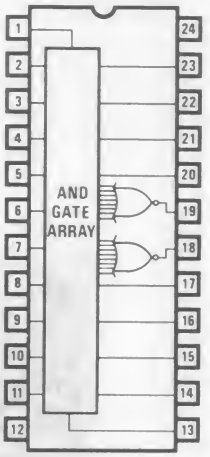

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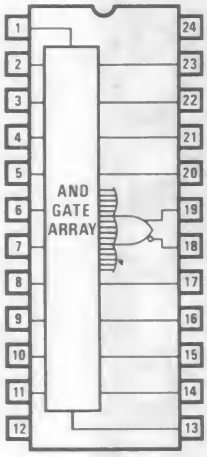

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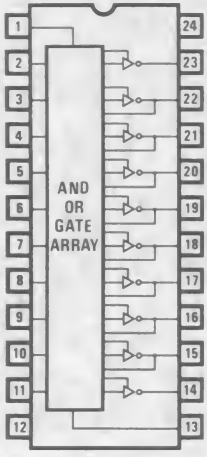

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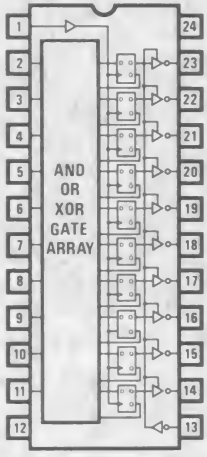

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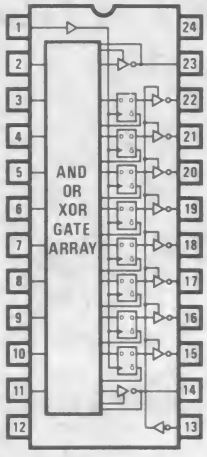

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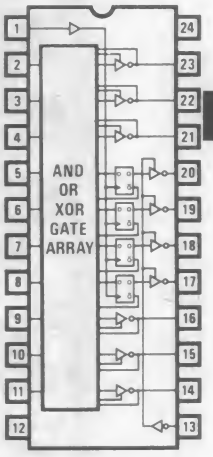

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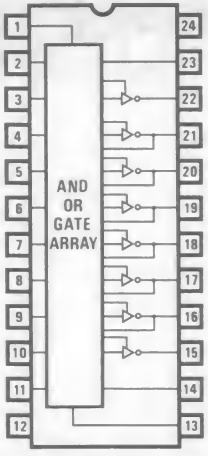
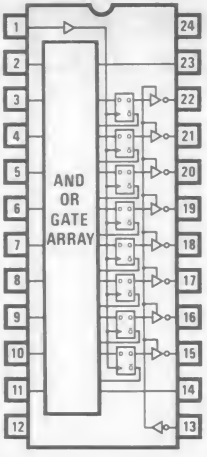
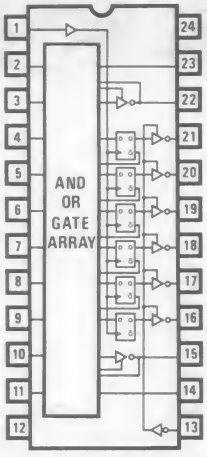


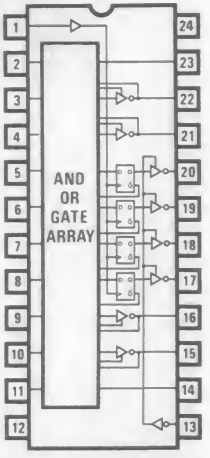
20R8

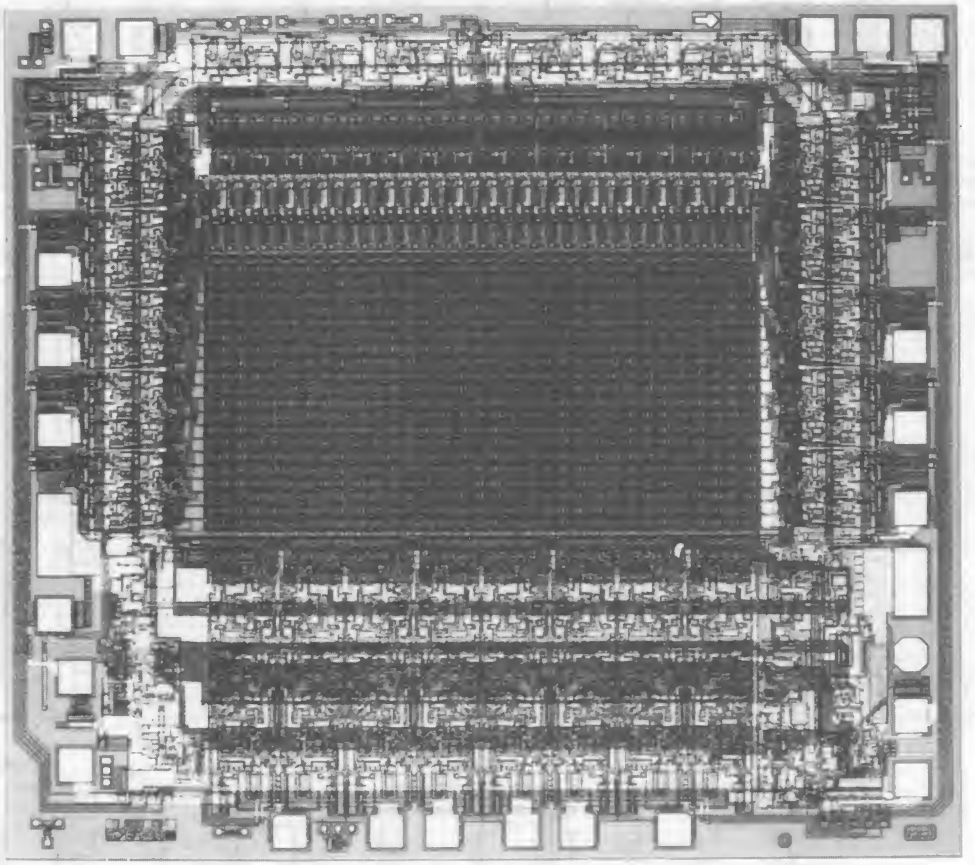


20R6



20R4



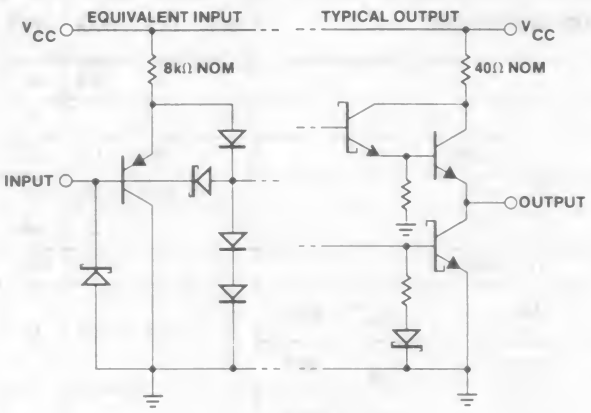


Absolute Maximum Ratings

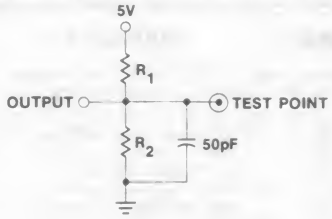
	Operating	Programming
Supply Voltage, V_{CC}	-0.5 to 7.0V	-0.5 to 12.0V
Input Voltage	-1.5 to 5.5V	-1.0 to 22V ⊕
Off-state output Voltage	5.5V	12.0V
Storage temperature		-65° to +150°C

⊕ Pins 1 and 11 may be raised to 20V

Schematic of Inputs and Outputs



Test Load



Other loads may be used.

7

Typical notes for all the following specifications (pages 7-22 — 7-30)

Notes: Apply to electrical and switching characteristics

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}.

* These are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

* * Only one output shorted at a time.

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				55	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	Except 16C1	R1 = 560Ω R2 = 1.1kΩ		25	45		25	35	ns
		16C1			25	45		25	40	

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R1 = 560Ω R2 = 1.1kΩ		25	45		25	40	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R8 16R6 16R4	45	25		35	25		ns
		16X4 16A4	55	30		45	30		
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4 16R6 16R8 16L8			120	180	mA
			16X4			160	225	
			16A4			170	240	

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6 16R4 16L8	R_1 = 200Ω, R_2 = 390Ω		25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8				15	25		15	25	ns
t_{PZX}	Input to output enable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
t_{PXZ}	Input to output disable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14	25		16	25		MHz
		16X4 16A4		12	22		14	22		

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		
t_{su}	Set up time from input or feedback to clock		60	38		50	38		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	20X10	20X8 20X4		120	180	mA
I_{CC}	Supply current	V_{CC} = MAX	20L10			90	165	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	R_1 = 200Ω, R_2 = 390Ω		35	60		35	50	ns
t_{CLK}	Clock to output or feedback			20	35		20	30	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L10			20	45		20	35	ns
t_{PZX}	Input to output enable except 20X10			35	55		35	45	ns
t_{PXZ}	Input to output disable except 20X10			35	55		35	45	ns
f_{MAX}	Maximum frequency		10.5	16		12.5	16		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Set up time from input or feedback to clock	16R8A 16R6A 16R4A	30	15		25†	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

†Can select 20ns upon customer request.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6A 16R4A 16L8A	R_1 = 200Ω, R_2 = 390Ω		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8A				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	16R6A 16R4A 16L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	16R6A 16R4A 16L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	16R8A 16R6A 16R4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	7		15	7		ns
		High	20	7		15	7		
t_{su}	Set up time from input or feedback to clock	20R8A 20R6A 20R4A	30	15		25	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−90	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				160	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	20R6A 20R4A 20L8A	R_1 = 200Ω, R_2 = 390Ω		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 13 to output enable except 20L8A				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	20R6A 20R4A 20L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	20R6A 20R4A 20L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	20R8A 20R6A 20R4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 4mA		0.3	0.5	V
			COM	I_{OL} = 4mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −1mA	2.4	2.8		V
			COM	I_{OH} = −1mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				30	45	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R1 = 1.12kΩ R2 = 2.2kΩ		45	80		45	60	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R6A-2 16R4A-2 16R8A-2	50	25		35	25		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16L8A-2 16R6A-2 16R4A-2	R_1 = 200Ω, R_2 = 390Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable except 16L8A-2				15	25		15	25	ns
t_{PZX}	Input to output enable	16L8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable	16R8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency	16R8A-2 16R6A-2 16R4A-2		14	25		16	25		MHz

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Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R8A-4 16R6A-4 16R4A-4	Low	40	20		30	20		ns
			High	40	20		30	20		
t_{su}	Set up time from input or feedback to clock	16R8A-4 16R6A-4 16R4A-4		90	45		60	45		ns
t_h	Hold time			0	−15		0	−15		ns
T_A	Operating free-air temperature			−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 4mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −1mA	2.4	2.8		V
			COM	I_{OH} = −1mA				
I_{OZL}	Output short-circuit current**	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4A-4 16R6A-4 16R8A-4 16L8A-4			30	50	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6A-4 16R4A-4 16L8A-4	R_1 = 800Ω, R_2 = 1.56kΩ		35	75		35	55	ns
t_{CLK}	Clock to output or feedback				20	45		20	35	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable — except 16L8A-4				15	40		15	30	ns
t_{PZX}	Input to output enable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
t_{PXZ}	Input to output disable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
f_{MAX}	Maximum frequency	16R8A-4 16R6A-4 16R4A-4		8	18		11	18		MHz

Programming/Verifying Procedure

NOTES: For programming purposes many PAL pins have double functions.

For The PAL 20:

As long as Pin 1 is at HH, Pin 11 is at ground, and Pin 12 is either at HH or Z (as defined in Table 1) — Pins 16, 17, 18, and 19 are outputs. The other pin functions are: I0 (Pin 2) through I7 (Pin 9) plus Pin 12 address the proper row; A0 (Pin 15), A1 (Pin 14), and A2 (Pin 13) address the proper product lines.

When Pin 11 is at HH, Pin 1 is at ground and Pin 19 is either at HH or Z — Pins 12, 13, 14, and 15 are outputs. The other pin functions are: I0 (Pin 2) through I7 (Pin 9) plus Pin 19 address the proper row; A0 (now Pin 18), A1 (now Pin 17), and A2 (now Pin 16) address the proper product lines.

For The PAL 24:

As long as Pin 1 is at HH, Pin 13 is at ground and Pin 14 is either at HH or Z (as defined in Table 1) — Pins 19, 20, 21, 22, and 23 are outputs. The other pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 14 address the proper row; A0 (Pin 15), A1 (Pin 16), and A2 (Pin 17) address the proper product lines.

As long as Pin 13 is at HH, Pin 1 is at ground, and Pin 23 is either at HH or Z (as defined in Table 1) — Pins 14, 15, 16, 17, and 18 are outputs. The other pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 23 address the proper row; A0 (Pin 22), A1 (Pin 21), and A2 (Pin 20) address the proper product lines.

For The PAL 24A:

As long as Pin 1 is at HH, Pin 13 is at ground, and Pin 14 is either at HH or Z (as defined in Table 1) — Pins 19, 20, 21, and 22 are outputs. The other pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 14 address the proper row; A0 (Pin 15), A1 (Pin 16), and A2 (Pin 17) address the proper product lines.

As long as Pin 13 is at HH, Pin 1 is at ground, and Pin 23 is either at HH or Z (as defined in Table 1) — pins 15, 16, 17, and 18 are outputs. The other Pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 23 address the proper row; A0 (Pin 22), A1 (Pin 21), and A2 (Pin 20) address the proper product lines.

Pre-Verification

5.1.1 Raise V_{CC} to 5.0 volts.

5.1.2 Raise Output Disable pin, OD, to VIHH.

5.1.3 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.1.4 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.1.5 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the state corresponding to an unblown fuse.

— For verified unblown condition, continue procedure from 5.1.3 through 5.1.5.

— For verified blown condition, stop procedure and reject part.

Programming Algorithm

5.2.1 Raise Output Disable pin, OD, to VIHH

5.2.2 Programming pass. For all fuses to be blown:

5.2.2.1 Lower CLOCK pin to ground.

5.2.2.2 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.2.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.2.4 Raise V_{CC} to VIHH.

5.2.2.5 Program the fuse by pulsing the output pins of the selected product group -one at a time- to VIHH (as shown in the Programming Waveforms, Section 5.5).

5.2.2.6 Lower V_{CC} to 5.0 volts.

5.2.2.7 Repeat this procedure from 5.2.2.2 until pattern is complete.

5.2.3 First verification pass. For all fuse locations:

5.2.3.1 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.3.2 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.3.3 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.

— For verified output state, continue procedure

— For overblow condition, stop procedure and reject part.

— For underblow condition, reexecute steps 5.2.2.4 through 5.2.2.6 and 5.2.2.3. If successful, continue procedure. After three attempts to blow fuse without success, reject part but continue procedure.

5.2.3.4 Repeat this procedure from 5.2.3.1 until the entire array is exercised.

5.2.4 High Voltage Verify. For all fuse locations:

5.2.4.1 Raise V_{CC} to 5.5 volts.

5.2.4.2 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.4.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.4.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.

— For verified output state, continue procedure

— For invalid output state, stop procedure and reject part.

5.2.4.5 Repeat this procedure from 5.2.4.1 until the entire array is exercised.

5.2.5 Low Voltage Verify. For all fuse locations:

5.2.5.1 Lower V_{CC} to 4.5 volts.

5.2.5.2 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.5.3 Select a product line by specifying A0, A1, and A2, one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.5.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.

— For verified output state, continue procedure.

— For invalid output state, continue procedure and reject part.

Programming the Security Fuses

5.3.1 Verify per Section 5.2.4 and 5.2.5.

5.3.2 Raise V_{CC} to 6 volts.

5.3.3 For PAL 20:

— Program the first fuse by pulsing Pin 1 to VP. (From 1 to 5 pulses is acceptable.)

— Program the second fuse by pulsing Pin 11 to VP. (From 1 to 5 pulses is acceptable.)

5.3.4 For PAL 24 and PAL 24A:

— Program the first fuse by pulsing Pin 1 to VP. (From 1 to 5 pulses is acceptable.)

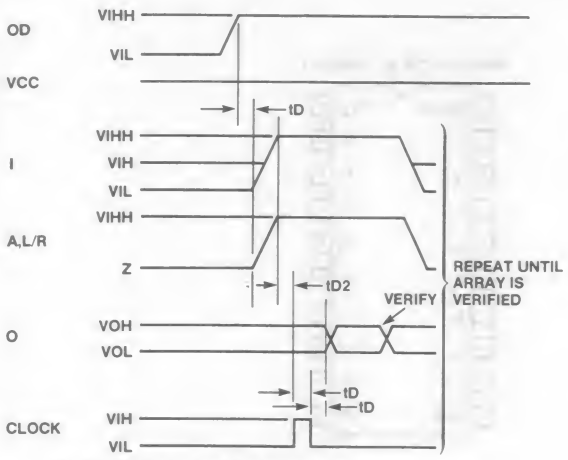
— Program the second fuse by pulsing Pin 13 to VP. (From 1 to 5 pulses is acceptable.)

5.3.5 Verify per Section 5.2.4 and 5.2.5:

— A device is "secure" if either half fails to verify.

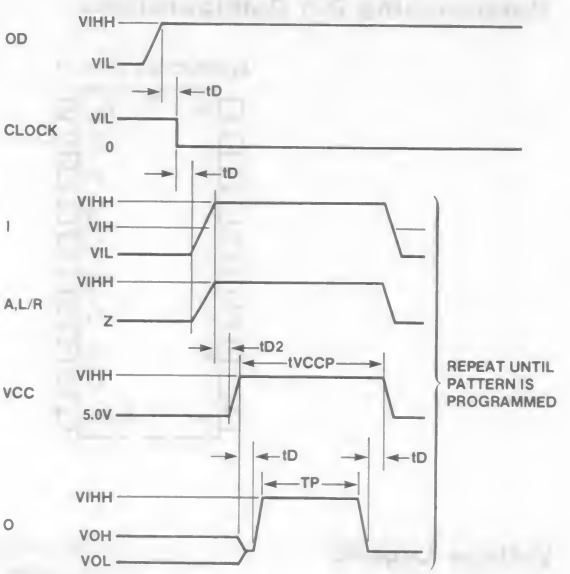
5.4 Programming Parameters

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11.5	11.75	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			50	
		All other inputs			10	
I_{CCH}	Program Supply Current				900	mA
t_{VCCP}	Pulse Width of V_{CC} @ V_{IHH}				60	µS
T_P	Program Pulse Width		10	20	50	µS
t_D	Delay Time		100			ns
t_{D2}	Delay Time after L/R Pin		10			µS
	V_{CCP} Duty Cycle				20	%
V_P	Security Fuse Programming Voltage		18	18.5	19	V
I_P	Security Fuse Programming Supply Current				400	mA
T_{PP}	Security Fuse Programming Pulse Width		10	40	70	µS
	Security Fuse Programming Duty Cycle				50	%
t_{RP}	Rise time of output programming and address pulses		1	1.5	10	V/µS
t_{RP}	Rise Time of security fuse programming pulses		1	1.5	10	V/µS
V_{CCPP}	V_{CC} value during security fuse programming		5.75	6.0	6.25	V
	V_{CC} value for first verify		4.75	5.0	5.25	
	V_{CC} value for High V_{CC} verify		5.4	5.5	5.6	
	V_{CC} value for Low V_{CC} verify		4.4	4.5	4.6	

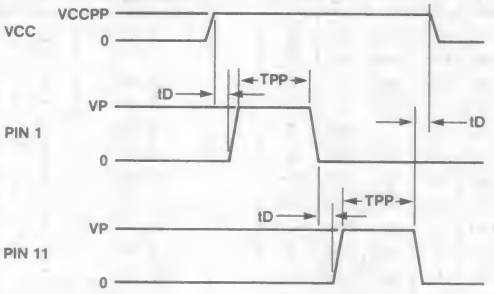


NOTE: VCC (Low Voltage Verify) = 4.5 volts
VCC (High Voltage Verify) = 5.5 volts
VCC (First Verify) = 5.0 volts
A Delay (tD2) must always precede the Positive Clock Transition. (e.g see section 5.2.3.3 for underblow condition)

5.5 ARRAY PROGRAMMING



5.6 SECURITY FUSE PROGRAMMING



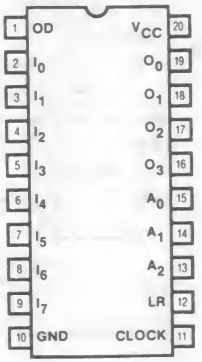
Programmer/Development Systems

VENDOR	PAL 20s (ALL)	PAL 24s (STD)	PAL 24s (FAST)
Data I/O	— LogicPak (Rev-010) — 1427 Card Set	LogicPak (Rev-010)	— LogicPak (Rev-010)
Structured Design	— SD 20/24 — PAL Burner *	— SD 20/24 — PAL Burner *	— SD 20/24 — PAL Burner *
STAG	— PM202 (Rev 3) — PM2200 *	— PM202 (Rev 3) — PM2200 *	— PM202 (Rev) — PM2200 *
DIGELEC	— UP803 (FAM51) or (FAM52)	— UP803 (FAM51) or (FAM52)	— UP803 (FAM51) or (FAM52)
PROLOG	— M980 PM9068		
KONTRON	— MPP80S MOD 21		

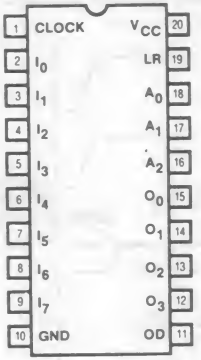
*Means that this version is being qualified.

Programming Pin Configurations

PRODUCTS 0 THRU 31



PRODUCTS 32 THRU 63



Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

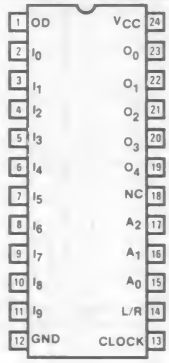
Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

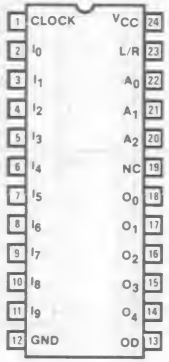
Table 2 Product Line Select

Programming Pin Configurations

PRODUCTS 0 THRU 39



PRODUCTS 40 THRU 79



Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g. 10K Ω to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION										
	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

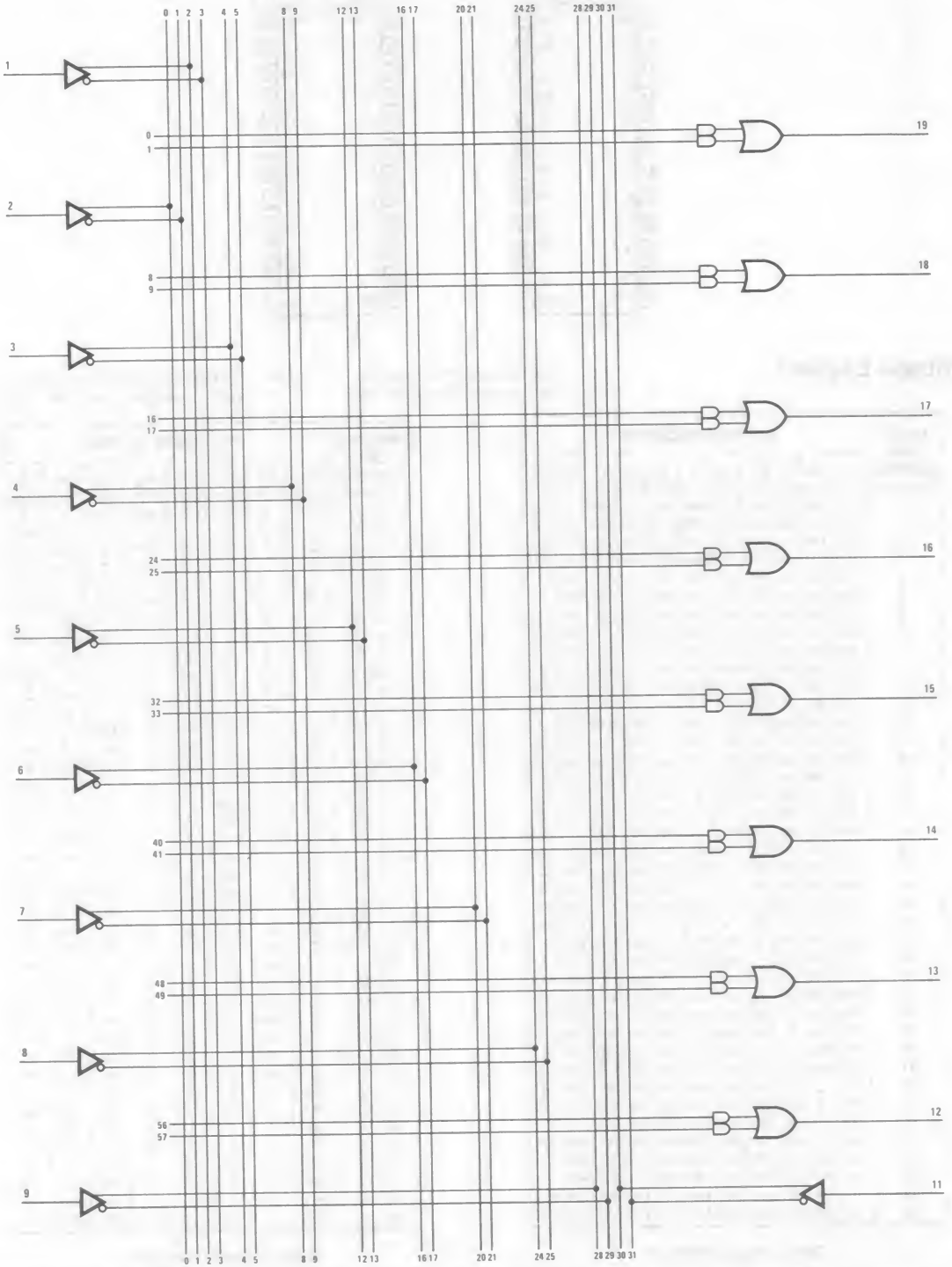
Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

7

10H8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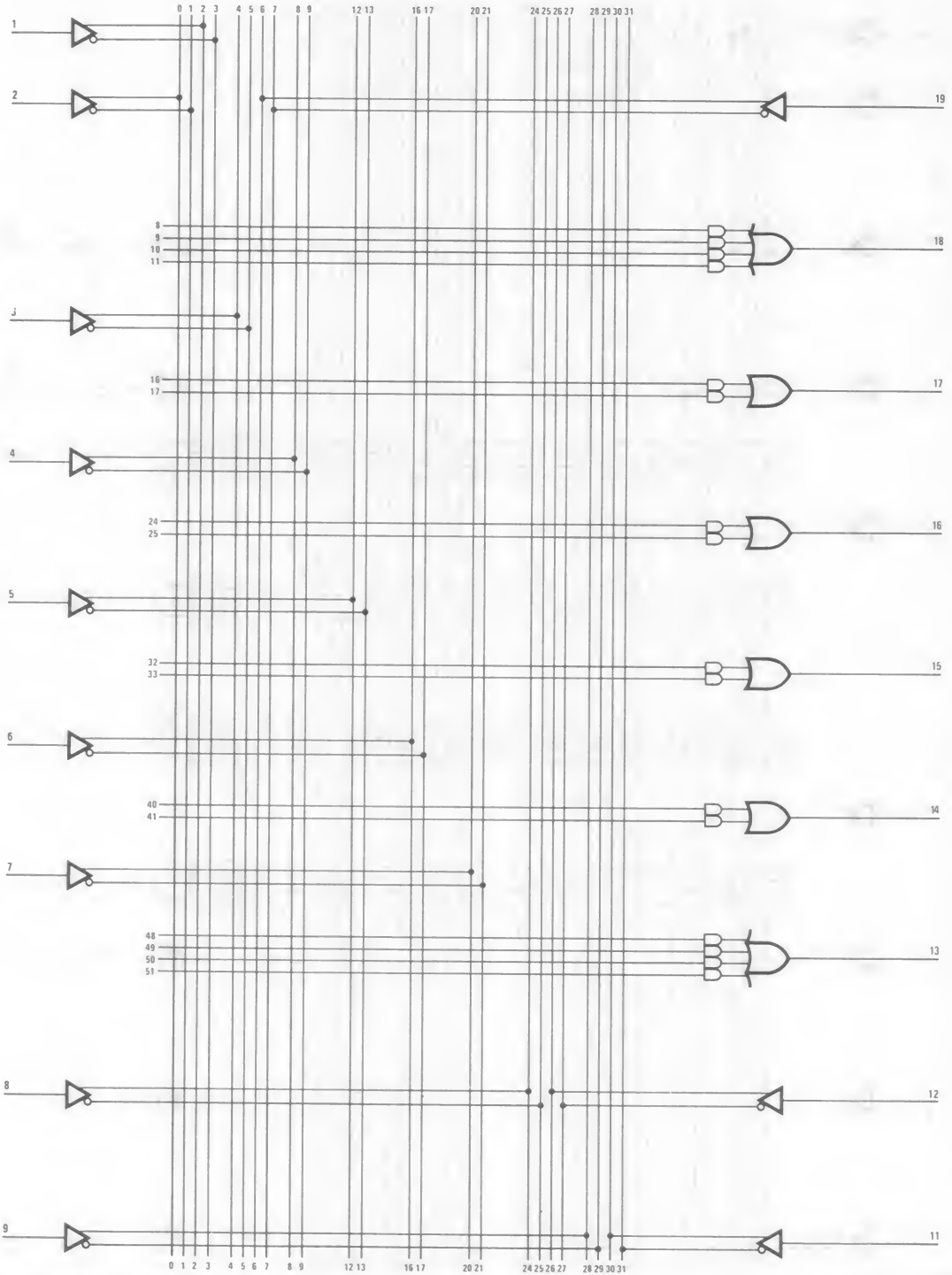
12H6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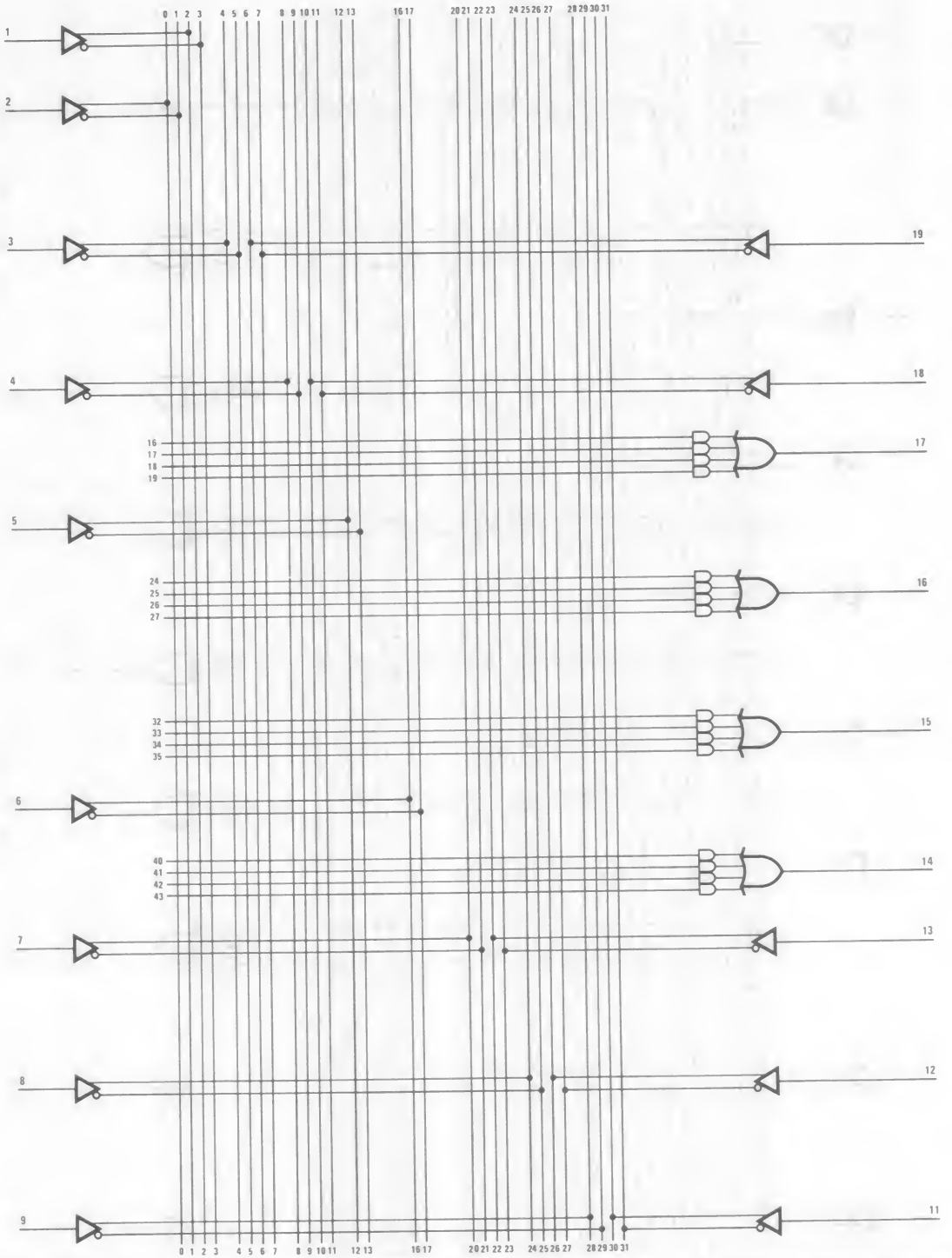
14H4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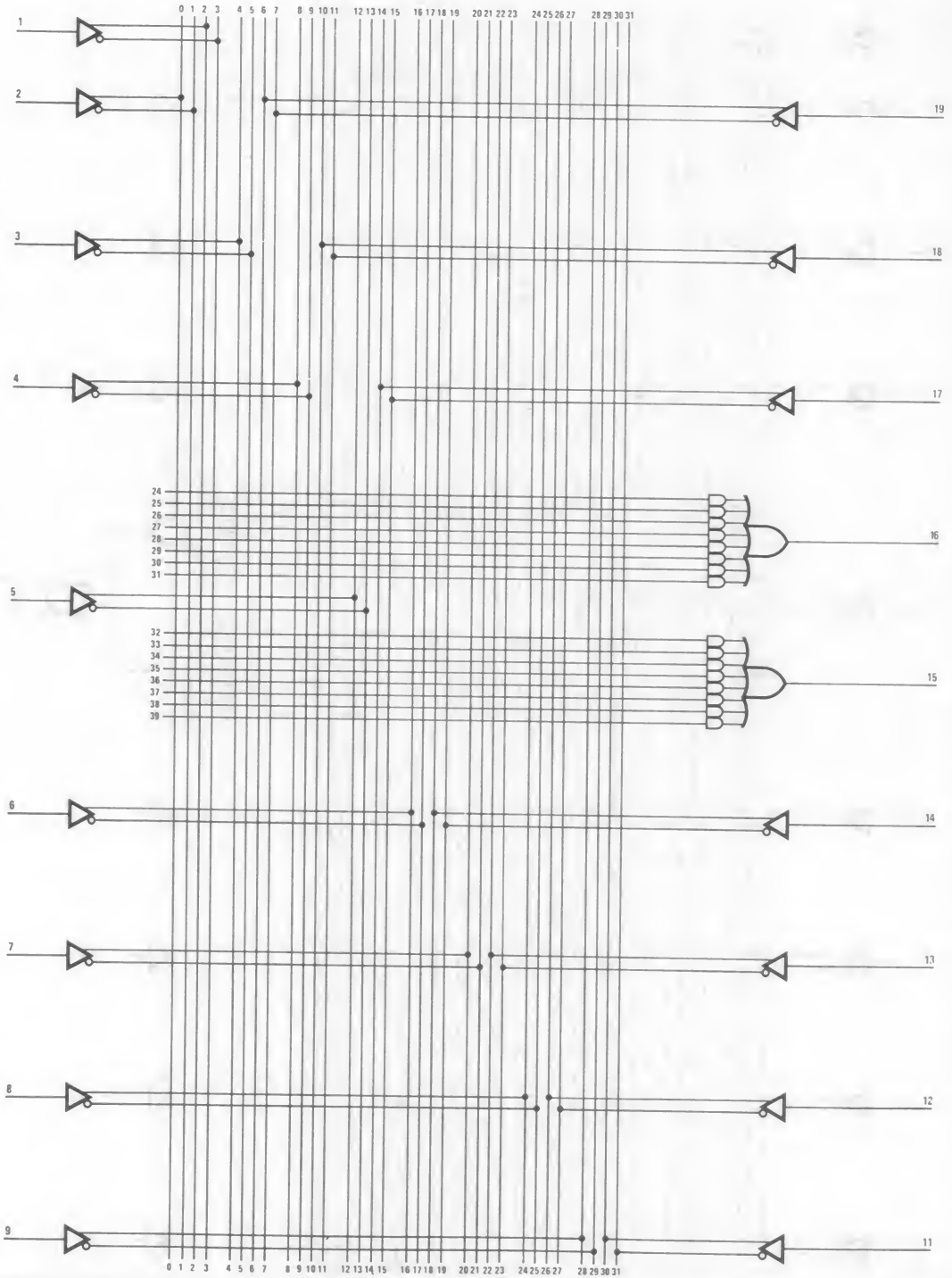
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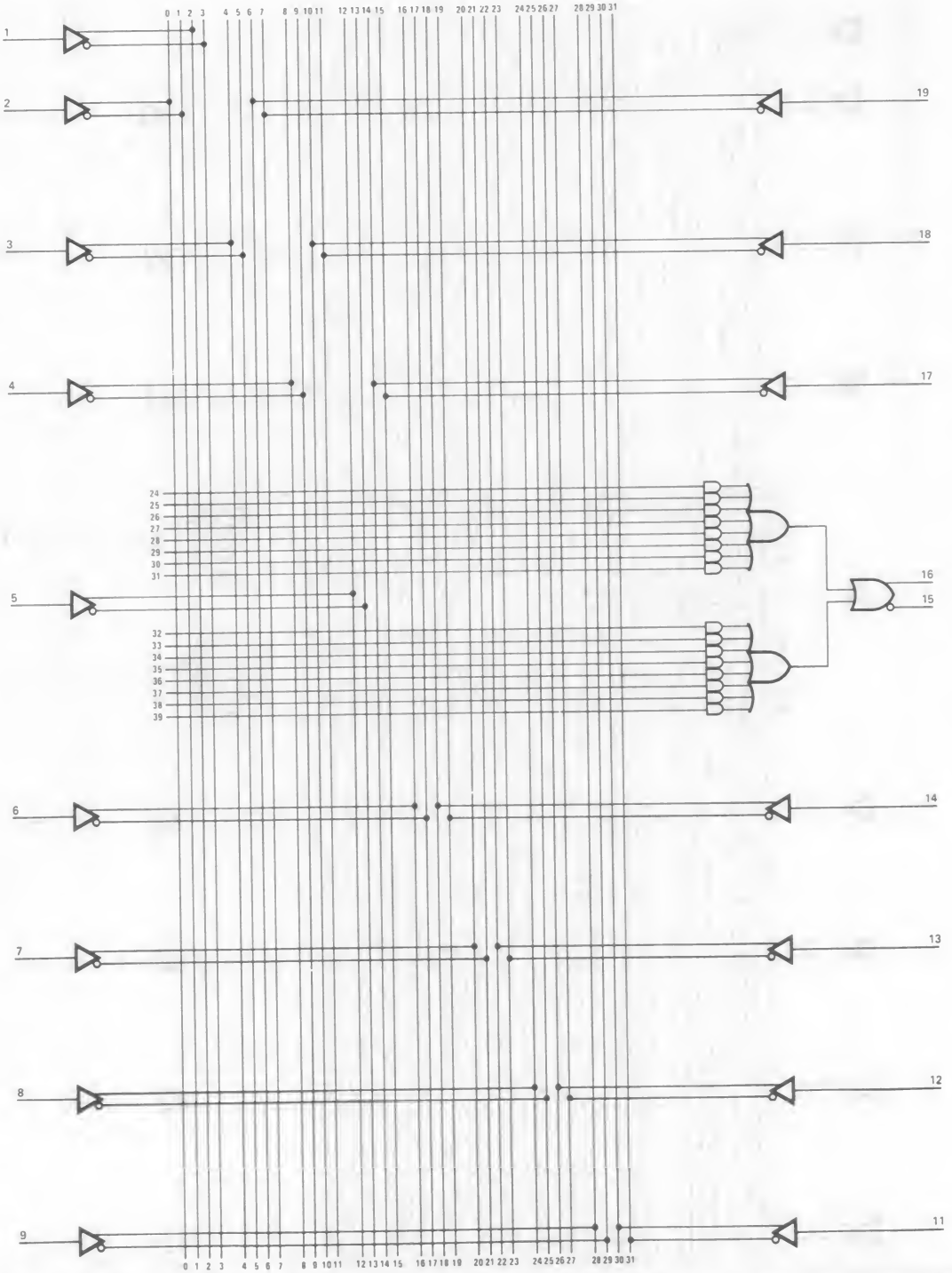
16C1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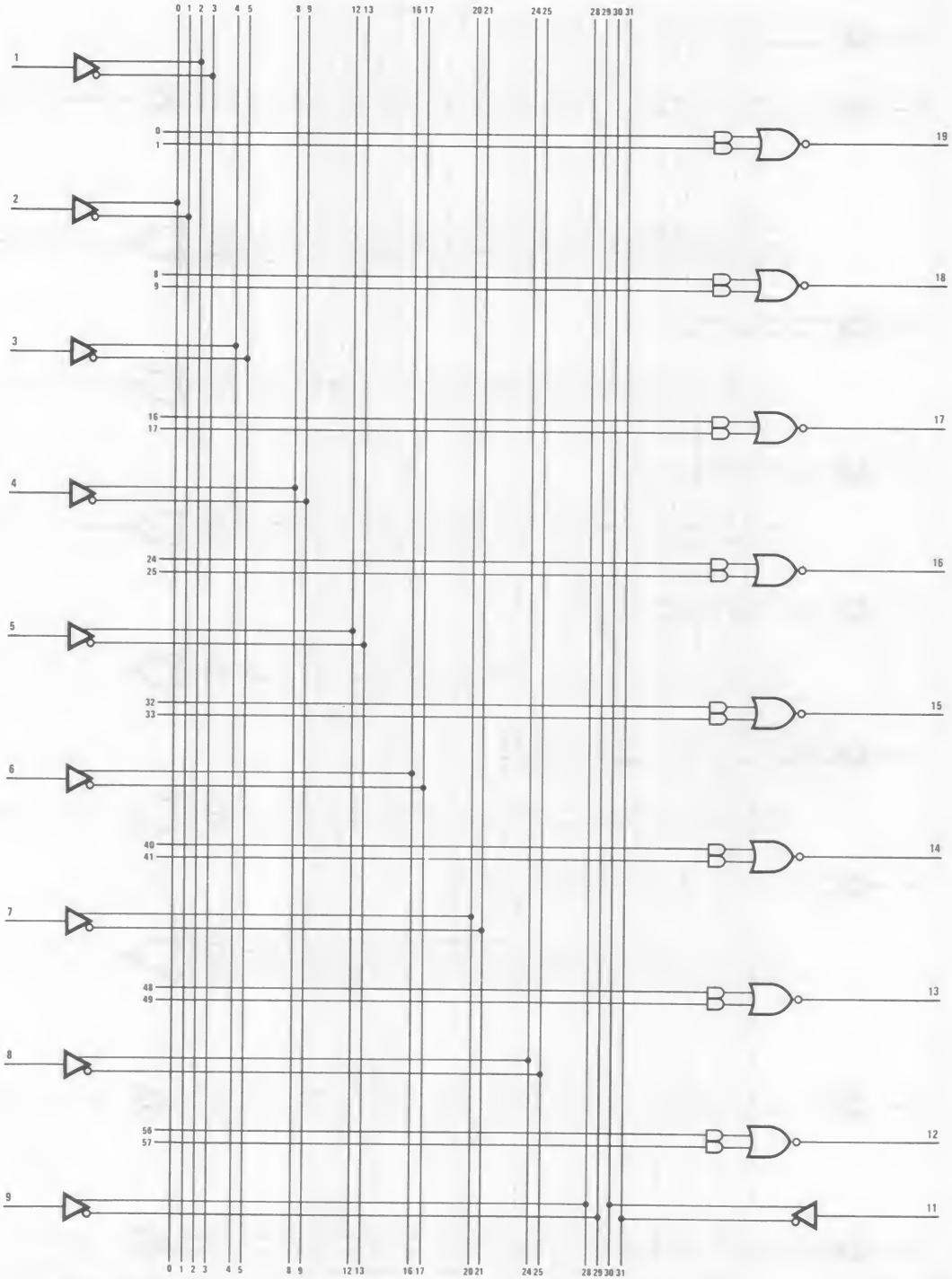
10L8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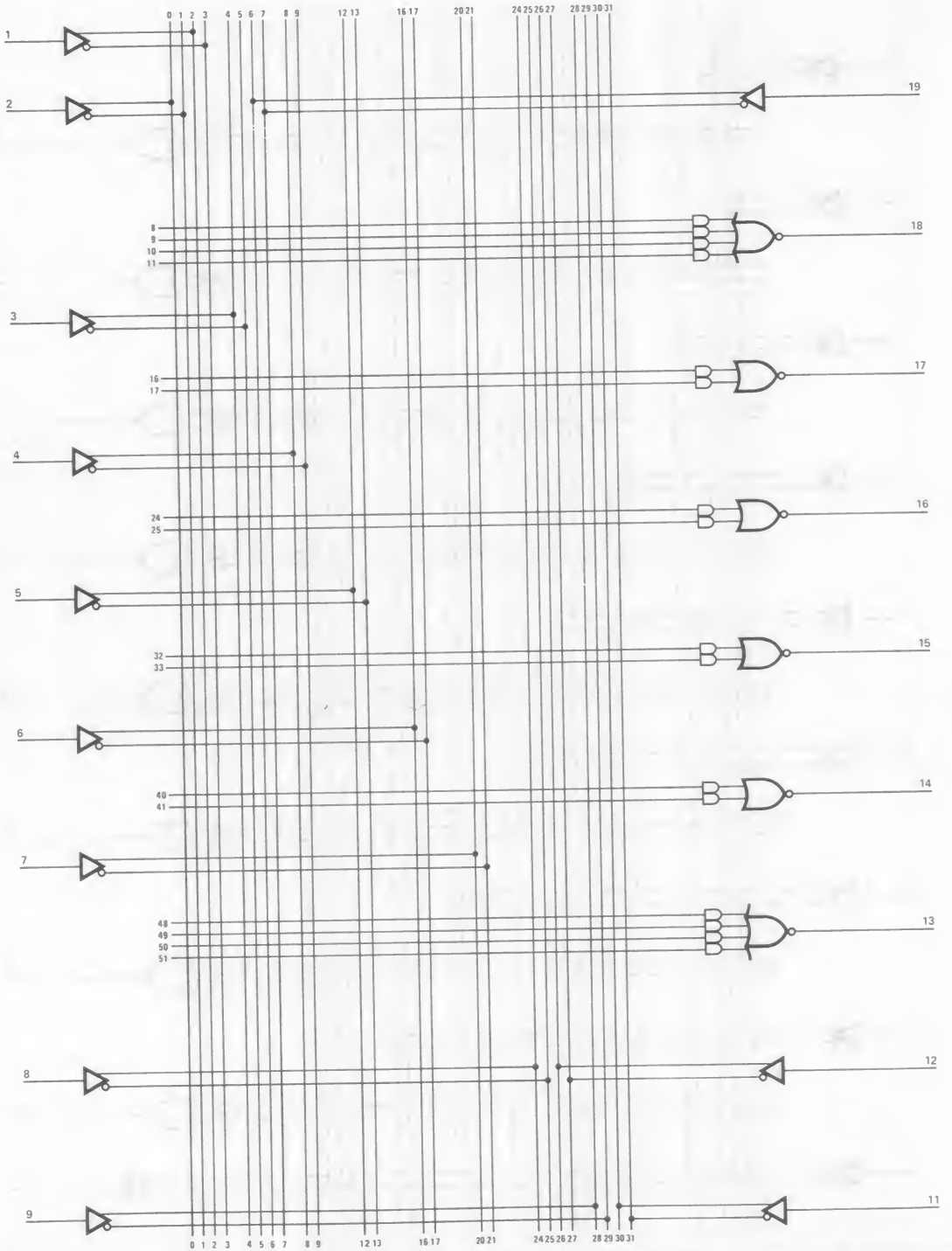
12L6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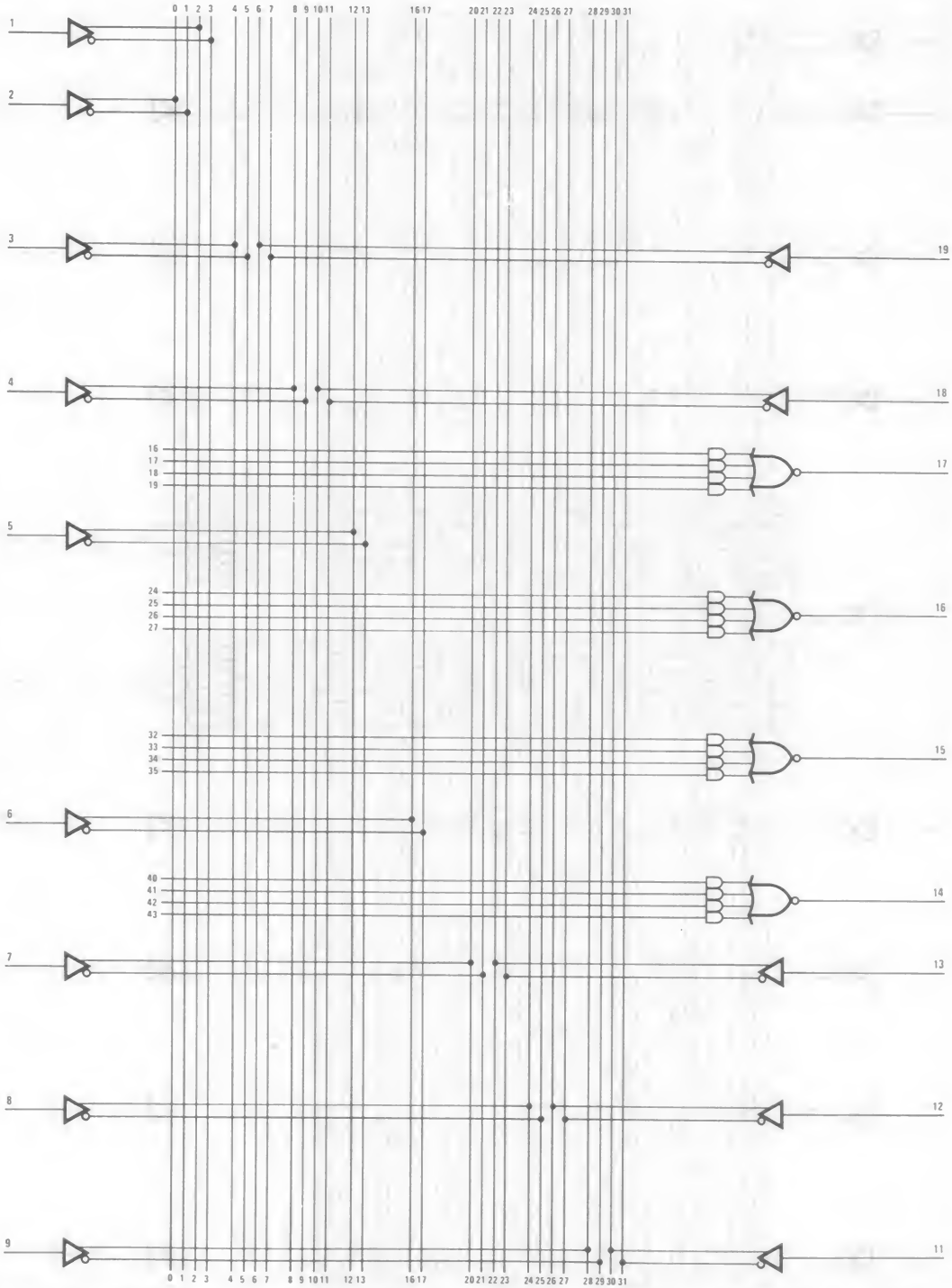
14L4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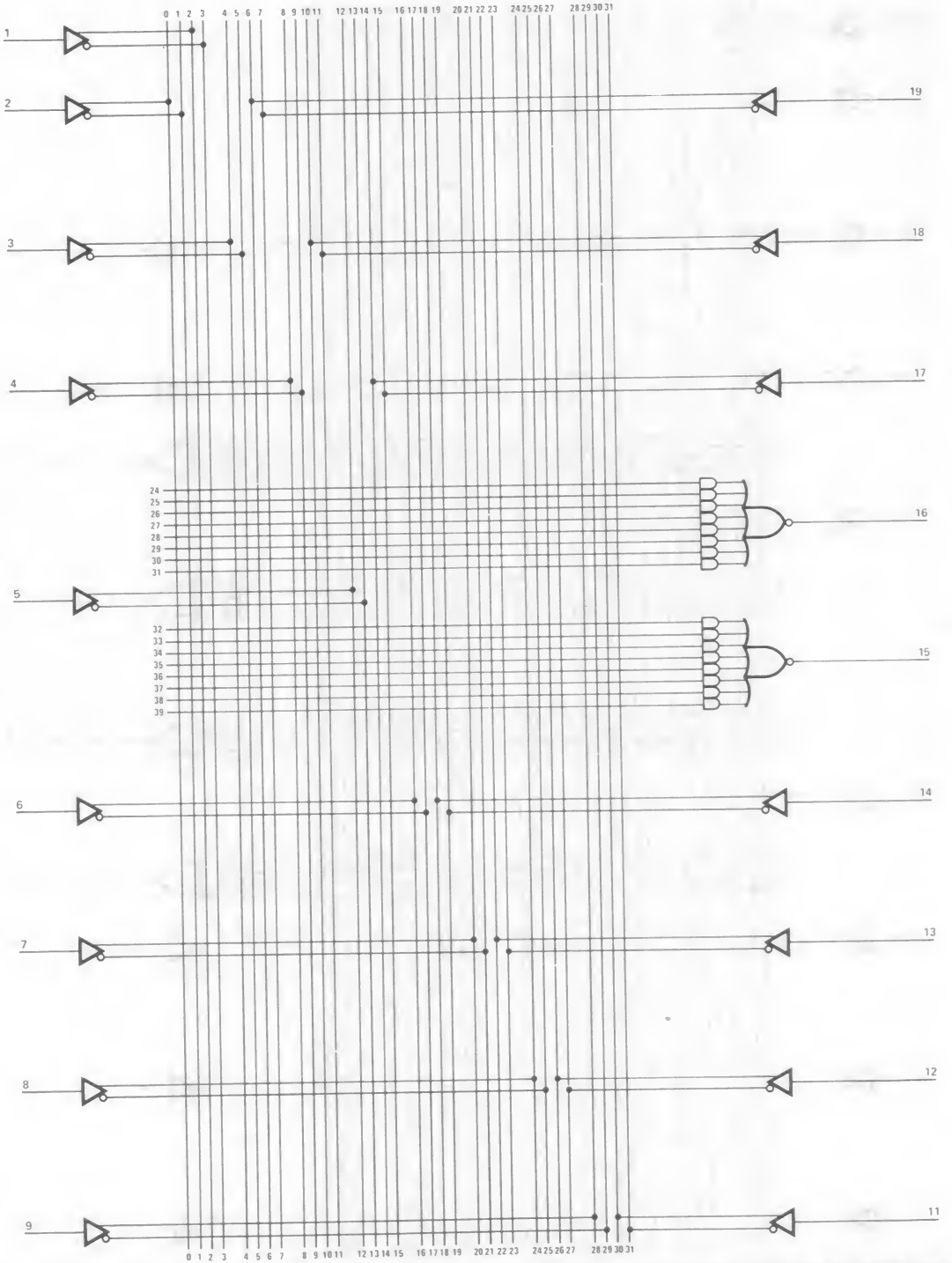
16L2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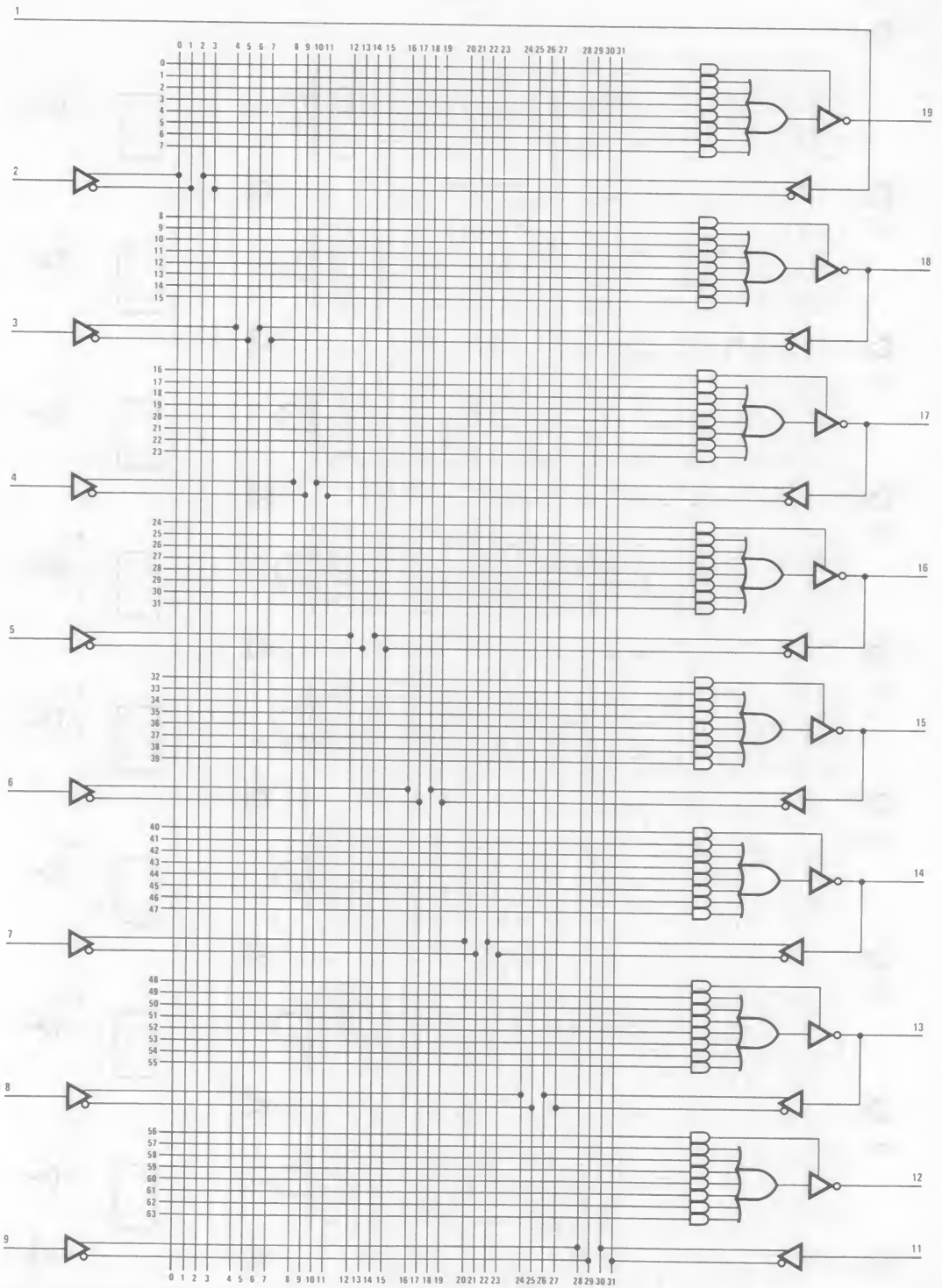
16L8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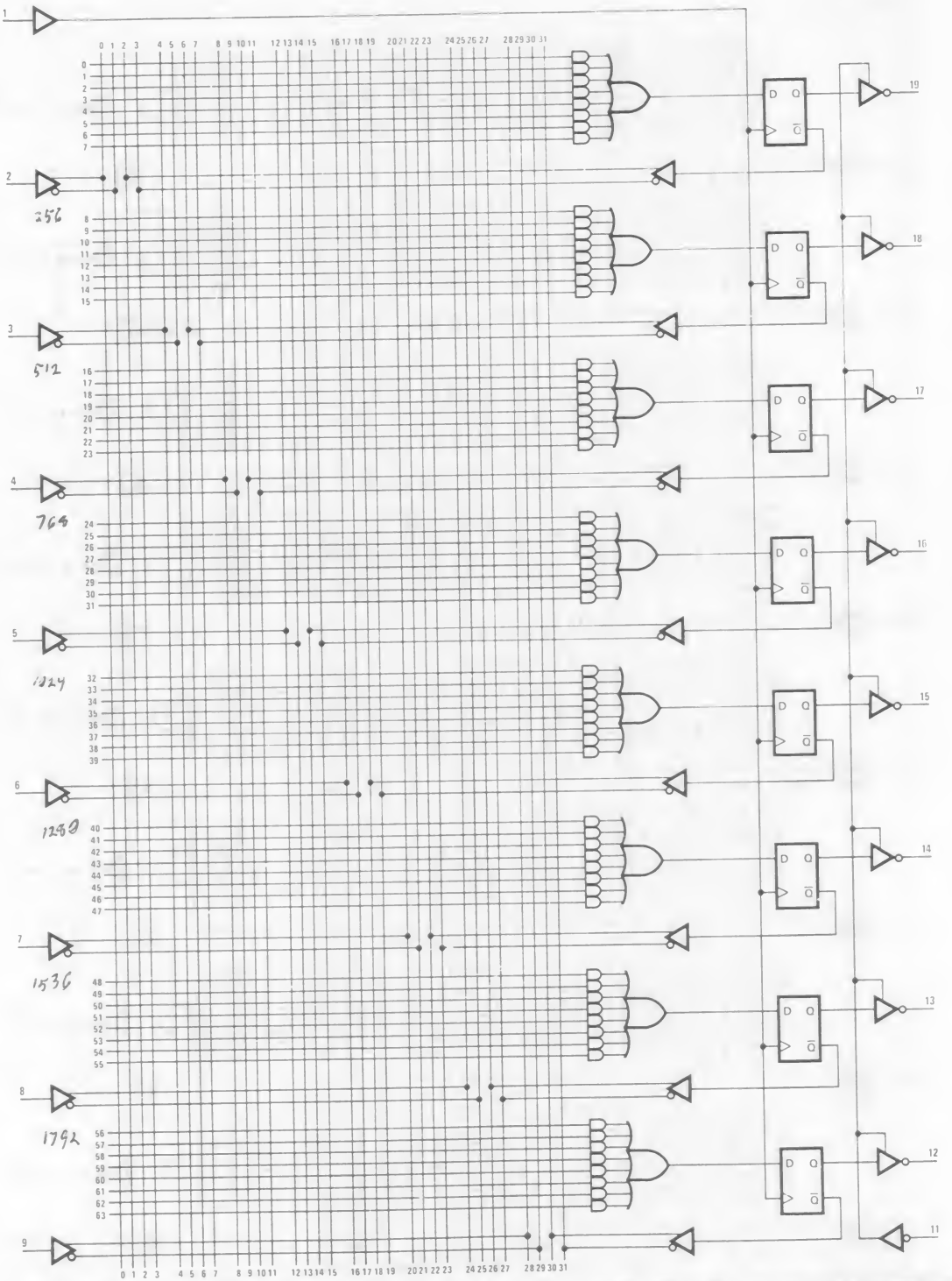
16R8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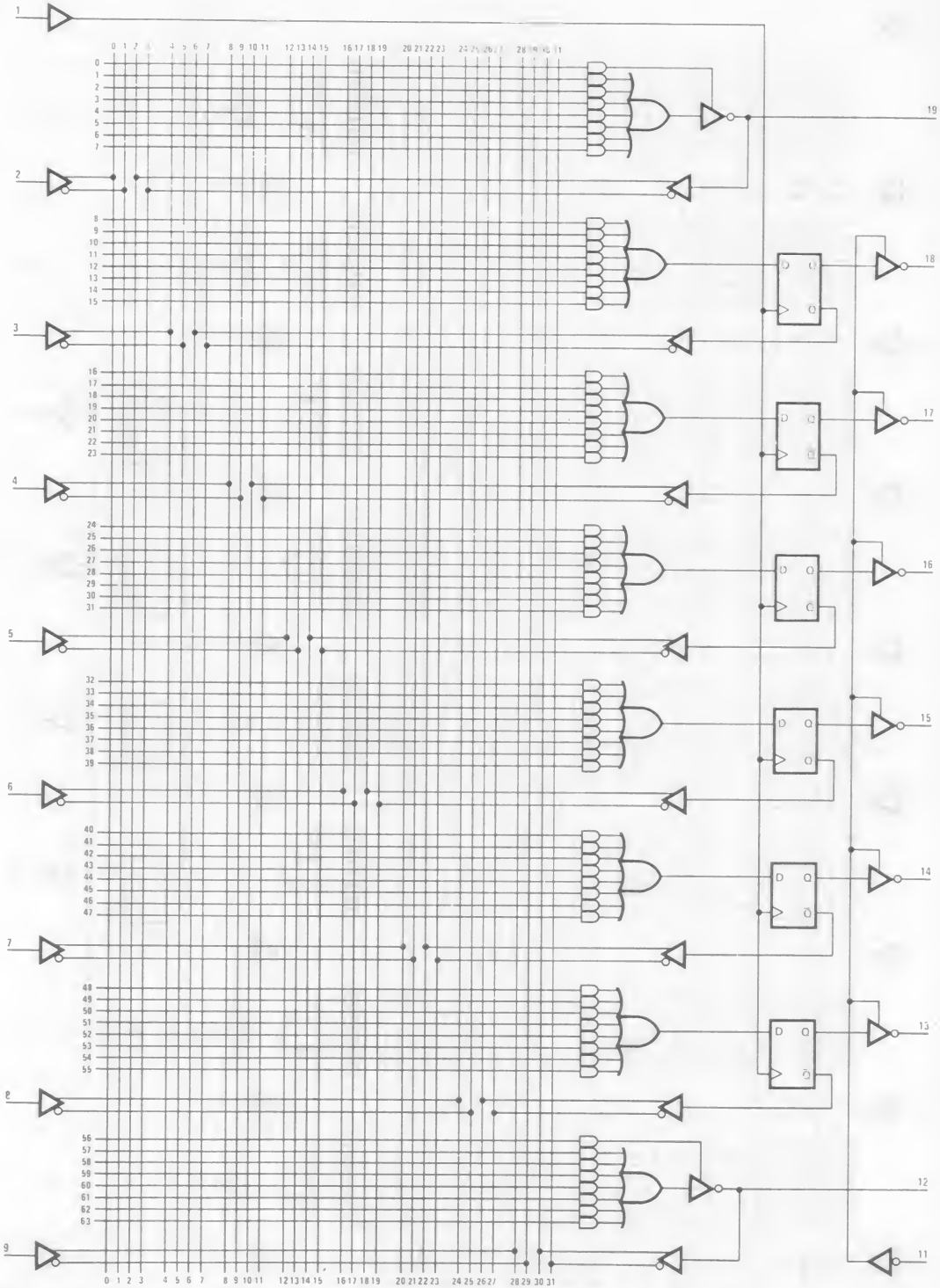
16R6



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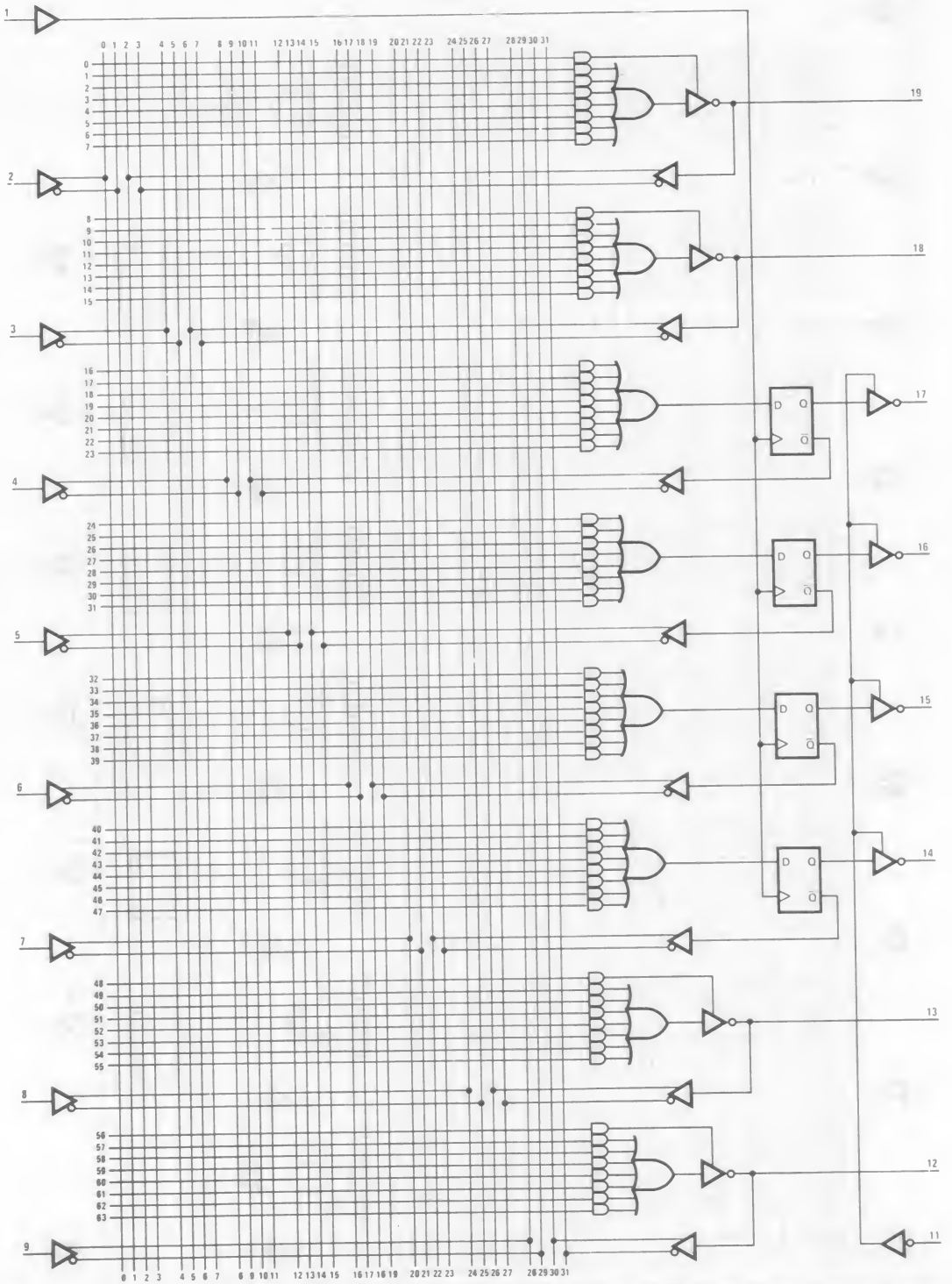

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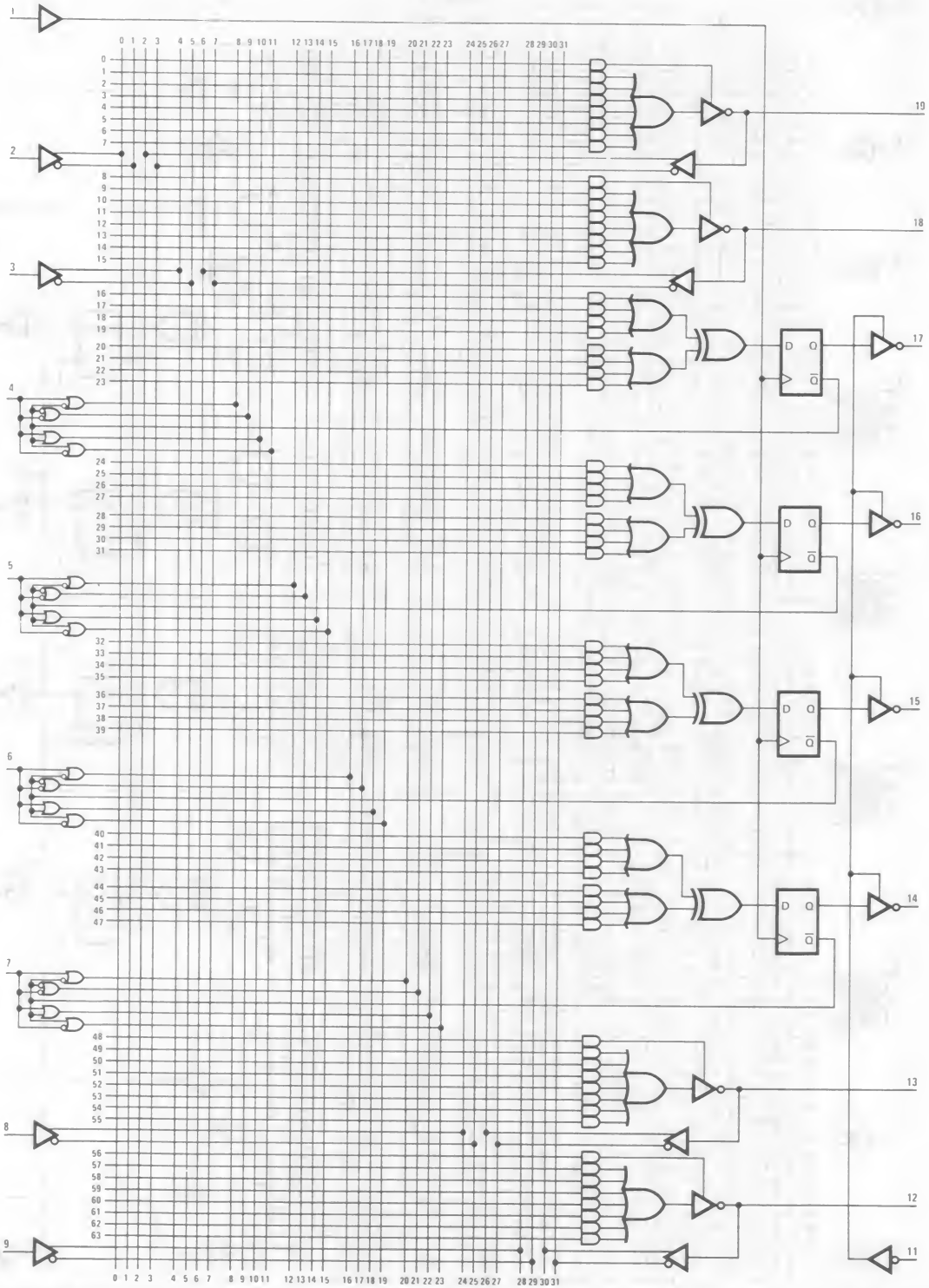
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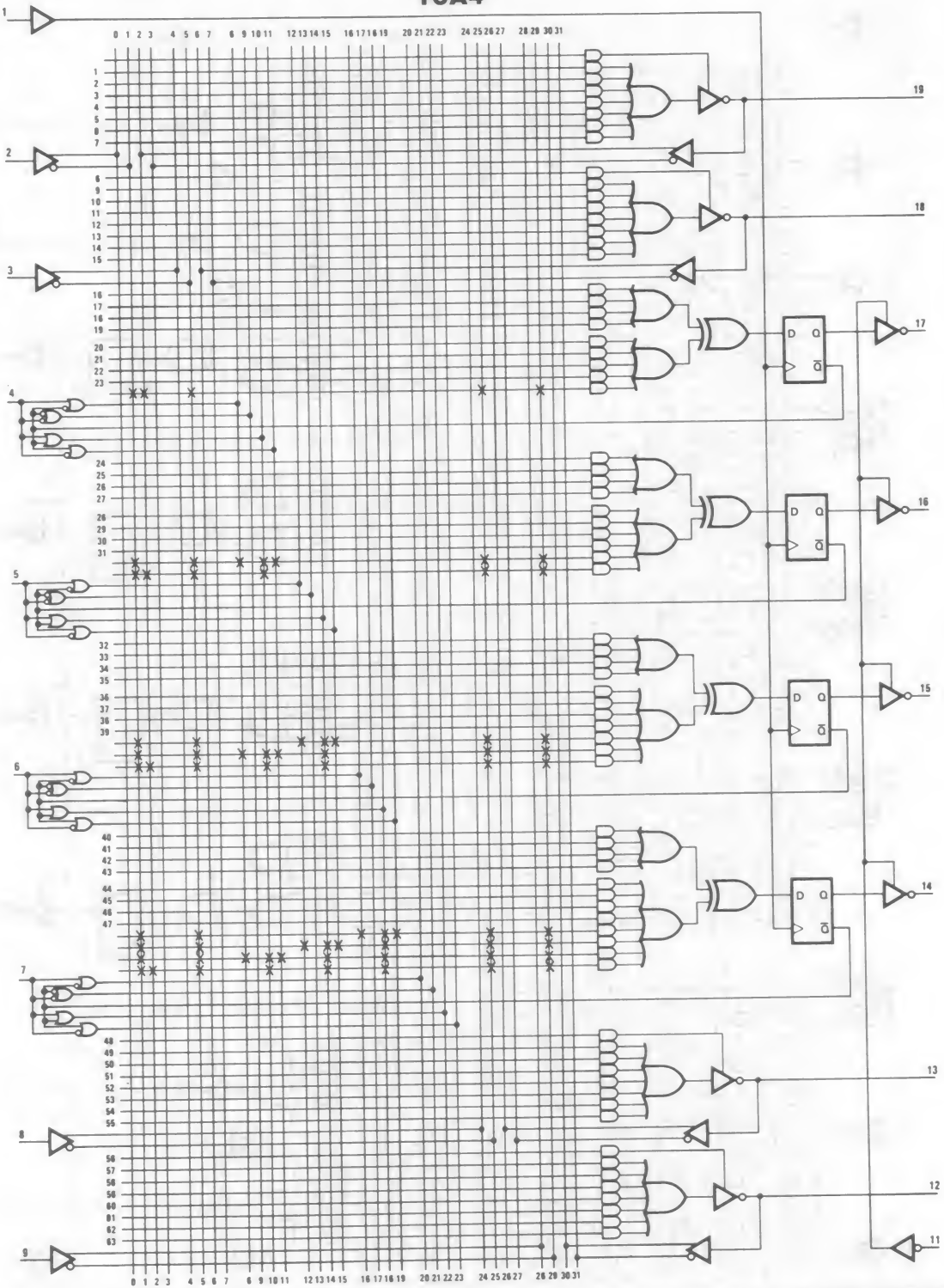
16A4



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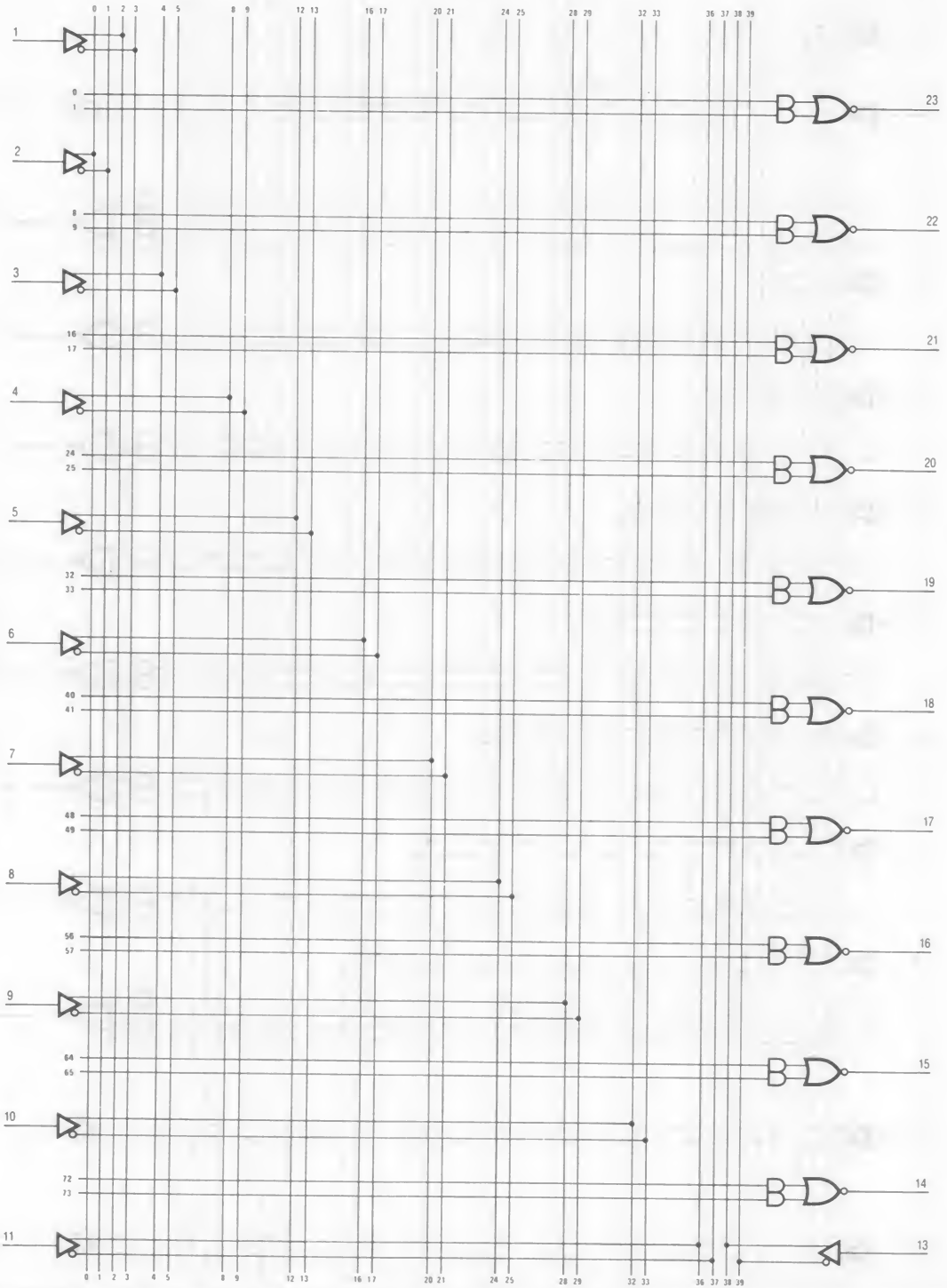
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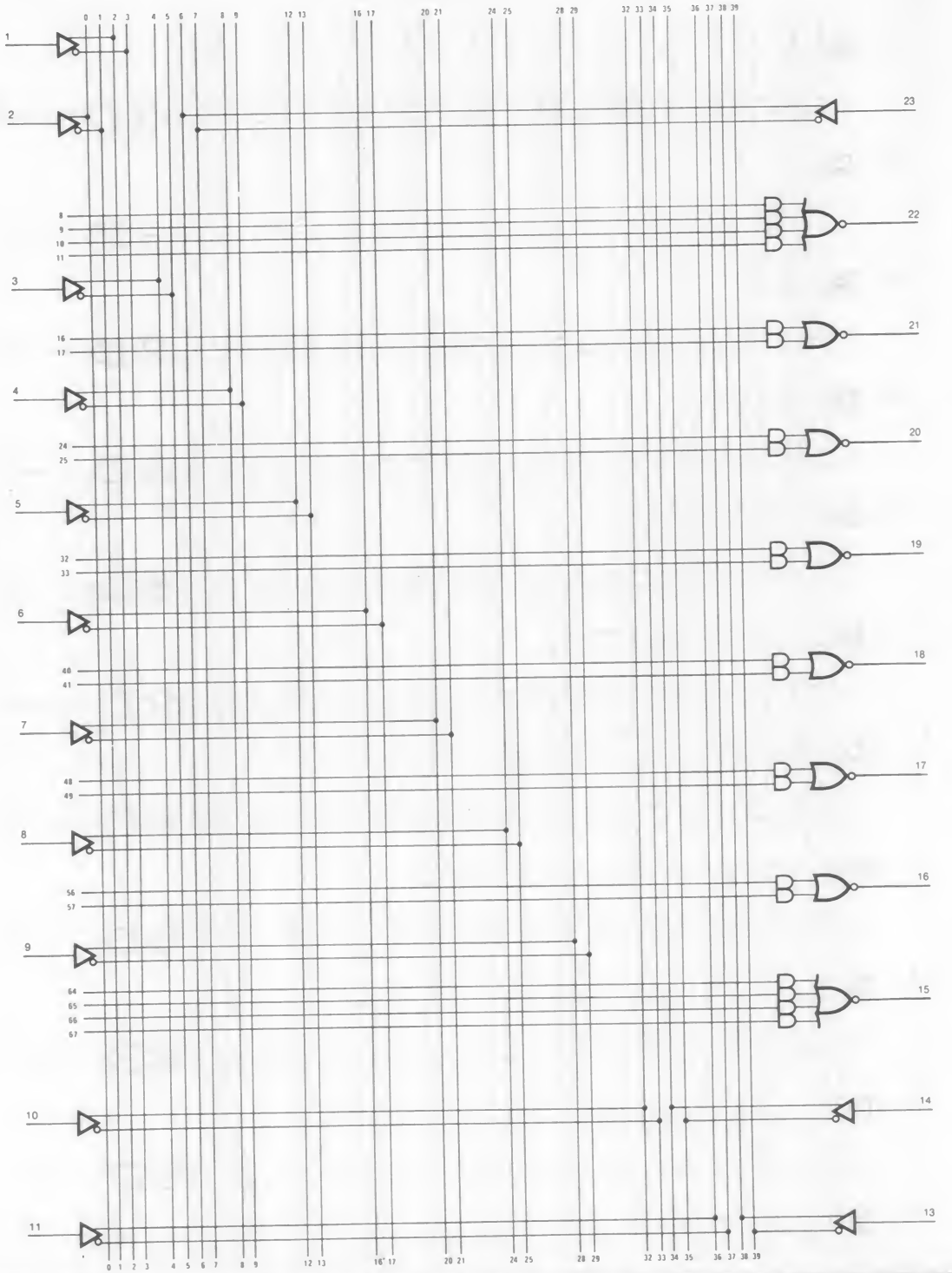
14L8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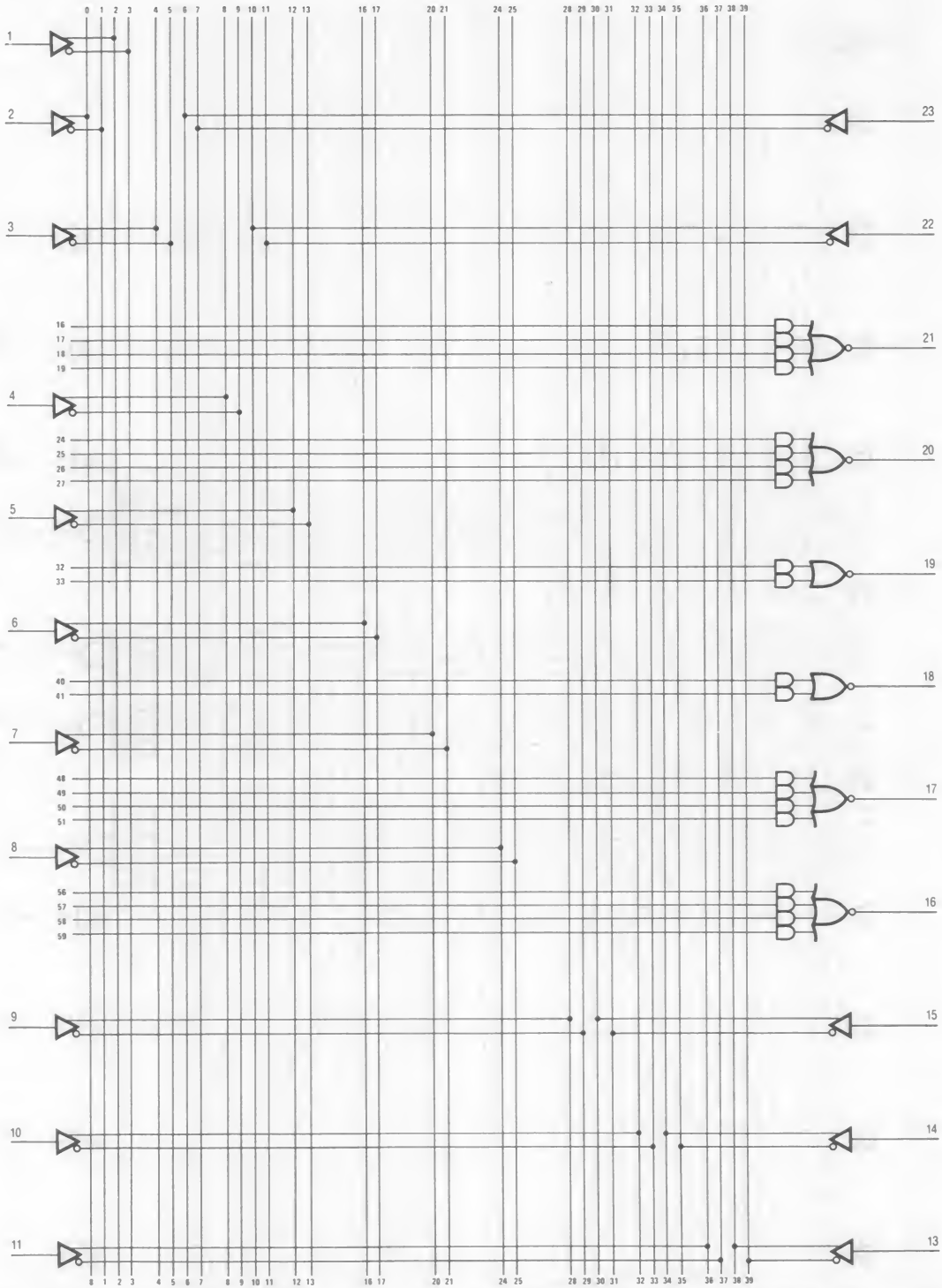
16L6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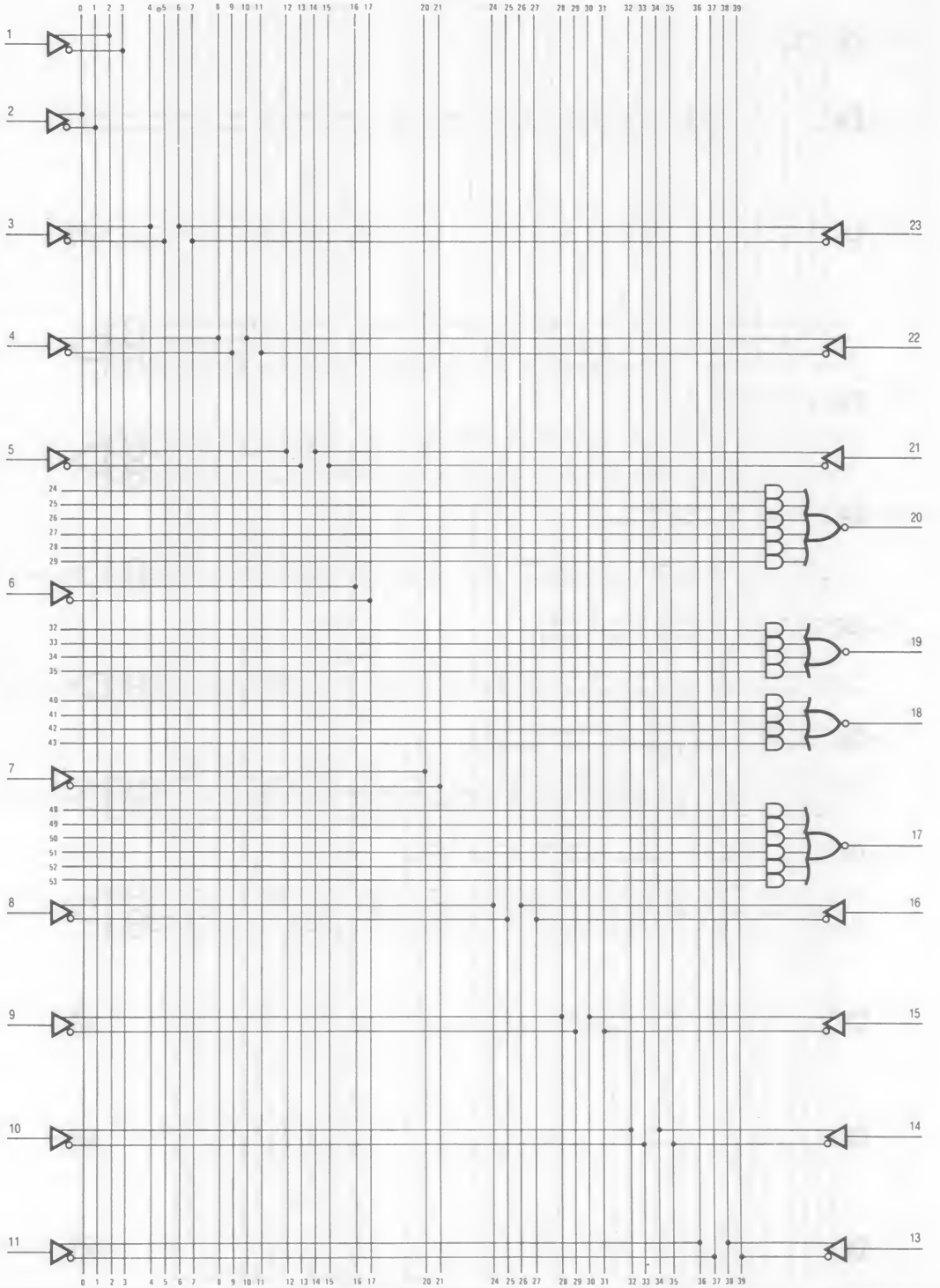
18L4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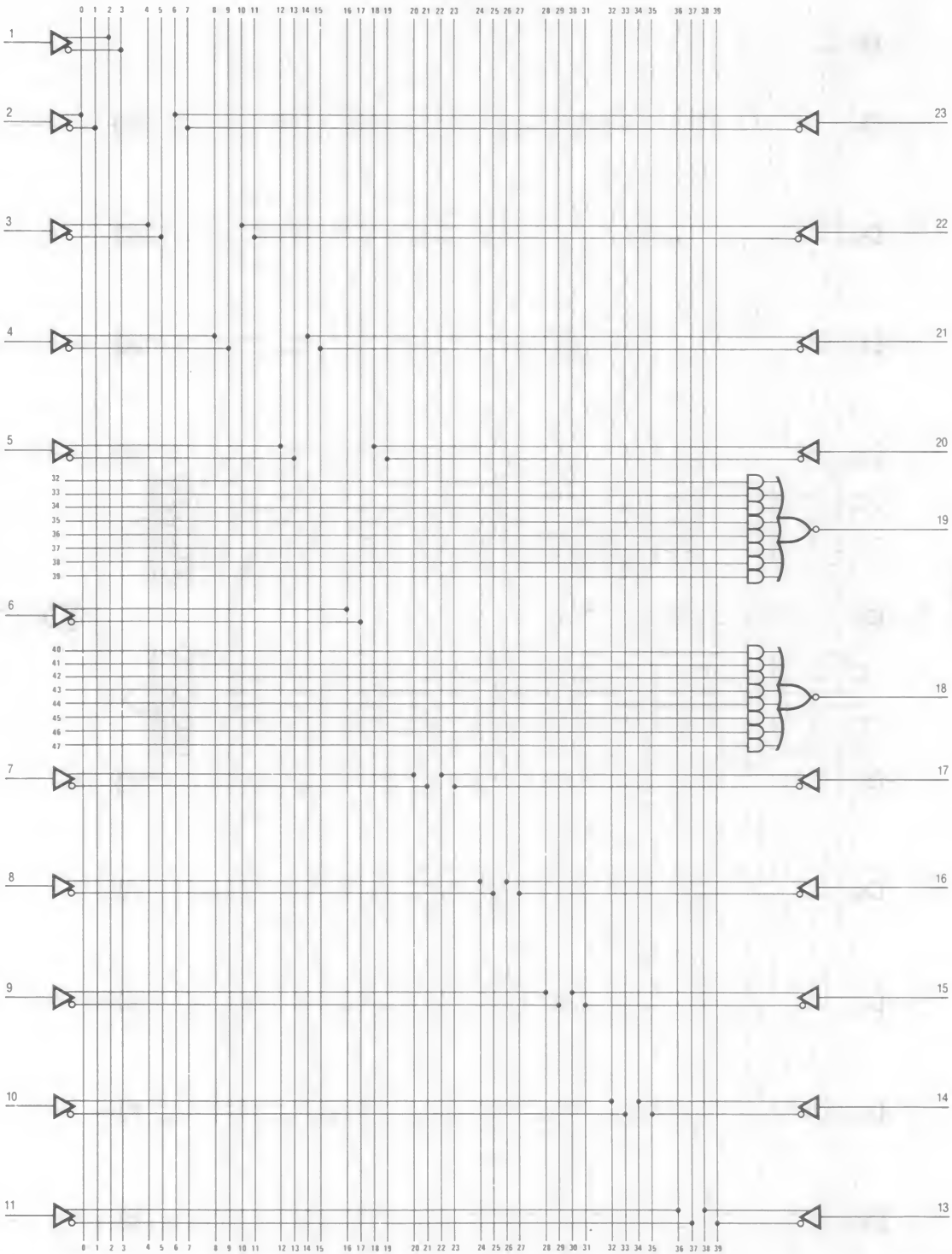
20L2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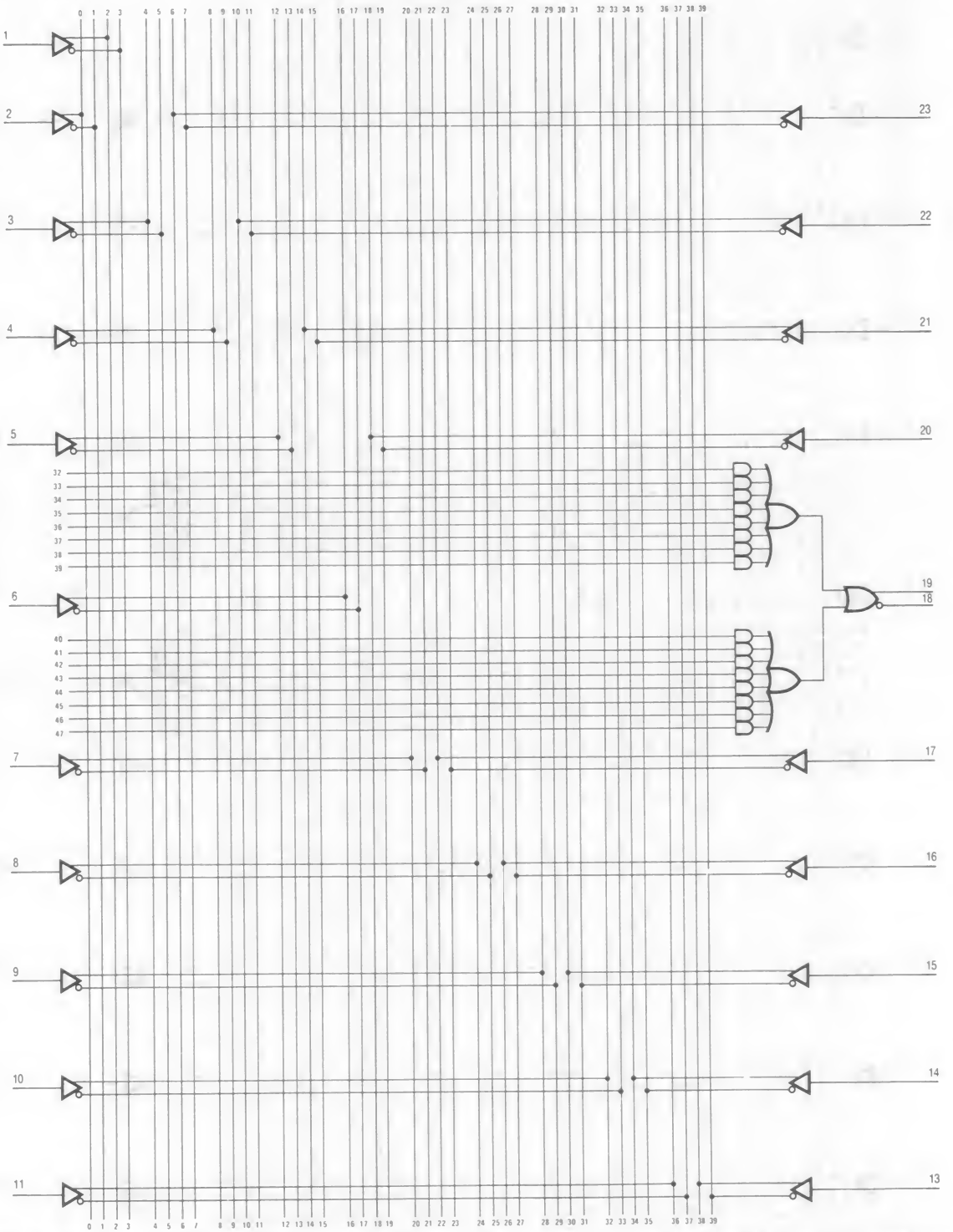
20C1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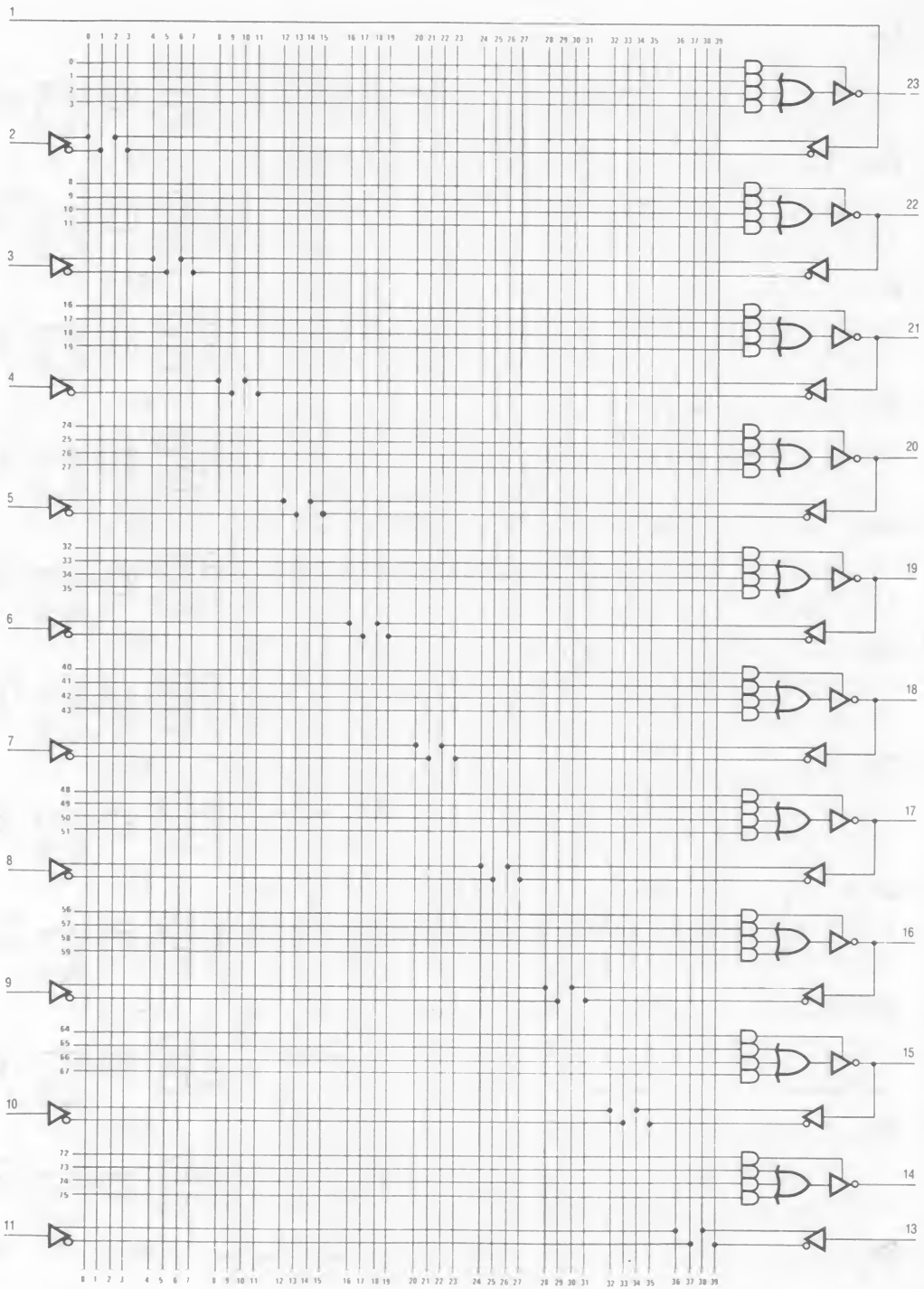
20L10



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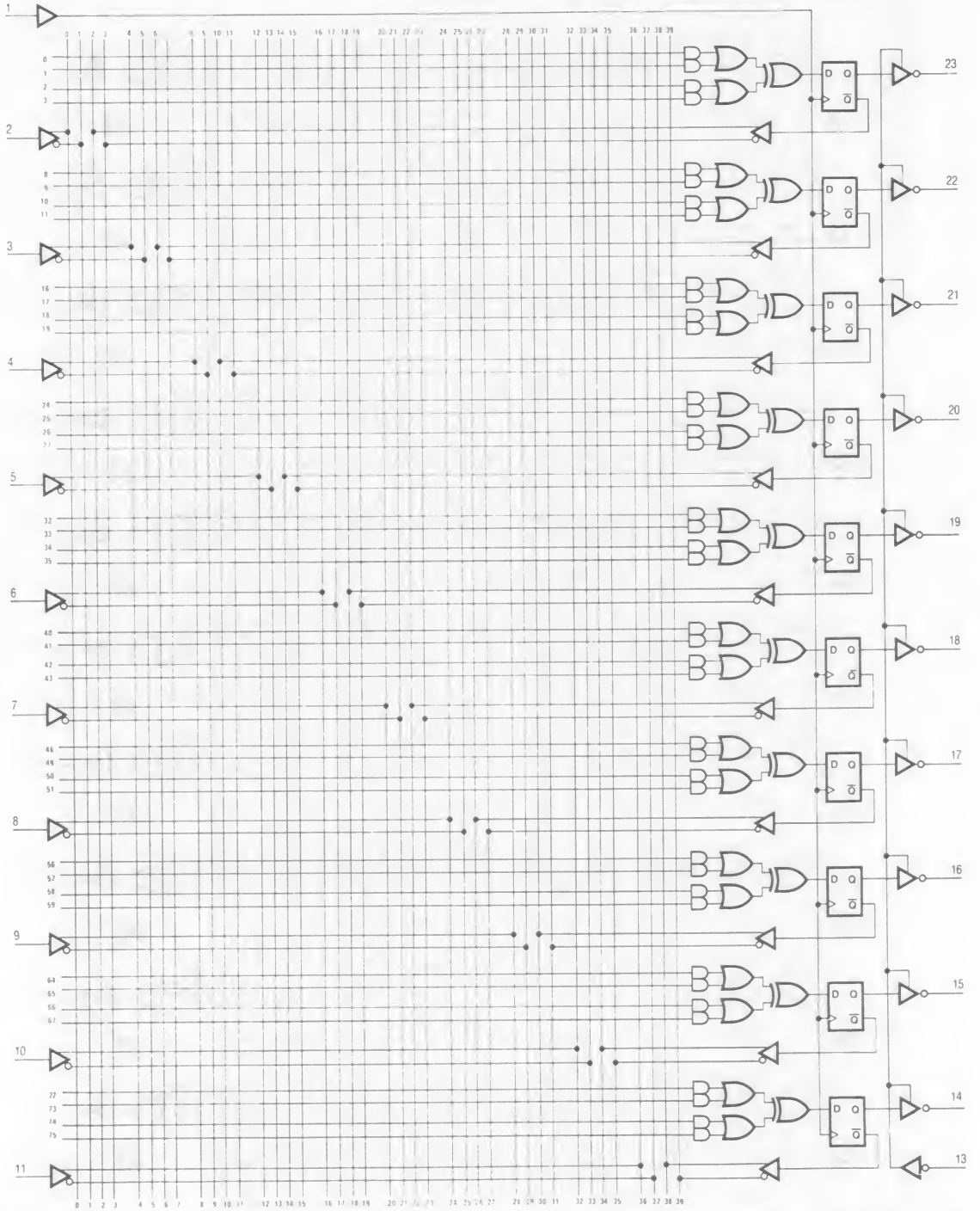

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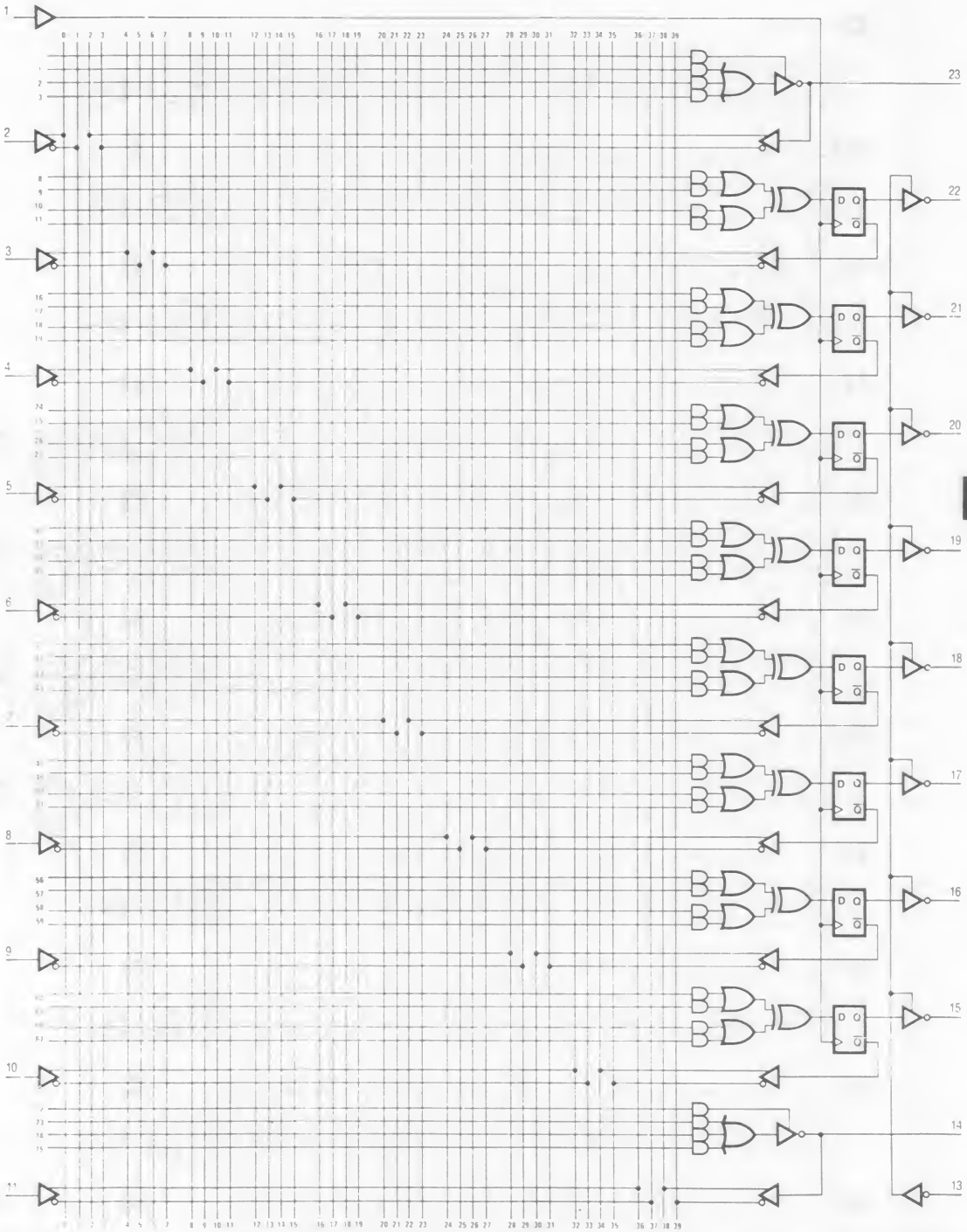

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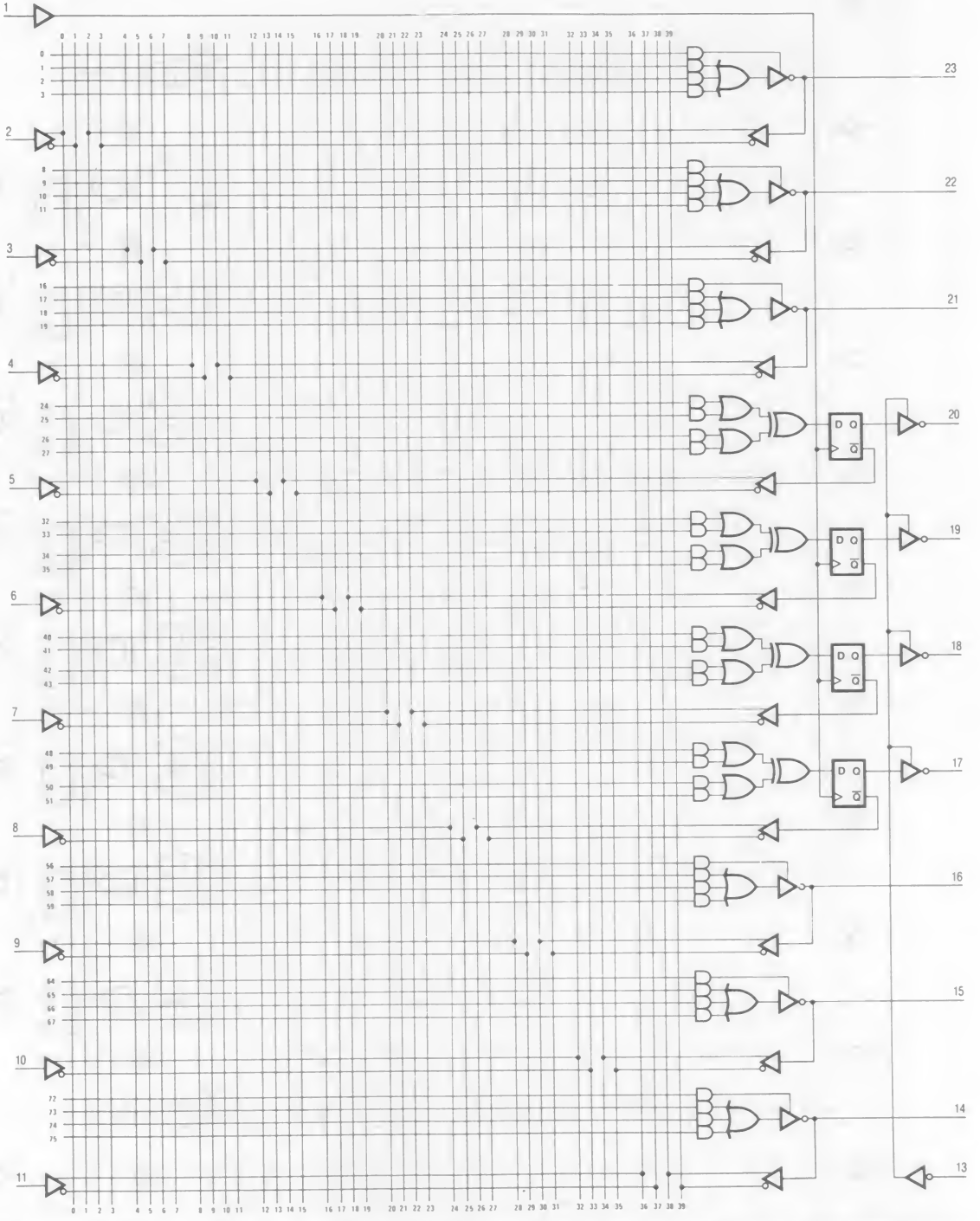

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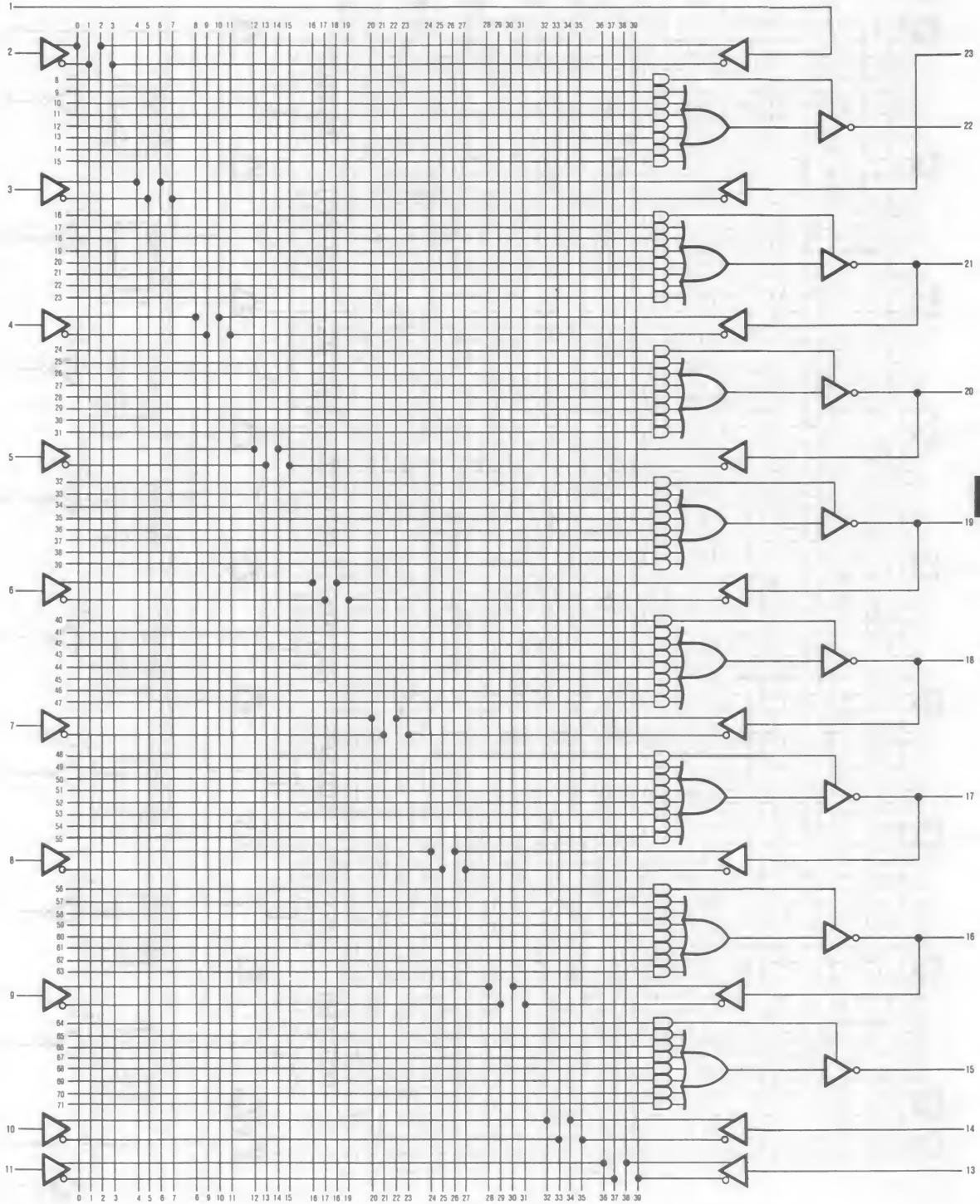
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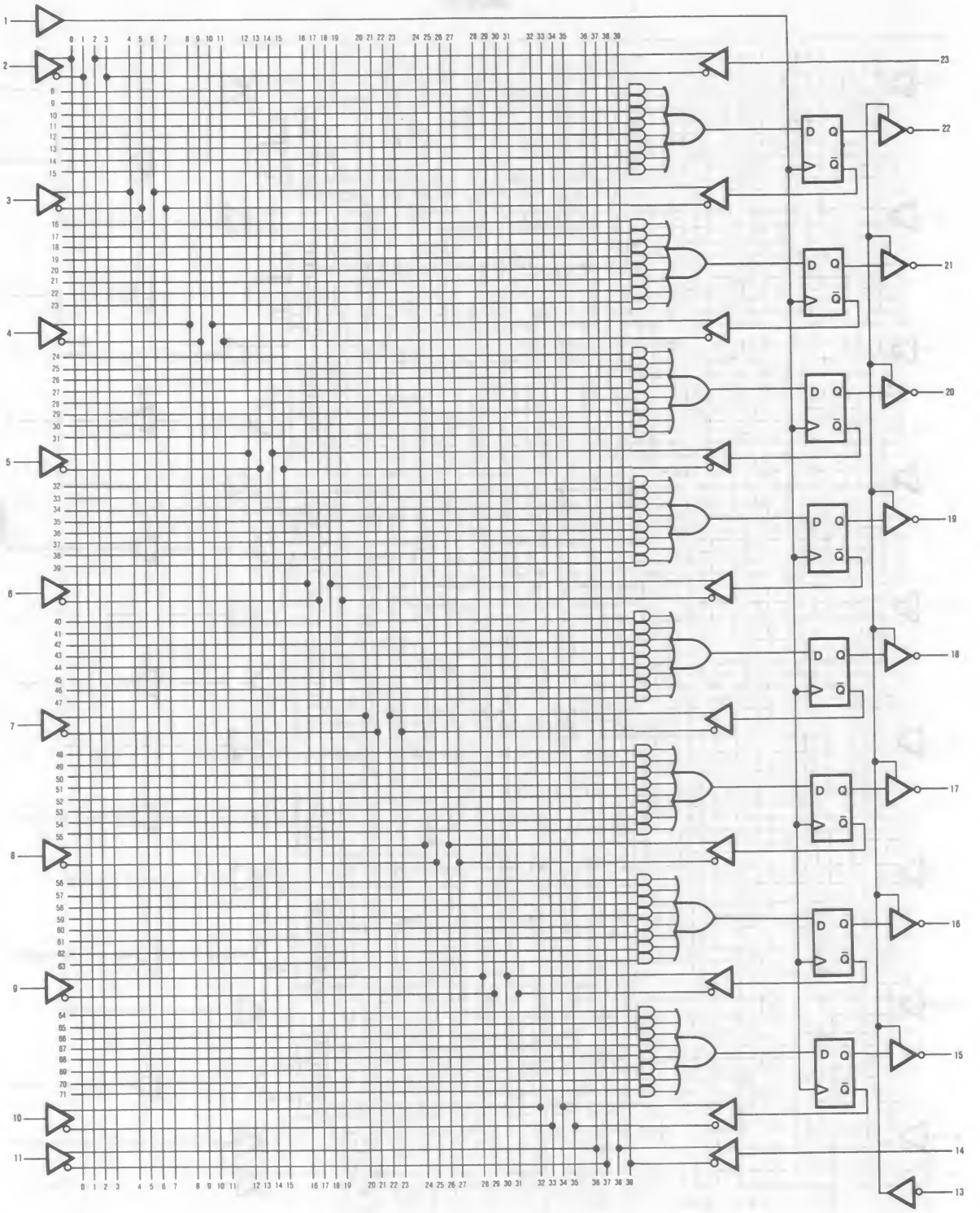
20R8



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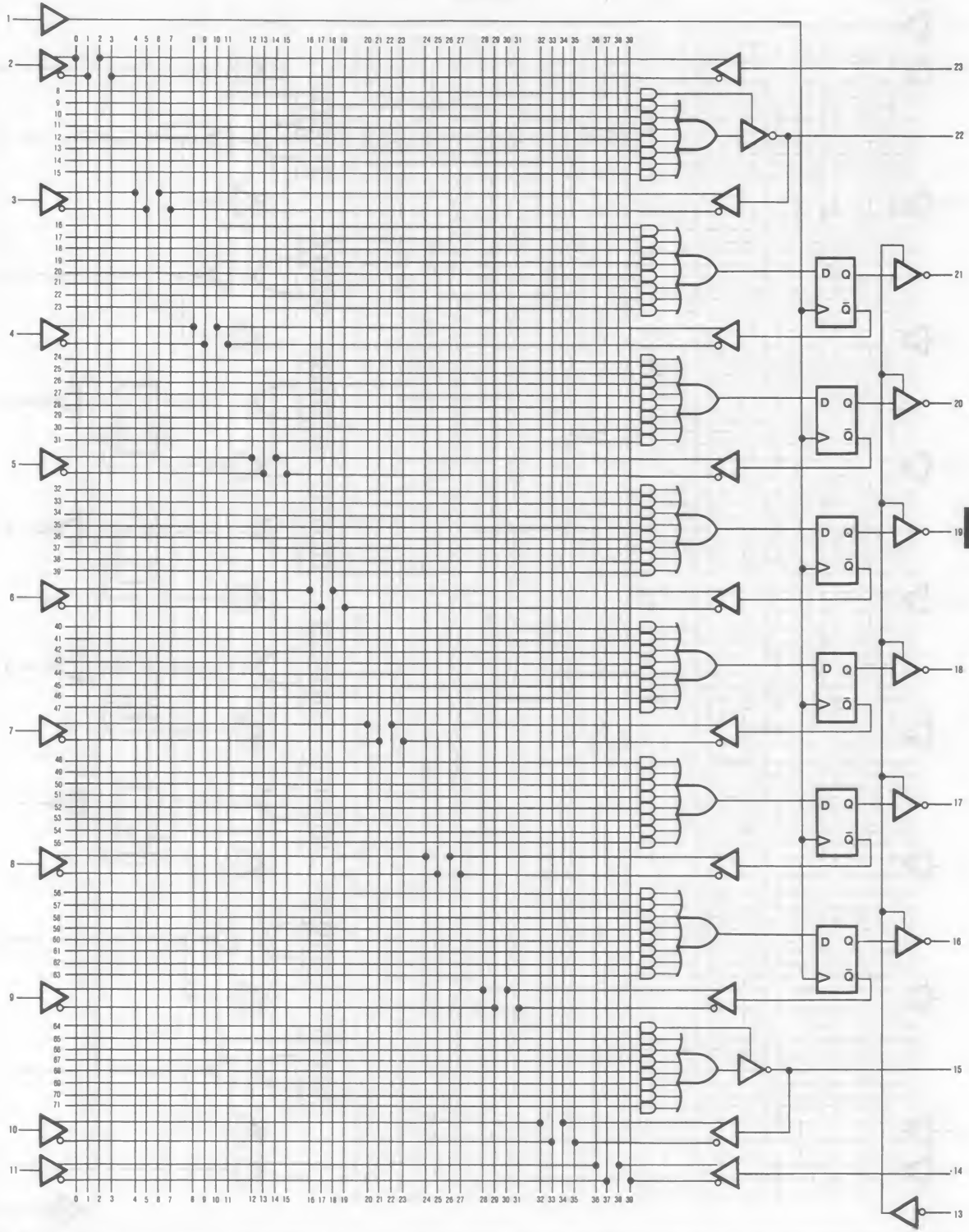

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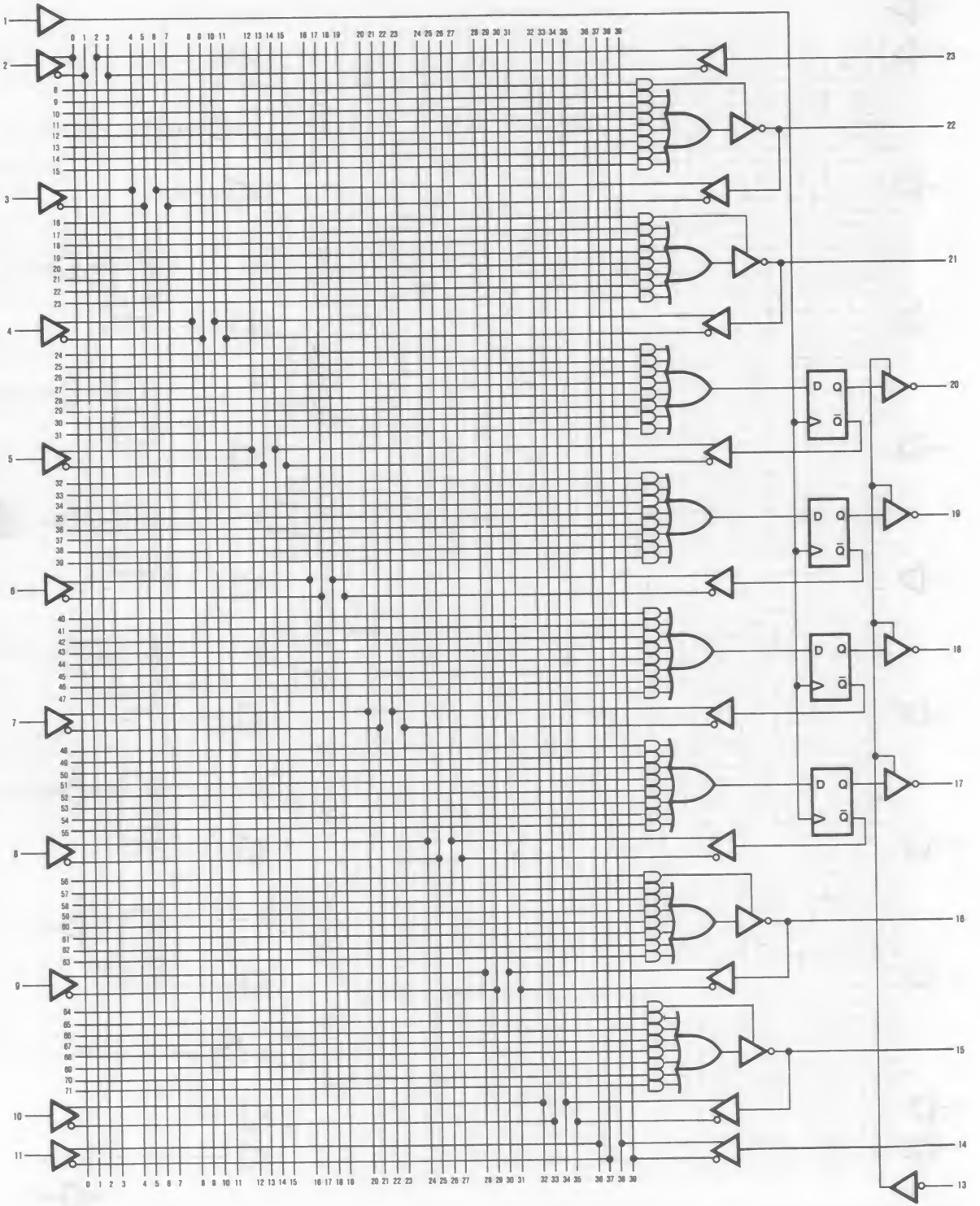
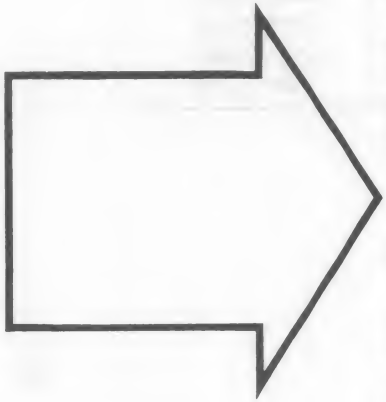




FUNCTION	PART NUMBER
Octal counter	SN54/74LS461
8-bit Up/Down counter	SN54/74LS469
Octal shift register	SN54/74LS498
Multifunction register	SN54/74LS380
10-bit counter	SN54/74LS491
16:1 Mux	SN54/74LS450
Dual 8:1 Mux	SN54/74LS451
Quad 4:1 Mux	SN54/74LS453
10-bit comparator	SN54/74LS460

HMSI

Octal Counter
SN54/74LS461

Features/Benefits

- **Octal counter for microprogram-counter, DMA controller and general purpose counting applications**
- **8 bits match byte boundaries**
- **Bus-structured pinout**
- **24-pin Skinny DIP® saves space**
- **3-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **Expandable in 8-bit increments**

Description

The LS461 is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D_7-D_0) into the output register (Q_7-Q_0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q_7-Q_0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

The output register (Q_7-Q_0— is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS461 octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I_1 is HIGH, I_0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

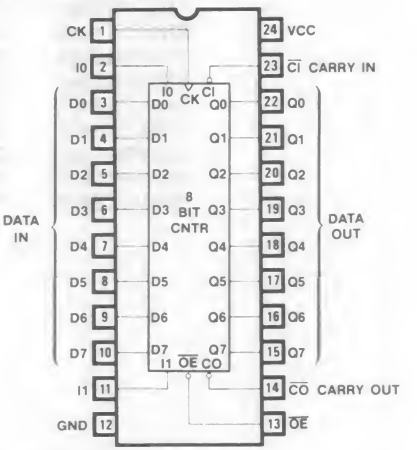
Function Table

$\overline{OE}$	CK	I1	I0	$\overline{CI}$	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	X	Z	HI-Z
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

Ordering Information

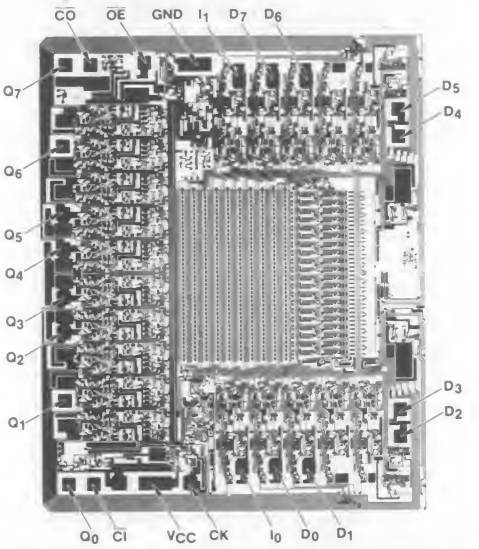
PART NUMBER	PACKAGE		TEMPERATURE
SN54LS461	JS, F	28L	MIL
SN74LS461	NS, JS		COM

Logic Symbol



Die Configuration

Die size: 140 x 172 mil

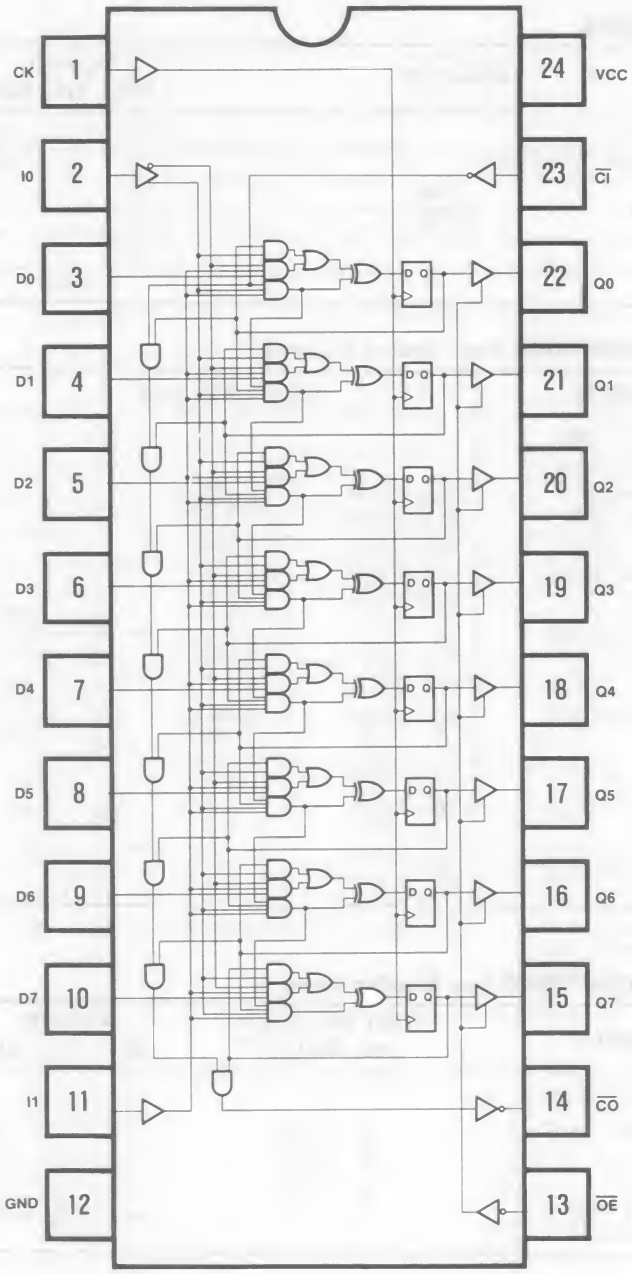


2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Logic Diagram

Octal Counter



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	40			35			ns
		High	30			25			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

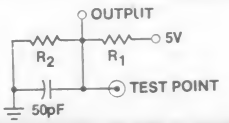
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP †	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current *	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

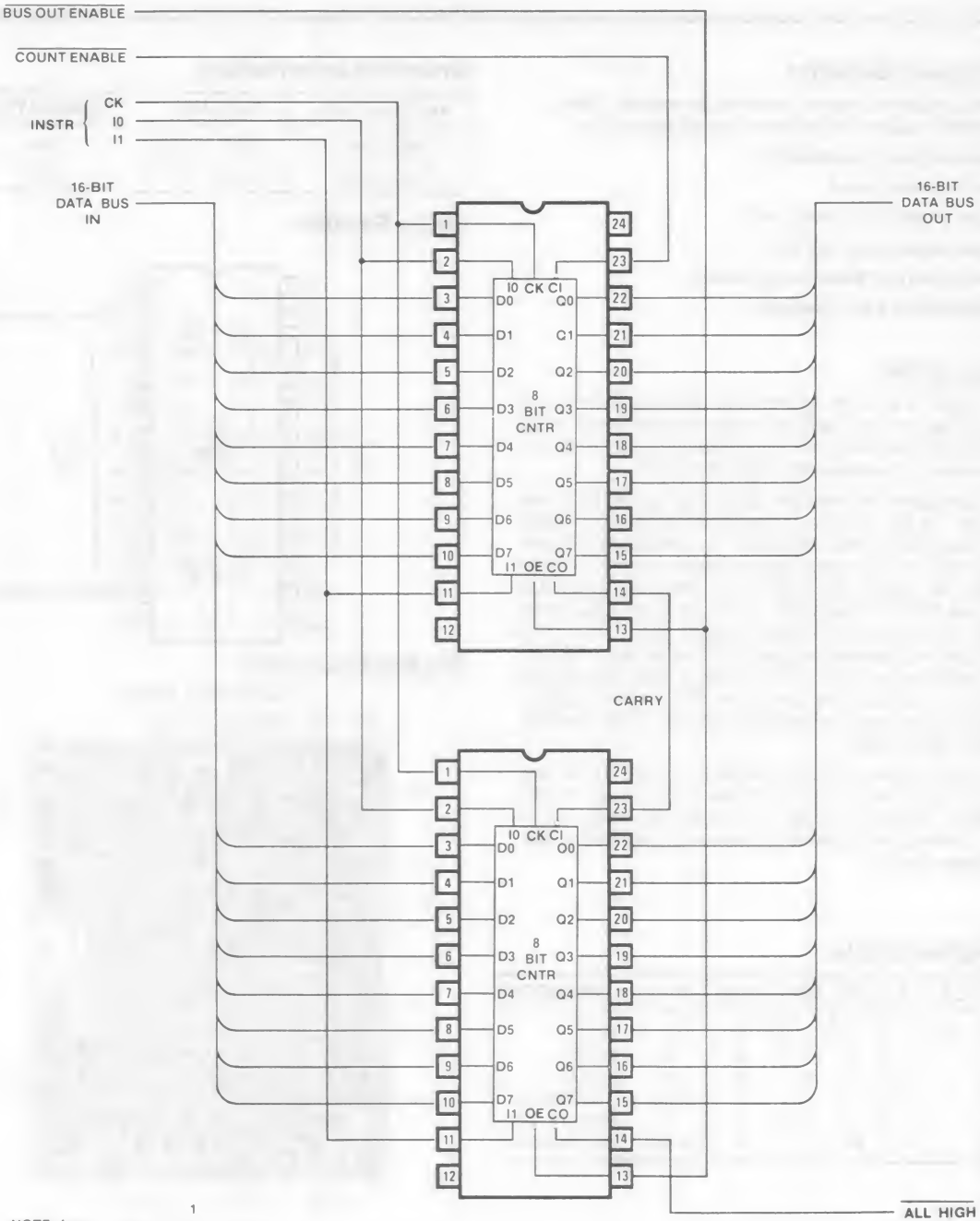
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	$\overline{CI}$ to $\overline{CO}$ delay			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to $\overline{CO}$			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Standard Test Load



Application

16-Bit Counter



NOTE: $f_{MAX} \approx \frac{1}{t_{PD\ CLK\ TO\ CO} + t_{SU}}$

8-Bit Up/Down Counter
SN54/74LS469

Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMA controller and general-purpose counting applications
- 8 bits matches byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Description

The 'LS469 is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ($\overline{LD}$, $\overline{UD}$, $\overline{CBI}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D_7-D_0) into the output register (Q_7-Q_0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CBI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q_7-Q_0) is all HIGHs, otherwise FALSE ($\overline{CBO}$ = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ($\overline{CBI}$ = LOW), otherwise the operation is a HOLD. The borrow-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q_7-Q_0) is all LOWs, otherwise FALSE ($\overline{CBO}$ = HIGH).

The output register (Q_7-Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469 octal up/down counters may be cascaded to provide larger counters.

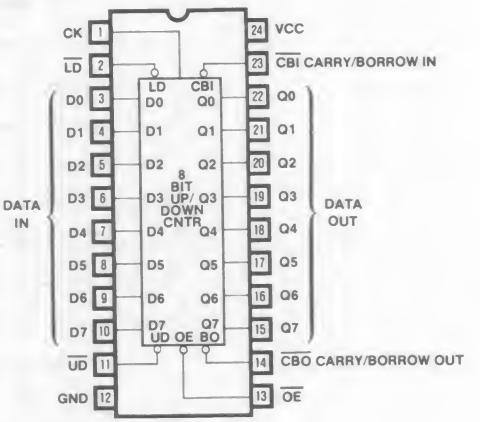
Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{UD}$	$\overline{CBI}$	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	D	D	LOAD
L	↑	H	L	H	X	Q	HOLD
L	↑	H	L	L	X	Q plus 1	INCREMENT
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q minus 1	DECREMENT

Ordering Information

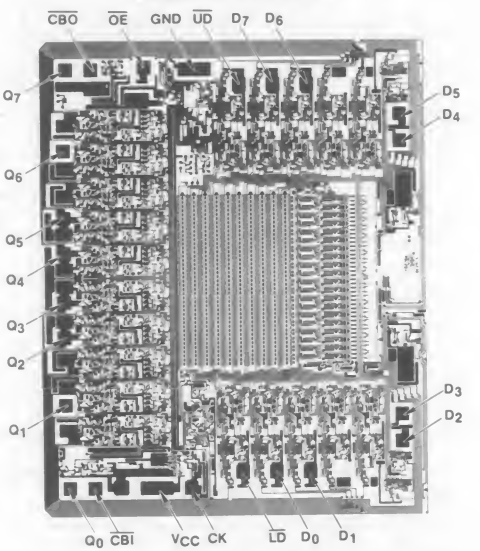
PART NUMBER	PACKAGE		TEMPERATURE
SN54LS469	JS, F	28L	MIL
SN74LS469	NS, JS		COM

Logic Symbol



Die Configuration

Die size: 140 x 172 mil



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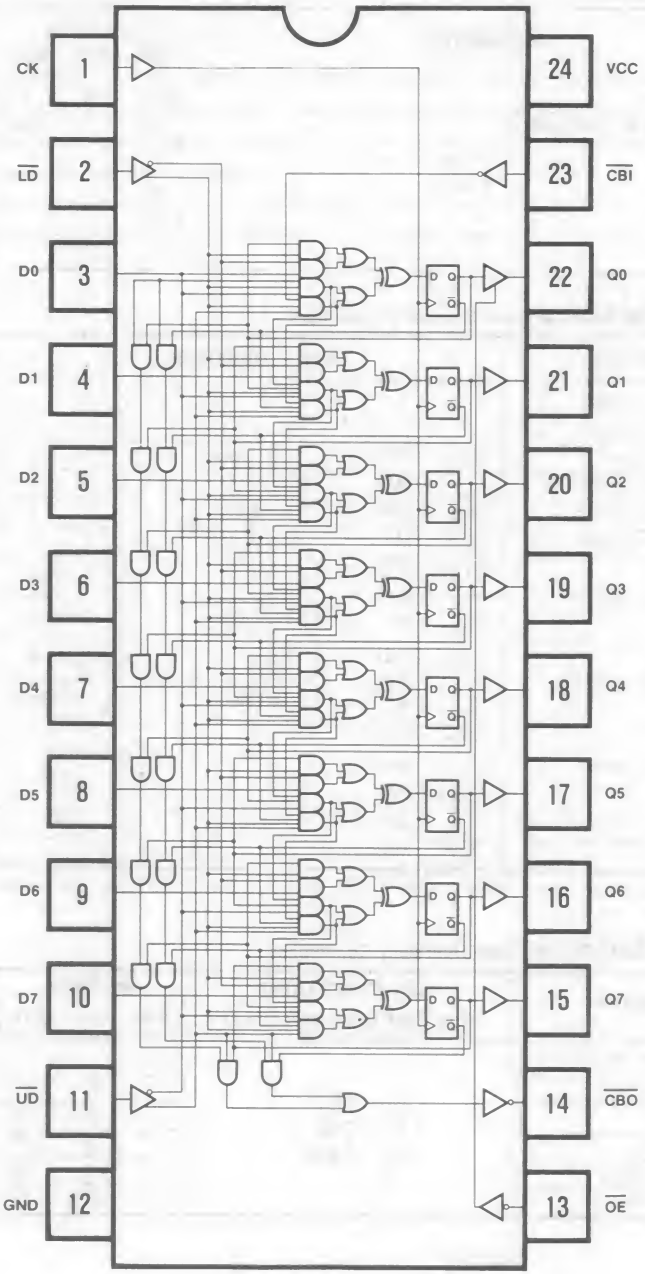
Monolithic Memories

Logic Diagram

8-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	40			35	10		ns
		High	30			25			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

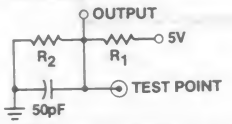
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
† All typical values are V_{CC} = 5V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

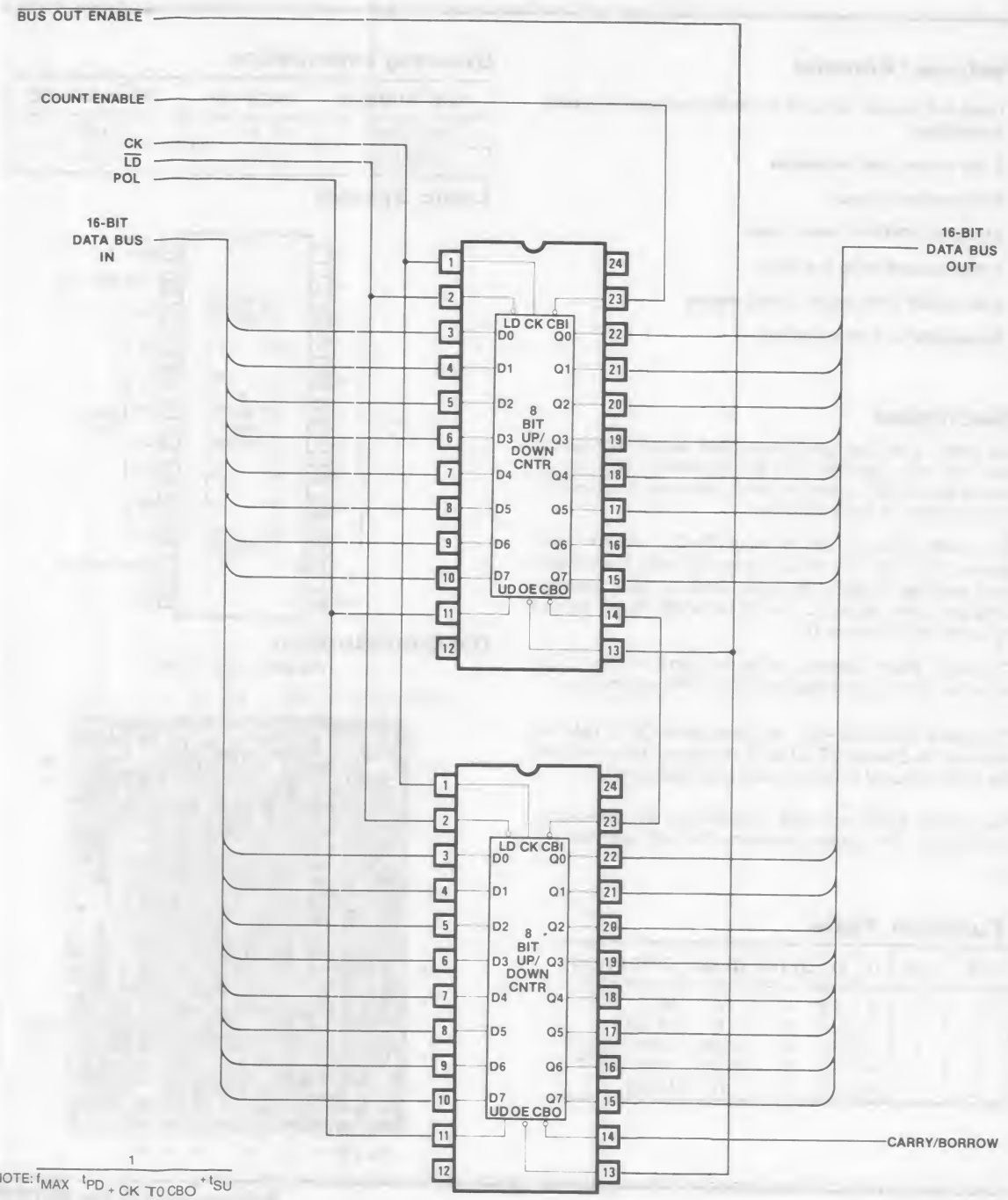
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	$\overline{CBI}$ to $\overline{CBO}$ delay			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to CBO			55	95		55	80	ns
t_{PZX}	Output enable delay			20	45		20	35	ns
t_{PXZ}	Output disable delay			20	45		20	35	ns

Standard Test Load



Application

16-Bit Register



NOTE: $f_{MAX} = \frac{1}{t_{PD} + CK\ T0\ CBO + t_{SU}}$

8

Octal Shift Register
SN54/74LS498

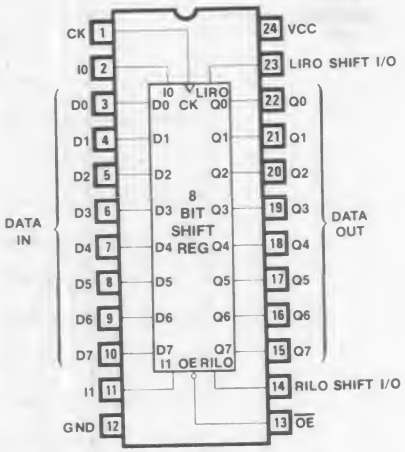
Features/Benefits

- Octal shift register for serial to parallel and parallel to serial applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS498	JS, F	28L	MIL
SN74LS498	NS, JS		COM

Logic Symbol



Description

The LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the input (D_7-D_0) into the output register (Q_7-Q_0). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, Q, one bit to the left; Q_0 is replaced by LIRO. RILO outputs Q_7.

The SHIFT RIGHT operation shifts the output register, Q, one bit to the right; Q_7 is replaced by RILO. LIRO outputs Q_0.

The output register (Q_7-Q_0— is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

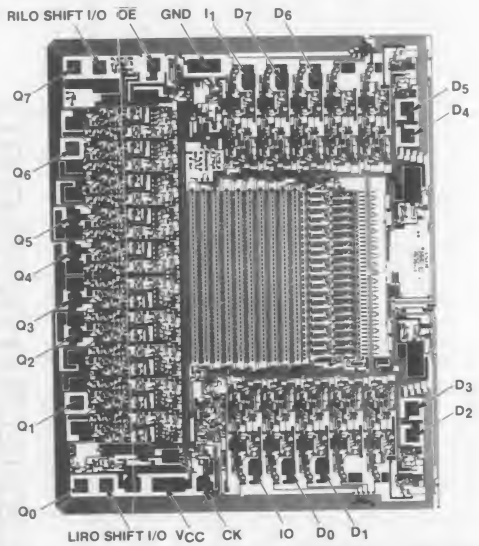
Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application section.

Function Table

$\overline{OE}$	CK	I1	I0	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	Z	HI-Z
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

Die Configuration

Die size: 140 x 172 mil



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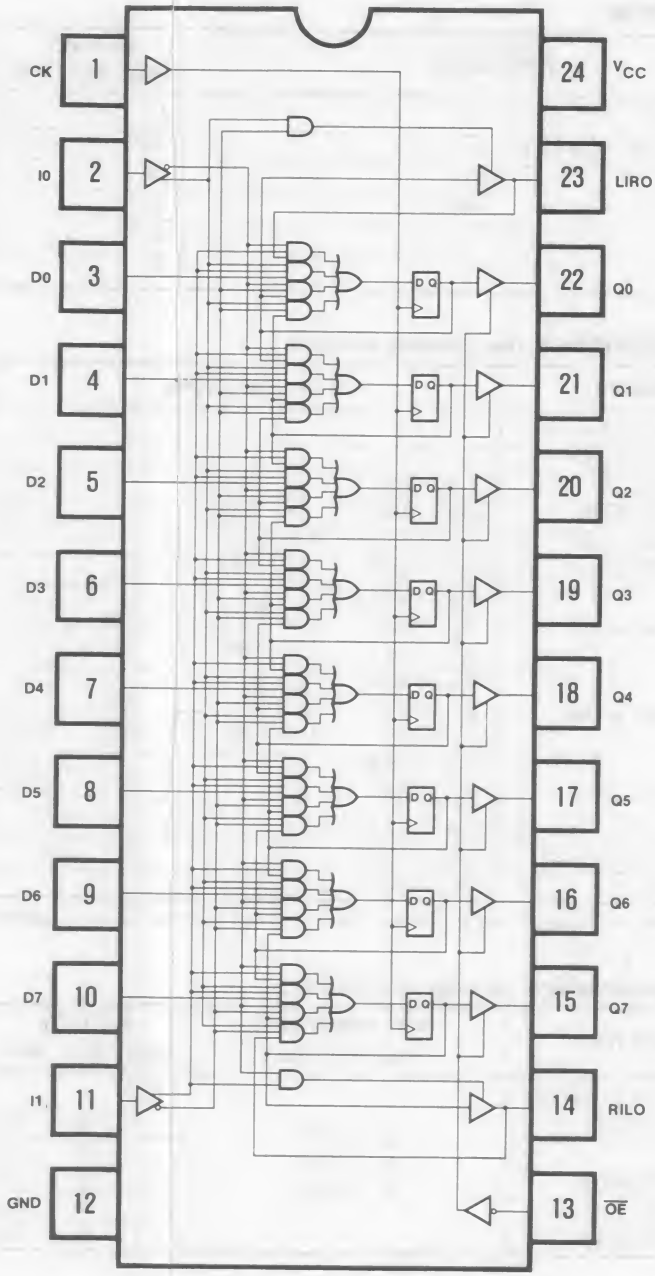
Monolithic Memories

Logic Diagram

Octal Shift Register



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	Low	40			35			ns
		High	30			25			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

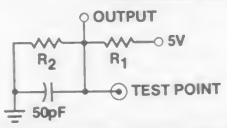
* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

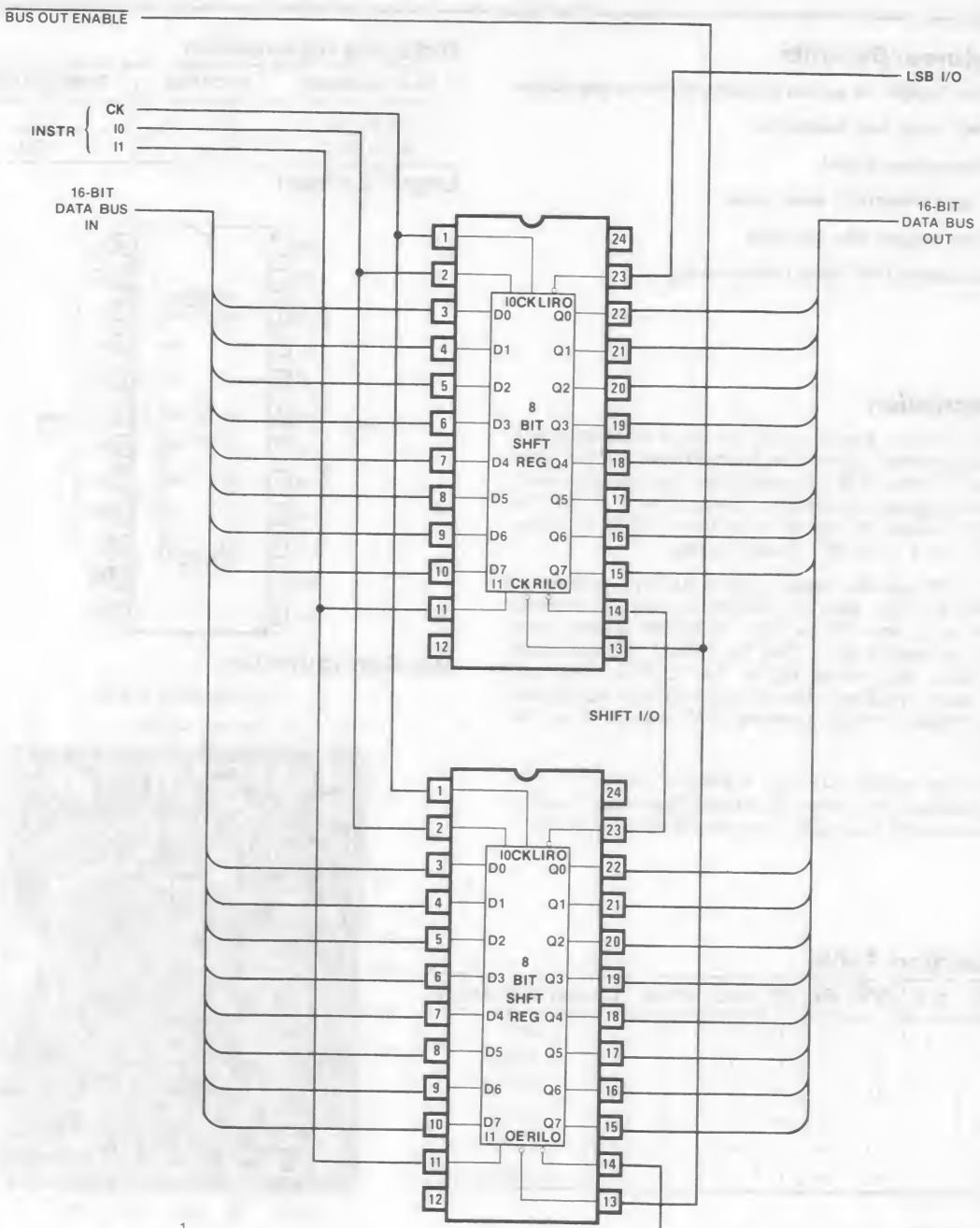
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	I0, I1 to LIRO, RILO			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to LIRO, RILO			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Standard Test Load



Application

16-Bit Shift Register



NOTE: $f_{MAX} = \frac{1}{t_{PD\ CLK\ TO\ LIRO} + t_{SU}}$

8

Multifunction Octal Register
SN54/74LS380

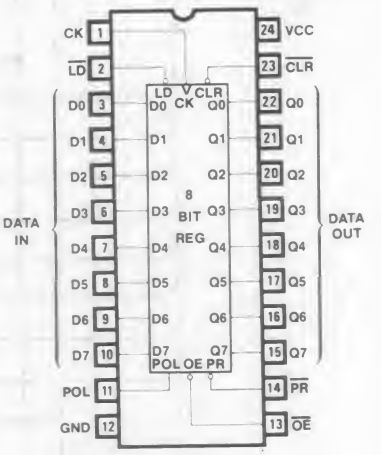
Features/Benefits

- Octal Register for general purposes interfacing applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS380	JS, F	28L	MIL
SN74LS380	NS, JS		COM

Logic Symbol



Description

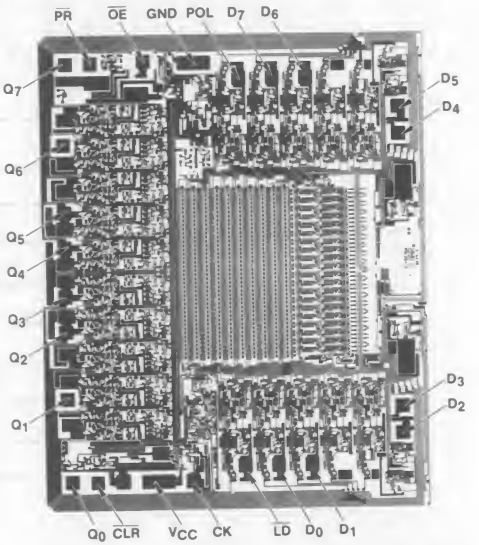
The LS380 is an 8-bit synchronous register with parallel load, load complement, preset, clear, and hold capacity. Four control inputs ($\overline{LD}$, POL, $\overline{CLR}$, $\overline{PR}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The LS380 combines the features of the LS374, LS377, LS273 and LS534 into a single 300 mil wide package.

The LOAD operation loads the inputs (D_7-D_0) into the output register (Q_7-Q_0), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

The output register (Q_7-Q_0— is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Die Configuration

Die size: 140 x 172 mil



Function Table

$\overline{OC}$	CLK	$\overline{CLR}$	$\overline{PR}$	$\overline{LD}$	POL	D7-D0	Q7-Q0	OPERATION
H	X	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	X	X	L	CLEAR
L	↑	H	L	X	X	X	H	PRESET
L	↑	H	H	H	X	X	Q	HOLD
L	↑	H	H	L	H	D	D	LOAD true
L	↑	H	H	L	L	D	$\overline{D}$	LOAD comp

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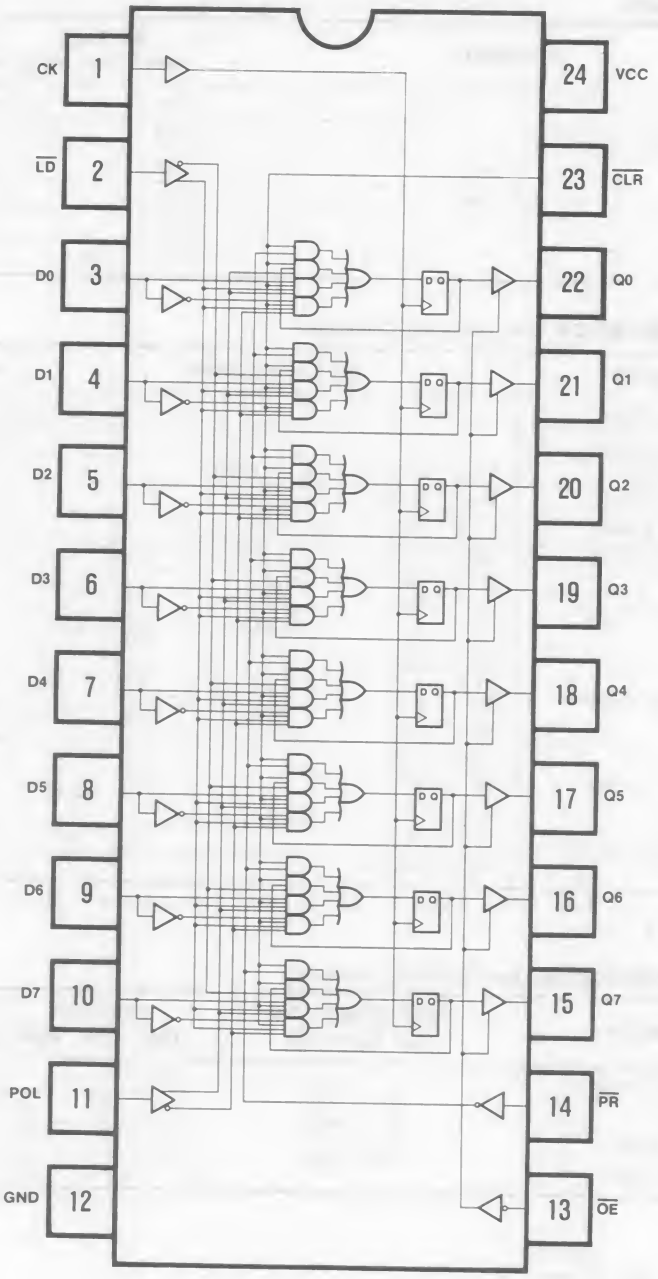
Monolithic Memories

Logic Diagram

Octal Register



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	High	40			40			ns
		Low	35			35			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

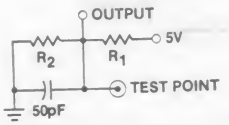
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
† All typical values are at V_{CC} = 5V T_A = 25°C

Switching Characteristics Over Operating Conditions

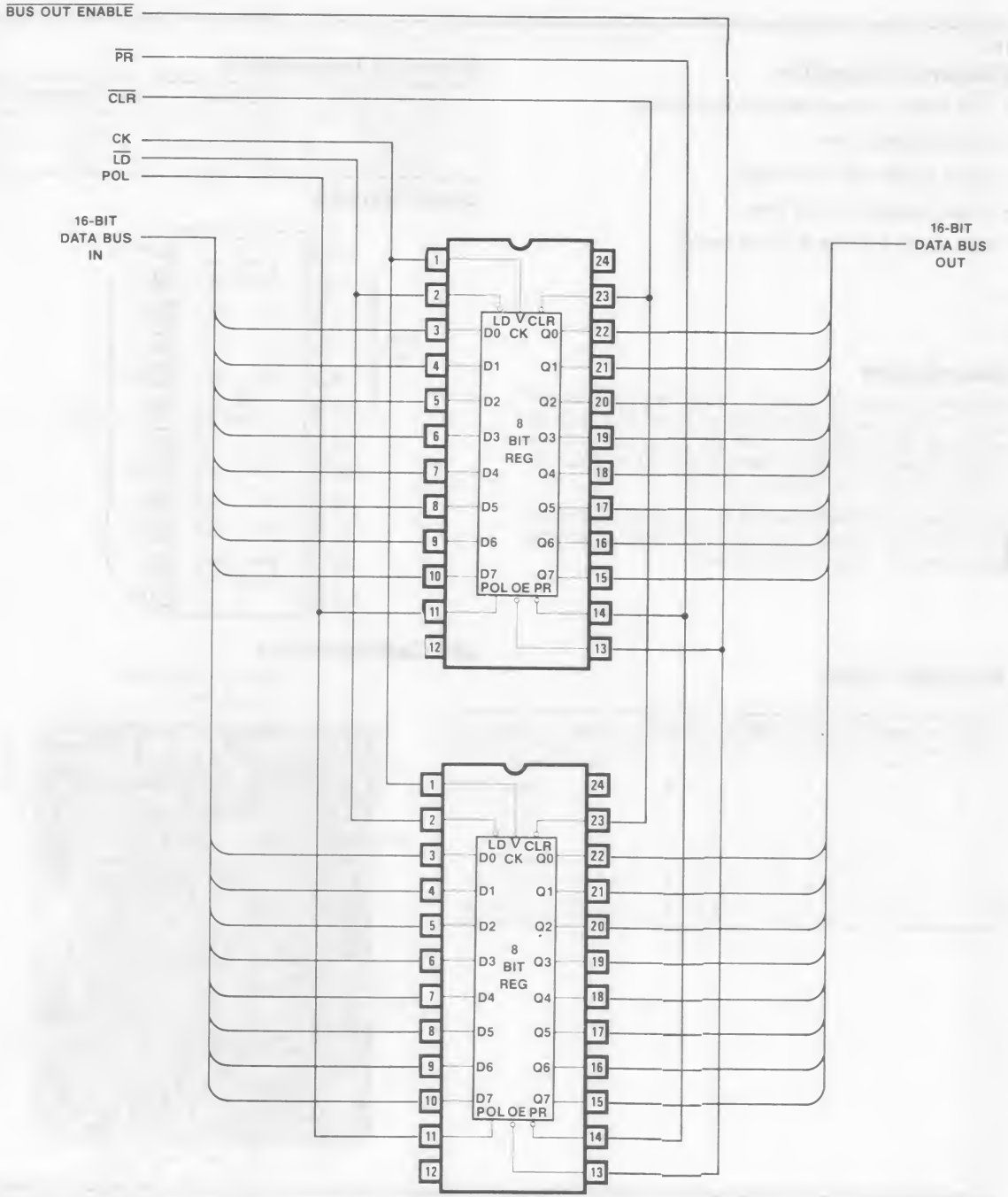
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Standard Test Load



Application

16-Bit Register



10-Bit Counter
SN54/74LS491

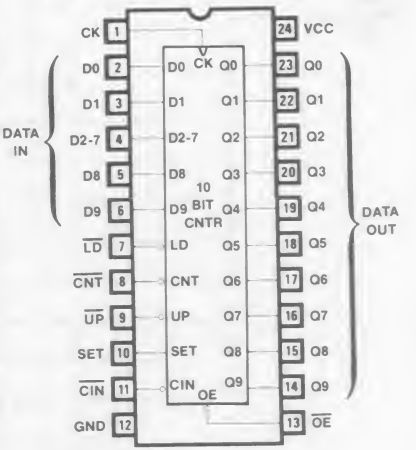
Features/Benefits

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- 24-pin SKINNYDIP™ saves space
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS491	JS, F	28L	MIL
SN74LS491	NS, JS		COM

Logic Symbol



Description

The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on CIN, otherwise it holds.

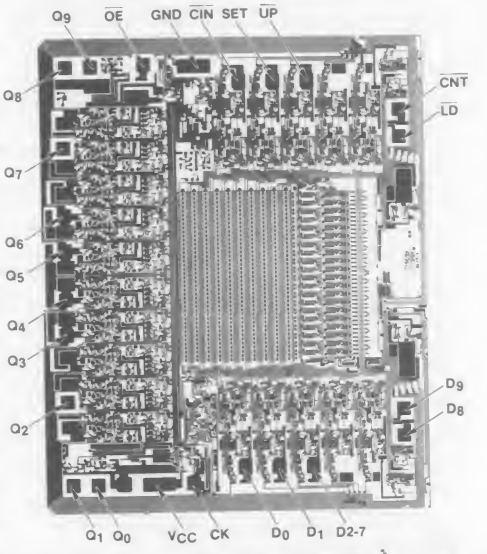
All outputs are enabled when $\overline{OE}$ is low, otherwise HIGH-Z. The 24 mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Function Table

$\overline{OE}$	CK	SET	$\overline{LD}$	$\overline{CNT}$	$\overline{CIN}$	$\overline{UP}$	D9-D0	Q9-Q0	OPERATION
H	X	X	X	X	X	X	X	Z	HI-Z
L	↑	H	X	X	X	X	X	H	Set all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q plus 1	Count UP
L	↑	L	H	L	L	H	X	Q minus 1	Count DN

Die Configuration

Die size: 140 x 172 mil



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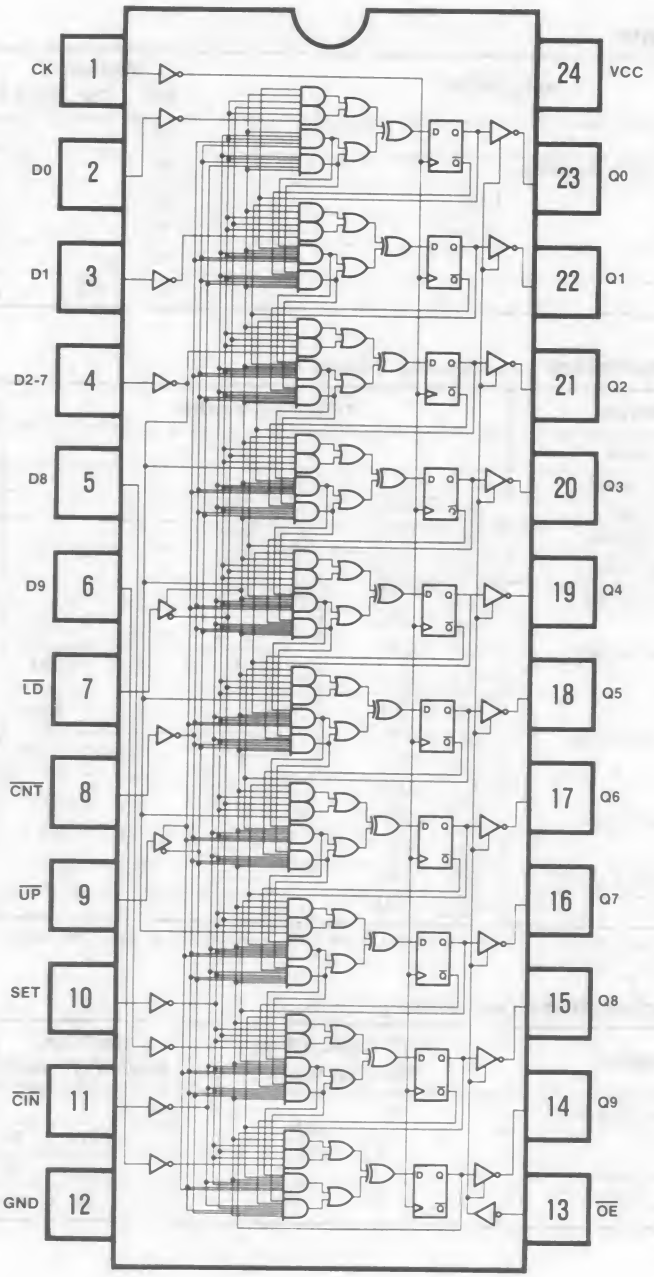
Monolithic Memories

Logic Diagram

10-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125*	0		75	°C
t_w	Width of clock	High	40			40			ns
		Low	35			35			
t_{su}	Set up time		60			50			ns
t_h	Hold time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

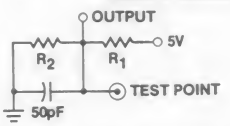
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA			0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

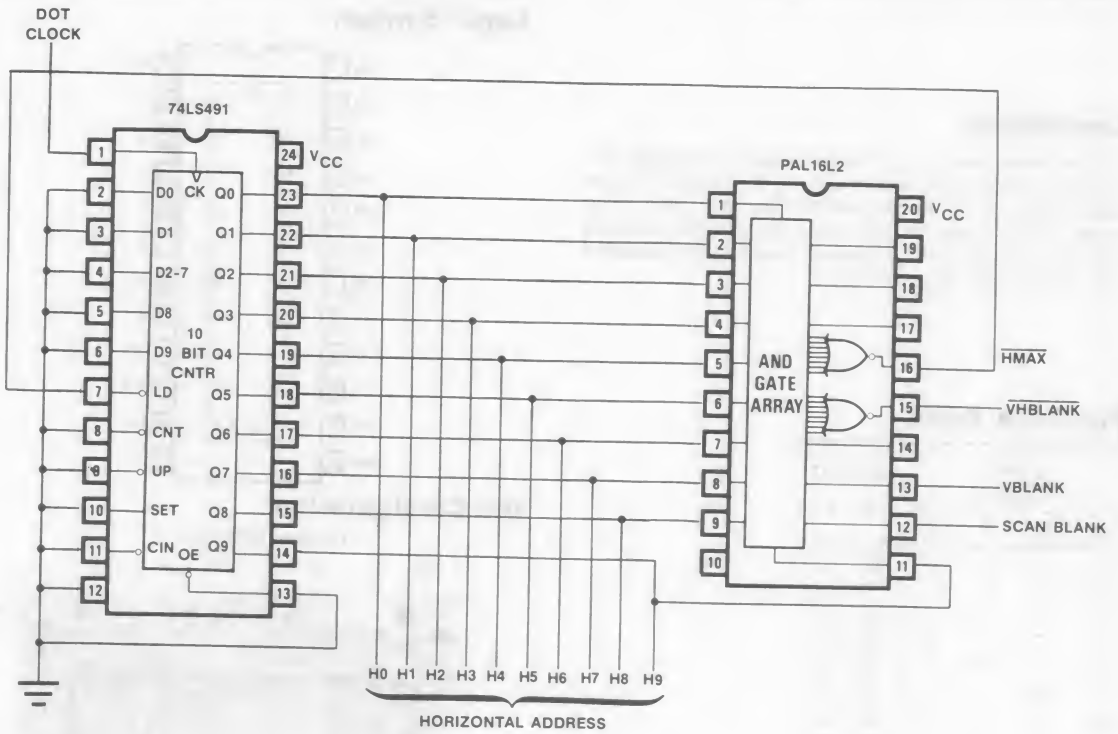
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 50pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

Standard Test Load



Application

CRT Horizontal Timing and Blanking



8

16:1 Mux
SN54/74LS450

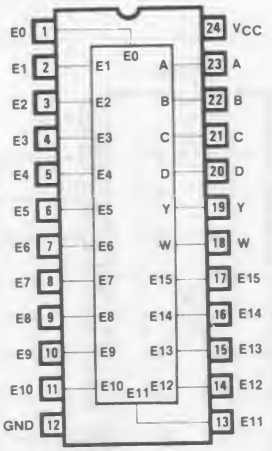
Features/Benefits

- 24-pin SKINNYDIP™ saves space
- Similar to 74150 (Fat DIP)
- Low current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54LS450	JS, F	28L	MIL
SN74LS450	NS, JS		COM

Logic Symbol



Description

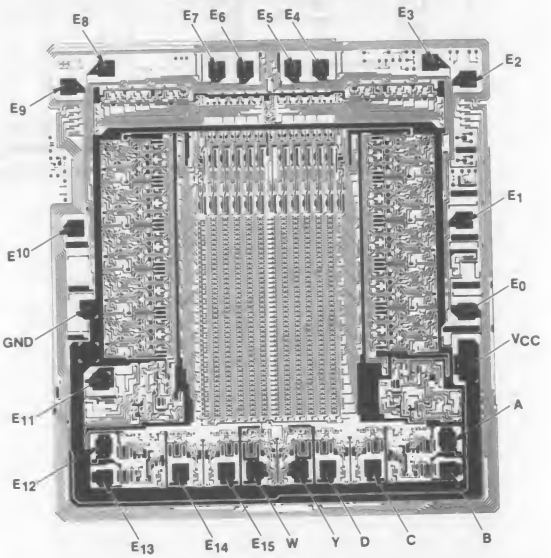
The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C, and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Function Table

INPUT SELECT				OUTPUT	
				W	Y
D	C	B	A		
L	L	L	L	$\overline{E0}$	E0
L	L	L	H	$\overline{E1}$	E1
L	L	H	L	$\overline{E2}$	E2
L	L	H	H	$\overline{E3}$	E3
L	H	L	L	$\overline{E4}$	E4
L	H	L	H	$\overline{E5}$	E5
L	H	H	L	$\overline{E6}$	E6
L	H	H	H	$\overline{E7}$	E7
H	L	L	L	$\overline{E8}$	E8
H	L	L	H	$\overline{E9}$	E9
H	L	H	L	$\overline{E10}$	E10
H	L	H	H	$\overline{E11}$	E11
H	H	L	L	$\overline{E12}$	E12
H	H	L	H	$\overline{E13}$	E13
H	H	H	L	$\overline{E14}$	E14
H	H	H	H	$\overline{E15}$	E15

Die Configuration

Die size: 140 x 131 mil



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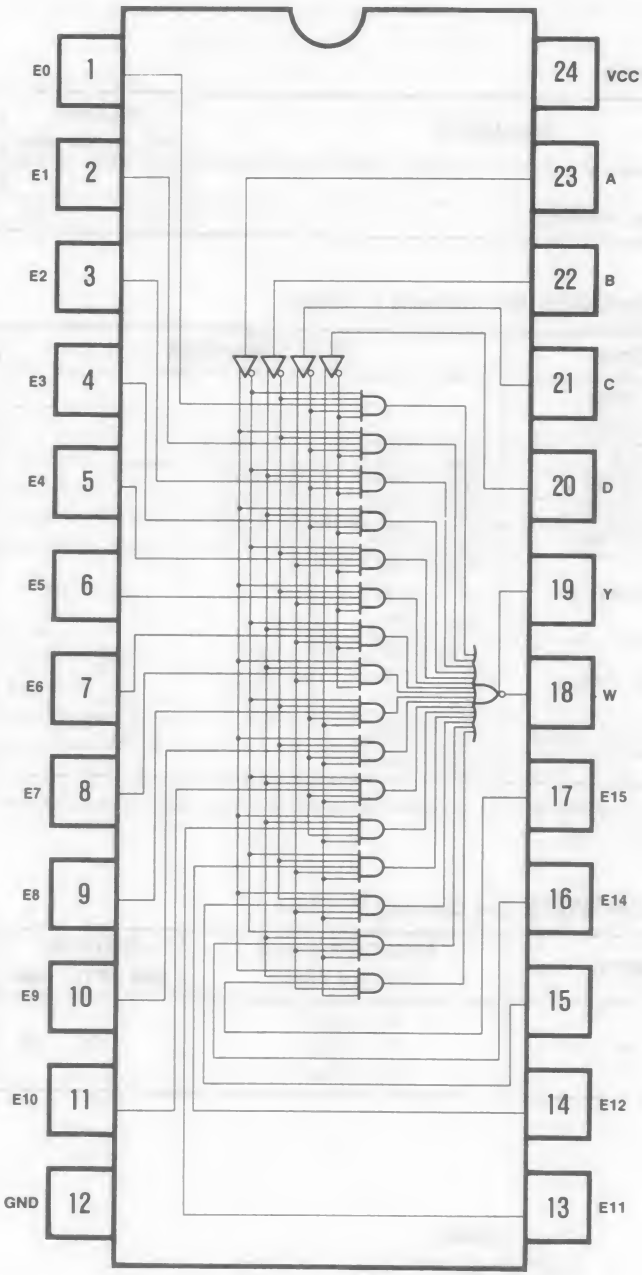
Monolithic Memories

Logic Diagram

16:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

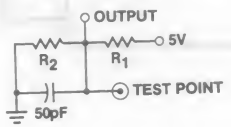
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

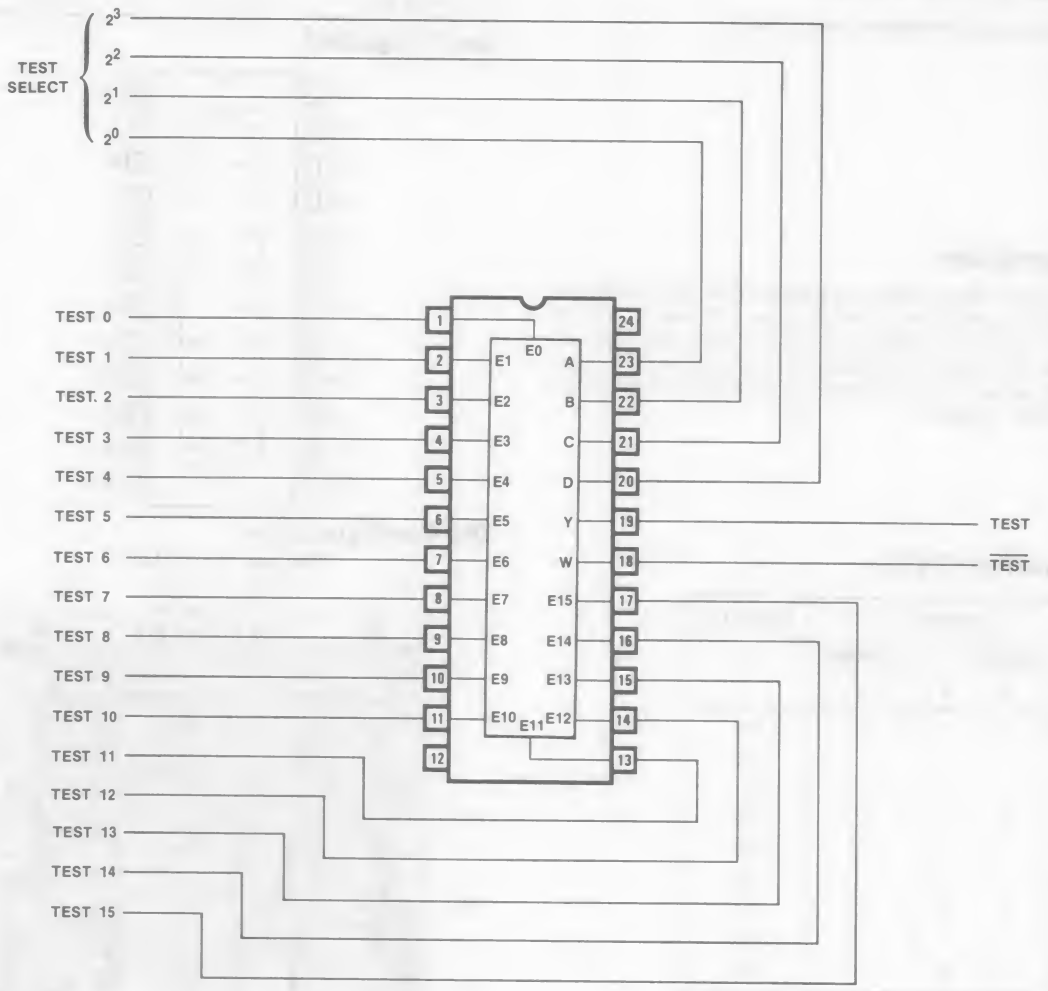
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y or W	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Standard Test Load



Application

Test Condition Mux



8

Dual 8:1 Mux
SN54/74LS451

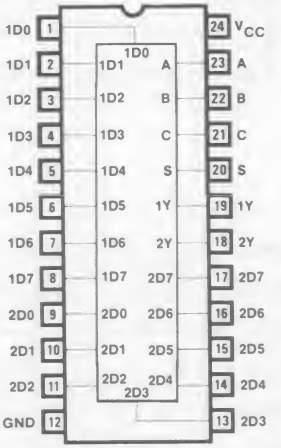
Features/Benefits

- 24-pin SKINNYDIP™ saves space
- Twice the density of 74LS151
- Low current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKAGE		TEMPERATURE
SN54L[illegible]51	JS, F	28L	MIL
SN74LS451	NS, JS		COM

Logic Symbol



Description

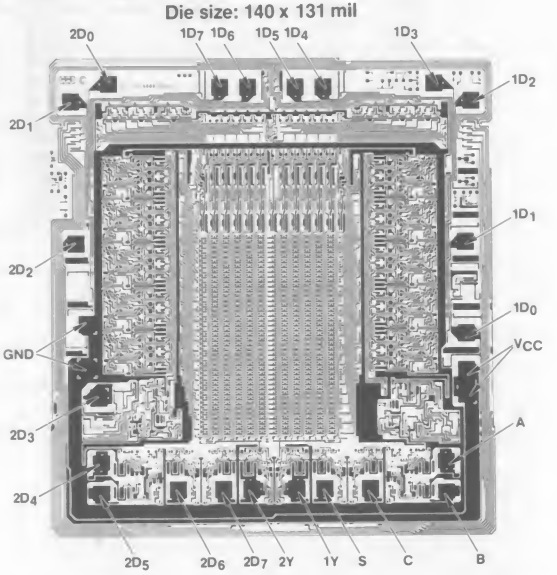
The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B, and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Function Table

INPUTS				OUTPUTS
SELECT			STROBE	Y
C	B	A	S	
X	X	X	H	H
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

Die Configuration

Die size: 140 x 131 mil



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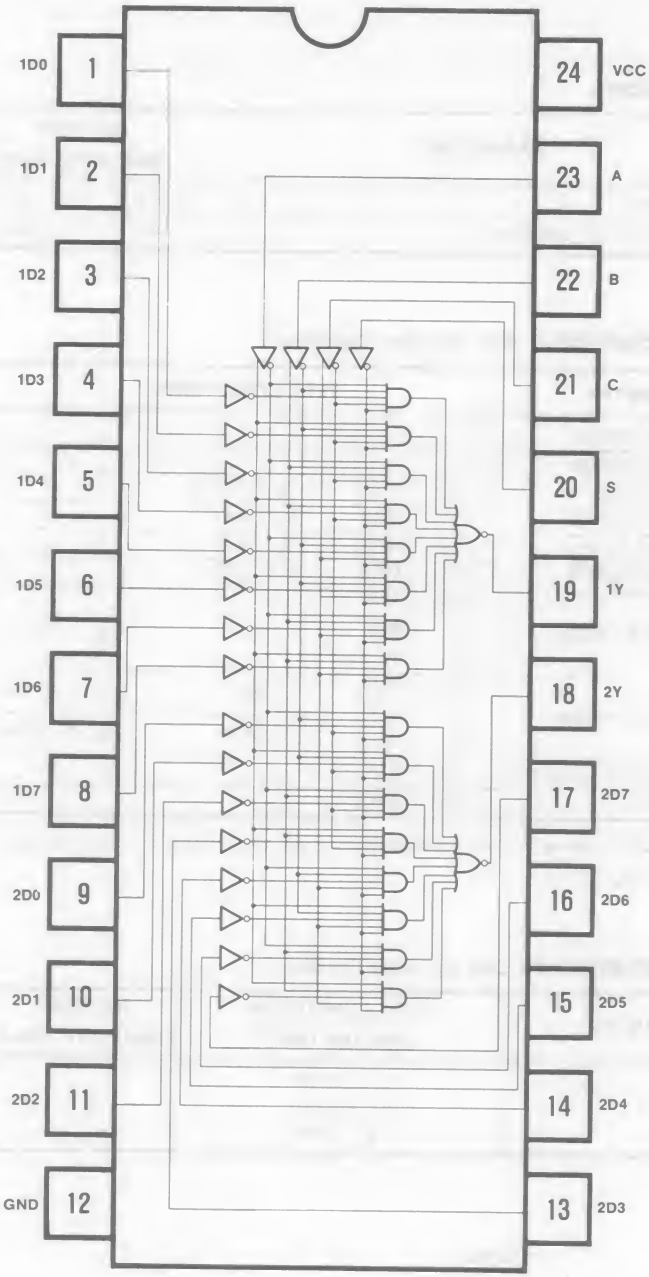
Monolithic Memories

Logic Diagram

Dual 8:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

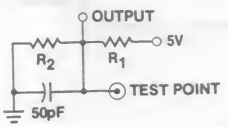
* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

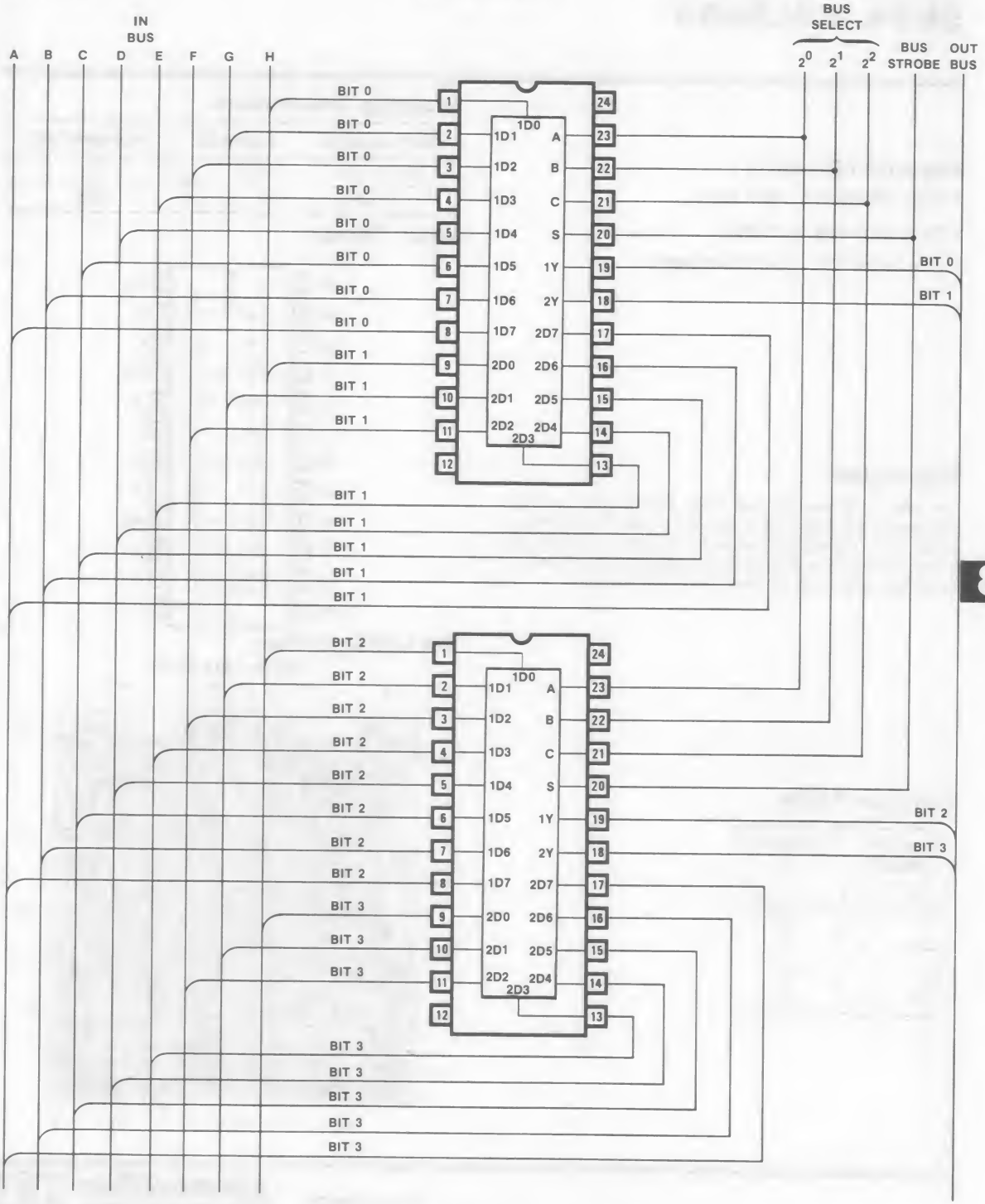
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Standard Test Load



Application

8:1 Bus Select



Quad 4:1 Mux
SN54/74LS453

Features/Benefits

- 24-pin SKINNYDIP™ saves space
- Twice the density of 74LS153
- Low current PNP inputs reduce loading

Description

The quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

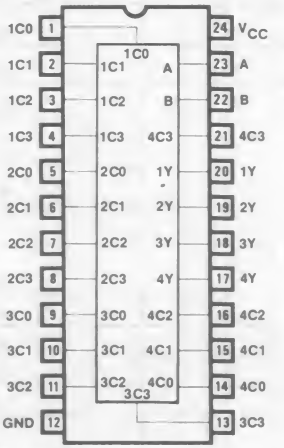
Function Table

INPUT SELECT		OUTPUTS Y
B	A	
L	L	C0
L	H	C1
H	L	C2
H	H	C3

Ordering Information

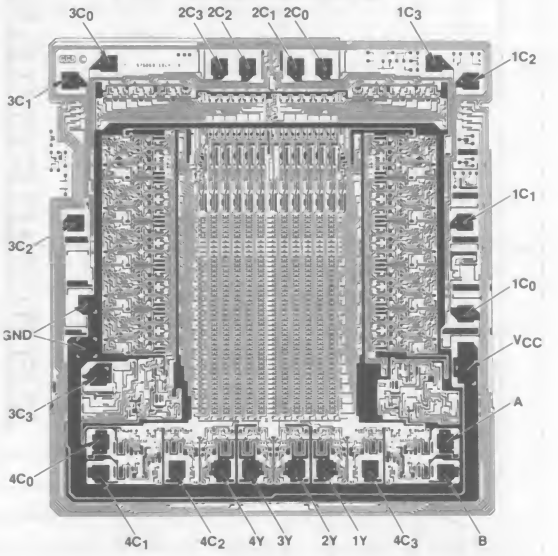
PART NUMBER	PACKAGE		TEMPERATURE
SN54LS453	JS, F	28L	MIL
SN74LS453	NS, JS		COM

Logic Symbol



Die Configuration

Die size: 140 x 131 mil



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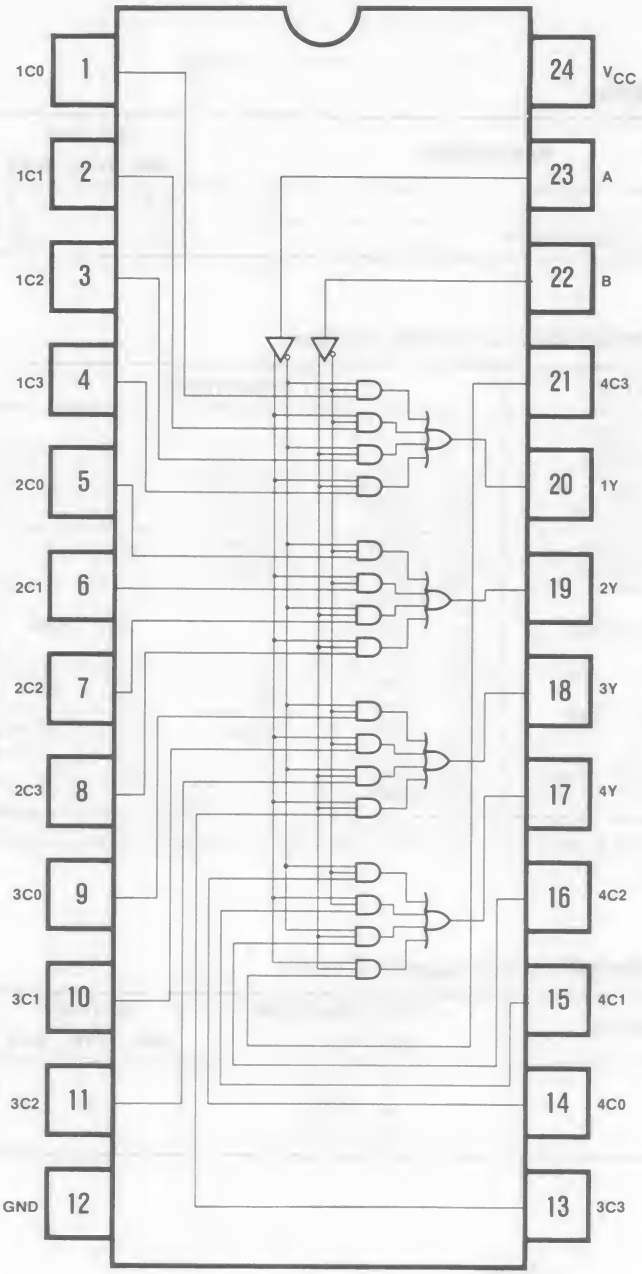
TWX: 910-338-2376

Monolithic Memories

Logic Diagram

Quad 4:1 Mux



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

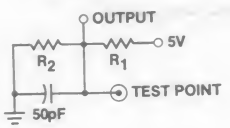
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

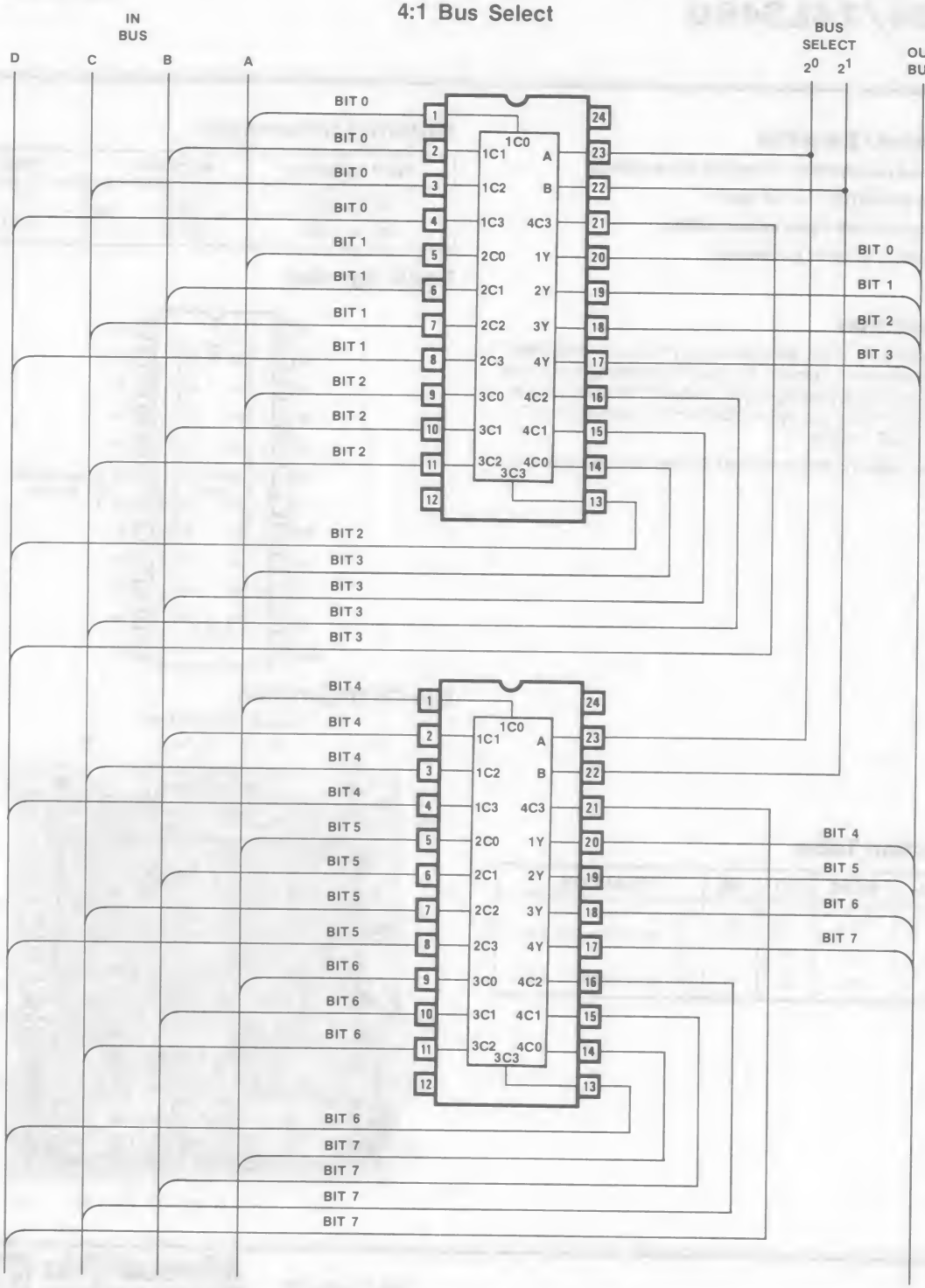
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Standard Test Load



Application

4:1 Bus Select



10-Bit Comparator
SN54/74LS460

Features/Benefits

- True and complement comparison status outputs
- 24-pin SKINNYDIP™ saves space
- Low current PNP inputs reduce loading
- Expandable in 10-bit increments

Description

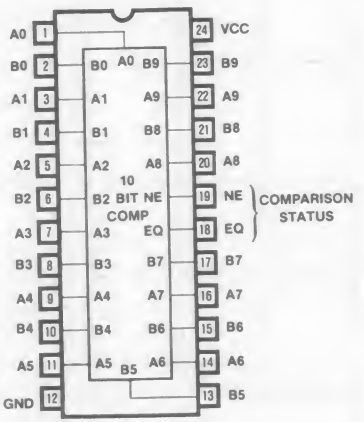
The'LS460 is an 10-bit comparator with true and complement comparison status outputs. The device compares two 10-bit data strings (A_9-A_0 and B_9-B_0) to establish if this data is Equivalent (EQ = HIGH and NE = LOW) or Not Equivalent (EQ = LOW and NE = HIGH).

Outputs conform to the usual 8mA LS totem-pole drive standard.

Ordering Information

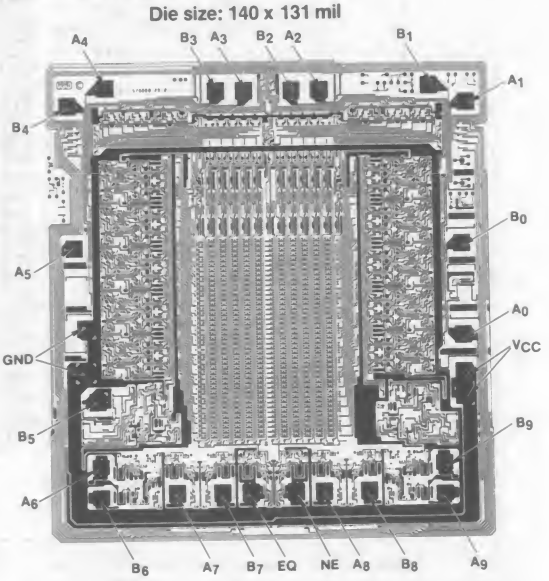
PART NUMBER	PACKAGE		TEMP
SN54LS460	JS, F	28L	MIL
SN74LS460	NS, JS		COM

Logic Symbol



Die Configuration

Die size: 140 x 131 mil



Function Table

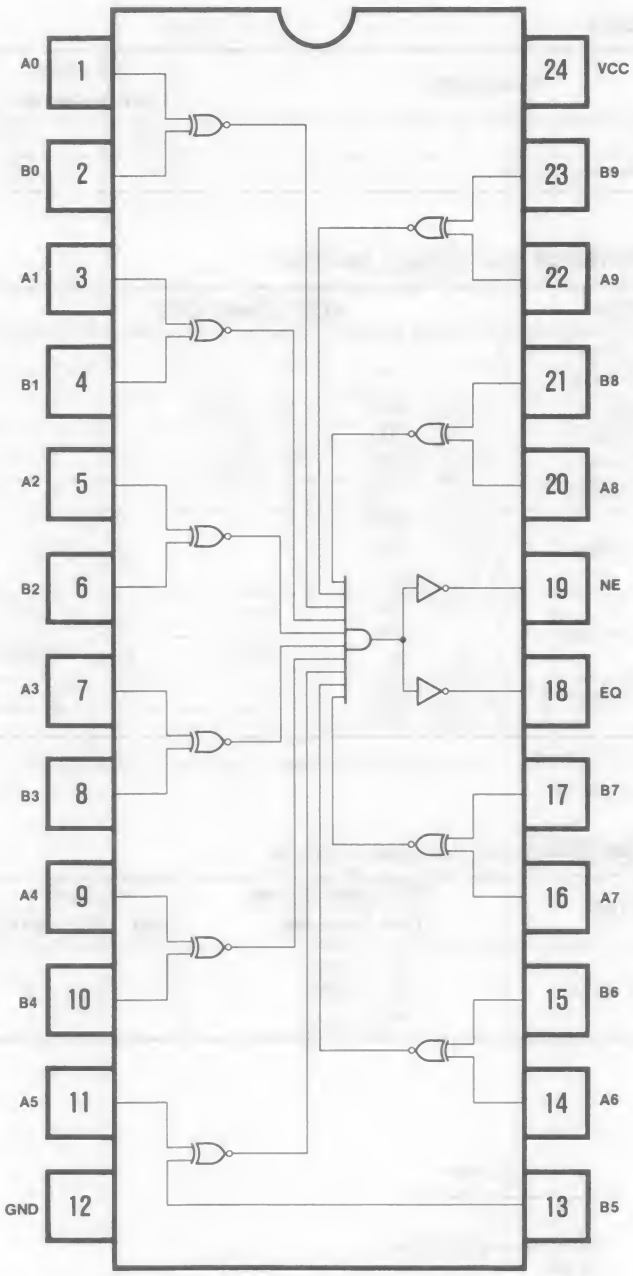
A9-A-	B9-B0	EQ	NE	OPERATION
A	A	H	L	Equivalent (A = B)
B	B	H	L	
A	B	L	H	Not Equivalent (A ≠ B)

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Logic Diagram

10-Bit Comparator



Absolute Maximum Ratings

Supply voltage V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

* Case temperature

Electrical Characteristics Over Operating Conditions

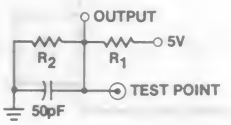
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

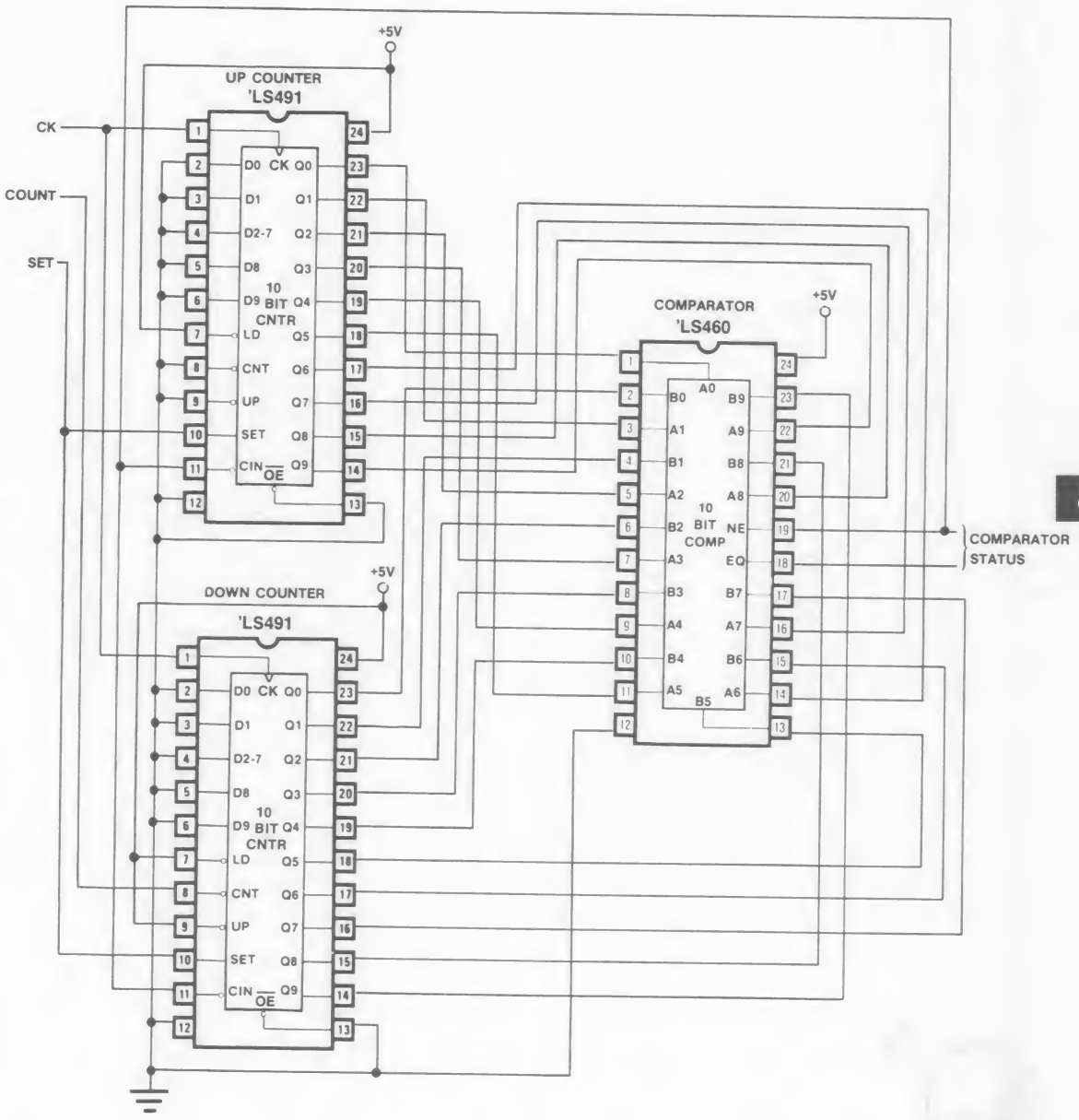
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Any input to EQ or NE	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Standard Test Load

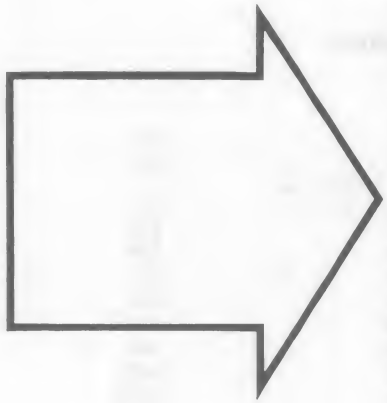


Application

10-Bit Up Counter/Down Counter Comparator




IMPORTANT
NOTES



The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

First-In First-Out (FIFO)

ORGANIZATION	FREQUENCY	CASCADABLE	STAND ALONE
COM 64x4	16.7 MHz	C67401B	67401B
COM 64x5	16.7 MHz	C67402B	67402B
COM 64x4	15 MHz	C67401A	67401A
COM 64x5	15 MHz	C67402A	67402A
COM 64x4	10 MHz	C67401	67401
COM 64x5	10 MHz	C67402	67402
MIL 64x4	10 MHz	C57401A	57401A
MIL 64x5	10 MHz	C57402A	57402A
MIL 64x4	7 MHz	C57401	57401
MIL 64x5	7 MHz	C57402	57402
COM 64x4	5 MHz	67L401	67L401

Contents

FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than other system components, but often operate with severly degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 Monolithic Memories FIFOs in particular.

What is a FIFO?

FIFO is one of those made-up words, or *acronyms*, formed from the initials of a phrase — in this case, "*F*irst-*I*n, *F*irst-*O*ut." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a *queue discipline* which may be applied to the processing of the elements of any *queue* or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel — "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices for coins which handle the coins in this same manner. (See Figure 1.)

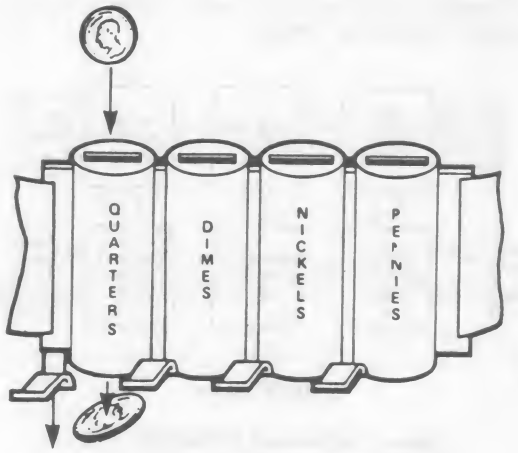


Figure 1. Primitive Mechanical FIFO Device

Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an *asynchronous* FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/output programming practice, a FIFO memory region is sometimes referred to as a *circular buffer*, and in programming for computer-controlled telephone systems it is called a *hopper*. A LIFO memory region is usually referred to as a *stack*.

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type 67401 64x4 FIFO and type 67402 64x5 FIFO which have been available for several years from Monolithic Memories. ("64x4" here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:

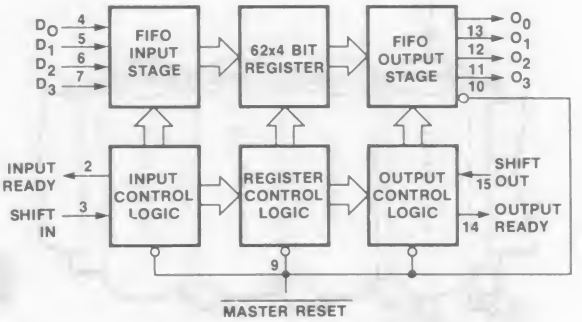


Figure 2. Architecture of the 67401 FIFO

The list of signals/pins for the 67401 is:

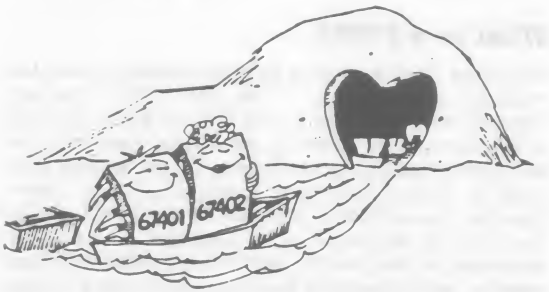
TYPE	HOW MANY	(CUM.)	I/O/V
Data In	4	4	I
Output	4	8	O
Control:			
Shift In	1	9	I
Shift Out	1	10	I
Master Reset	1	11	I
Status:			
Input Ready	1	12	O
Output Ready	1	13	O
Not Connected	1	14	—
Voltage:			
V_{CC} (+5V)	1	15	V
Ground	1	16	V

The corresponding list for the 67402 differs only in that there are 5 Data In lines rather than 4, and 5 Output lines rather than 4. The reason that there is an unused pin is that the 67401 was originally designed as a faster bipolar upgrade of a MOS part, the Fairchild 3341, which needs a second power-supply voltage (-12V) as well as V_{CC}. Much of the description to be given here of the 67401 also applies to the 3341, except for data rate — the 67401 can operate at 10-16.7 MHz depending on the exact version, compared with approximately 1 MHz for the 3341. Pinouts are as indicated in the data sheet.

The reason for having a 5-bit model as well as a 4-bit model of basically the same part is that if two 4-bit FIFOs are placed side-by-side they make only an 8-bit FIFO, and many people have FIFO applications which entail using a parity bit with each byte and/or a frame-marker bit with the last byte of a frame or block, which means that they want 9-bit or 10-bit FIFOs. A 67402 next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.

A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted. Likewise, a logic High on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data In lines (the *top* of the FIFO, as it were), this word automatically *sinks all the way to the bottom* (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym *hopper*?) In keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn *only* in the order in which they were originally inserted.

There is no provision for *random access* in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO *from a magnetic-tape* perspective. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.



"'FIRST-IN, FIRST-OUT' . . . DESCRIBES A QUEUE DISCIPLINE WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE . . ."

We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00, the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01, the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest vacant word in the FIFO — the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO — word 63 — has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequences of this manner of operation in shift-register-technology FIFOs is that it takes quite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402, rated at 7, 10, 15, or 16.7 MHz over commercial (0°C to + 75°C) or military (-55°C to + 125°C) temperature ranges. Thus, for instance, a 16.7-MHz FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 60 nanoseconds. However, the "fall-through time t_{PT} for these same FIFOs is stated in the data sheet as 1.3 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00, which should be identical to t_{PT}, and probably is although as *measured* on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement. By the way, the stated operating frequencies and the t_{PT} value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice.

Besides Monolithic Memories, other manufacturers of bipolar (fast) FIFOs include Fairchild Semiconductor, MosTek, National Semiconductor, RCA, Texas Instruments, and TRW LSI Products. MOS (slow) FIFOs are available from Advanced Micro Devices, Fairchild Semiconductor, Texas Instruments, Western Digital, Zilog, and probably other firms. FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well as parallel data ports, and additional status flags. For instance, Monolithic Memories has a FIFO in development which has a "half-full" flag which tells when half of the FIFO's words contain data, and also a second flag which indicates that the FIFO is either "almost full" (within 8 words of full) or "almost empty" (within 8 words of empty),reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that *some* action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap around" from the highest RAM address back to zero. The out-pointer chases the in-pointer, the region just traversed by the in-pointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other — unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be quite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of full-blown binary counters. What this means in practice is that there are now *two* extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small (16x4) bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fall-through time but needs proportionally more silicon area to store a given number of bits.

Designing with FIFOs

Returning now to the Monolithic Memories 67401 and 67402, if what you *really* need is a "deeper" FIFO, say 128x4 instead of just 64x4, these parts are designed to *cascade* using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift In control input of FIFO B is connected to the Output Ready status output of FIFO A, and likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 3.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.

"...THE MONOLITHIC MEMORIES C67401 AND C67402...ARE DESIGNED TO CASCADE USING A SIMPLE 'HANDSHAKING' PROCEDURE..."

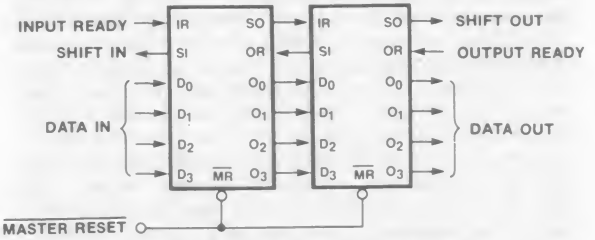


Figure 3. Cascading FIFOs to Form 128x4 FIFO

If what you *really* need is a "wider" FIFO, then you simply arrange 64x4 or 64x5 FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74S08 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 12 in the FIFO data sheet.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array — and if you chose wrongly, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungus number of 67401s and 67402s are in use world-wide giving hassle-free service, it should be kept in mind that these devices are *asynchronous sequential circuits*. (One definition of "asynchronous sequential circuit" is "a fortuitous collection of race conditions," but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setup-time and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a $\overline{\text{Master Reset}}$. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be *told* to issue a $\overline{\text{Master Reset}}$ as part of your power-up sequence.) In the event that you still get what appear to be occasional errors, very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to ground will often eliminate these. But by all means start with a *good* circuit board — these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1-microfarad disk capacitors between V_{CC} and ground for each chip to bypass switching noise.

The sequence of events which occurs during the operation of shifting a new data word into the "top" of a FIFO is shown in Figure 3 in the FIFO data sheet, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 7 in the FIFO data sheet. In both of these figures, it has been assumed that the external logic — whether it be the rest of your system, or just another FIFO — refrains from raising the respective Shift line to "High" until the respective Ready line has gone "High;" if the Shift line is raised any earlier, it simply gets ignored.

When two FIFOs are cascaded as shown in Figure 3, the sequences of events shown in data-sheet Figures 3 and 7 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 3 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using. FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider data-sheet Figures 3 and 7 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 or FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go "High," and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going "High." Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from data-sheet Figure 3 that the conditions for inputting a word into FIFO B have now been met, and from data-sheet Figure 7 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been met. The time delays shown in both data-sheet Figure 3 and data-sheet Figure 8 from the event at 2 to the event at 3, and from the event at 4 to the event at 5A, are asynchronous internal-logic-determined times of the order of 4 or 5 gate delays, where the gates in question are high-speed-Schottky LSI *internal* gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.

Returning now to applying the timing analysis shown in data-chart Figures 3 and 7 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in

the opposite sense (falling or rising, that is) for the Ready signal from the other part. The two signals, ORA/SIB (meaning "Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain High at the same time for more than a few nanoseconds, since if they are both High a data word will pass between the two FIFOs as already described. So, at the point when *both* the sequence of events shown in data-sheet Figure 3 and the sequence of events shown in data-sheet Figure 7 have been completed, and consequently ORA/SIB and IRB/-SOA have both gone High again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks Low, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks Low, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

Various Uses for FIFOs

The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter — it's all the same to an asynchronous FIFO such as the 67401 or 67402, as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modus operandi is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic — or perhaps even a microprocessor — which is otherwise occupied most of the time.

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some way for the system to sense that all is not well and halt itself. Such a record of jumps can be very valuable in tracing out what happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt — perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO *per bit-stream* is required — but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.

References (1), (2), and (3) are formal applications notes available from Monolithic Memories, which discuss FIFOs from different viewpoints than this paper has taken. Each of them presents a more detailed explanation of one or more applications than there has been room for here. Reference (1) is mainly an overall applications survey, reference (2) emphasizes digital communications, and reference (3) emphasizes digital spectrum analyzers and also includes an overview of digital signal processing in general.

"A LESS OBVIOUS BUT INTERESTING APPLICATION OF FIFOS IS AS AUTOMATIC 'BUS-WATCHERS' . . ."

References

(1) "First IN First Out Memories...Operations and Applications," applications note published March 1978 by Monolithic Memories, Inc and being reissued.

(2) "Understanding FIFO's," applications note published by Monolithic Mem ories, Inc. The author, Alan Weissberger, has also now gotten a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in *Electronic Design*, November 27, 1981. Despite the general title, the emphasis is on digital communications applications.

(3) "PROMs, PALs, FIFOs and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories, Inc. The author, Richard Wm. Blasco, also got this note published in *Electronic Design* in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.

First-In First-Out (FIFO) 64x4 64x5 Cascadable Memory

C5/67401 C5/67401A C67401B
C5/67402 C5/67402A C67402B

Features/Benefits

- Choice of 16.7, 15, and 10 MHz shift out/shift in rates
- Choice of 4 bit or 5 bit data width
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

The C5/C67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

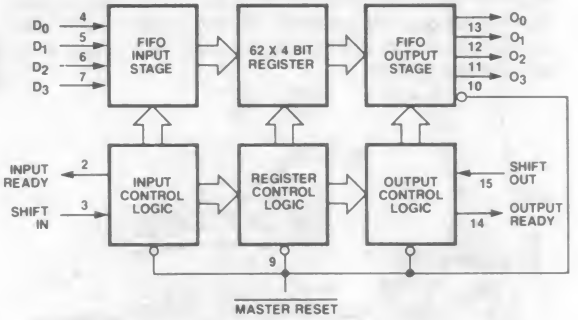
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C57401	J, F, L,* N	MIL	7 MHz 64x4 FIFO
C67401	J, N	COM	10 MHz 64x4 FIFO
C57402	J, F, L,* N	MIL	7 MHz 64x5 FIFO
C67402	J, N	COM	10 MHz 64x5 FIFO
C57401A	J, F, L,*	MIL	10 MHz 64x4 FIFO
C67401A	J	COM	15 MHz 64x4 FIFO
C57402A	J, F, L,*	MIL	10 MHz 64x5 FIFO
C67402A	J	COM	15 MHz 64x5 FIFO
C67401B	J	COM	16.7 MHz 64x4 FIFO
C67402B	J	COM	16.7 MHz 64x5 FIFO

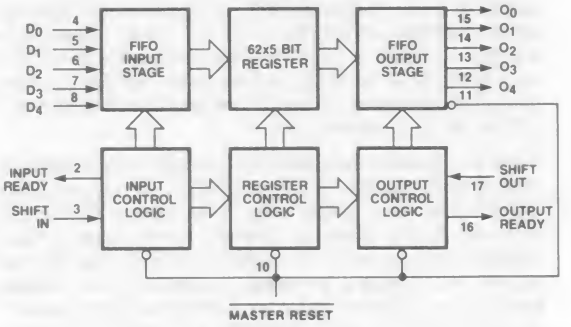
* LCC — contact the factory

Block Diagrams

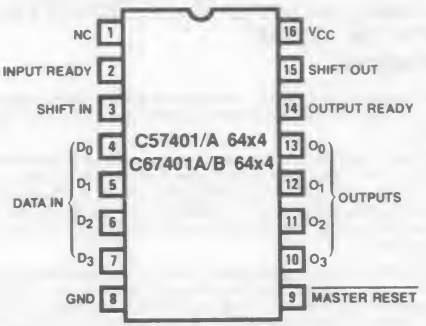
C57401/A 64x4
C67401A/B 64x4

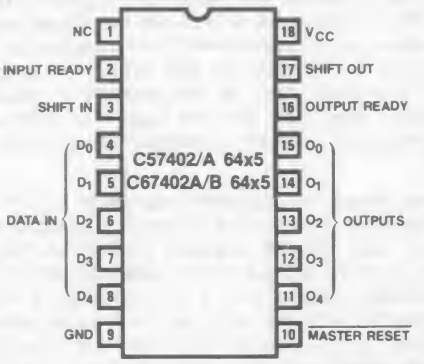


C57402/A 64x5
C67402A/B 64x5



Pin Configurations





2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −.5V to 7V
Input voltage ..... −1.5V to 7V
Off-state output voltage ..... −.5V to 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions C67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data set up	1	0			ns
t_{IDH}	Input data hold time	1	45			ns
t_{SOH}†	Shift Out HIGH time	5	18			ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

* Case temperature.

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Switching Characteristics C67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to Input Ready LOW	1			35	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			44	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.3	μs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

†See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... —.5V to 7V
Input voltage ..... —1.5V to 7V
Off-state output voltage ..... —.5V to 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions C5/C67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY A			COMMERCIAL A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23			ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data set up	1	0			0			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23			ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

Switching Characteristics C5/C67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY A			COMMERCIAL A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	30			30			ns
t_{OPH}*	Output Ready pulse HIGH	8	30			30			ns

† See AC test and High Speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −.5V to 7V
Input voltage ..... −1.5V to 7V
Off-state output voltage ..... −.5V to 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions C5/C67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data set up	1	0			0			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			35			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature

Switching Characteristics C5/C67401/2

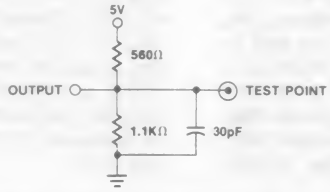
Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			60			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			4			3	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	30			30			ns
t_{OPH}*	Output Ready pulse HIGH	8	30			30			ns

† See AC test and High Speed application note.

*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Standard Test Load



Input Pulse 0 to 3V
Input Rise and Fall Time (10% - 90%)
2 - 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open	C5/67401			160	mA
				C5/67402			180	
				C5/67401A			170	
				C5/67402A			190	
				C67401B			180	
				C67402B			200	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App.Notes

Since the FIFO ia a very high speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. MMI recommends a monolithic ceramic capacitor of 0.1μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift In pulse is not recognized until Input Ready is High. If Input Ready is not high due to (a) too high a frequency, (b) too wide a Shift In pulse at that frequency, or (c) FIFO being full or effected by Master Reset, the Shift In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold Time (TIDH) and the next activity of Input Ready (TIRL) to be extended relative to Shift ingoing High. This same type of problem is also related to TIRH, TORL and TORH as related to Shift Out.

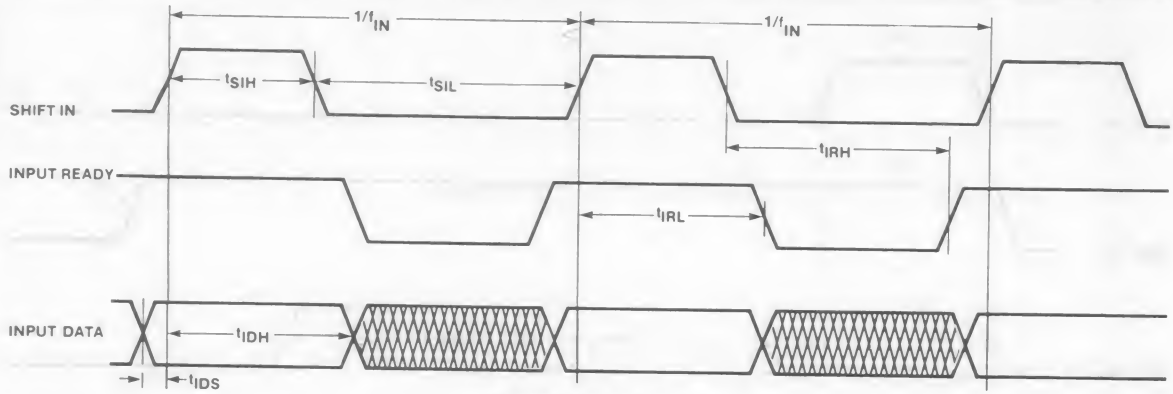


Figure 1. Input Timing

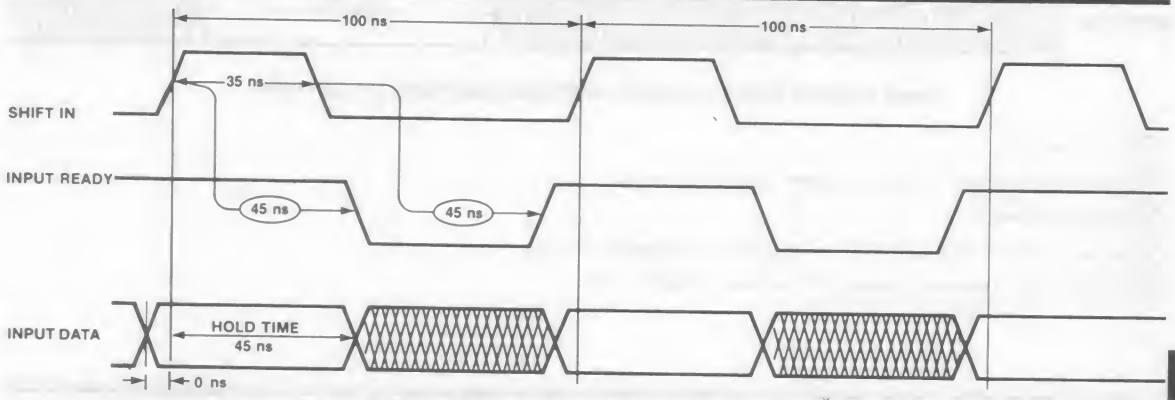


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

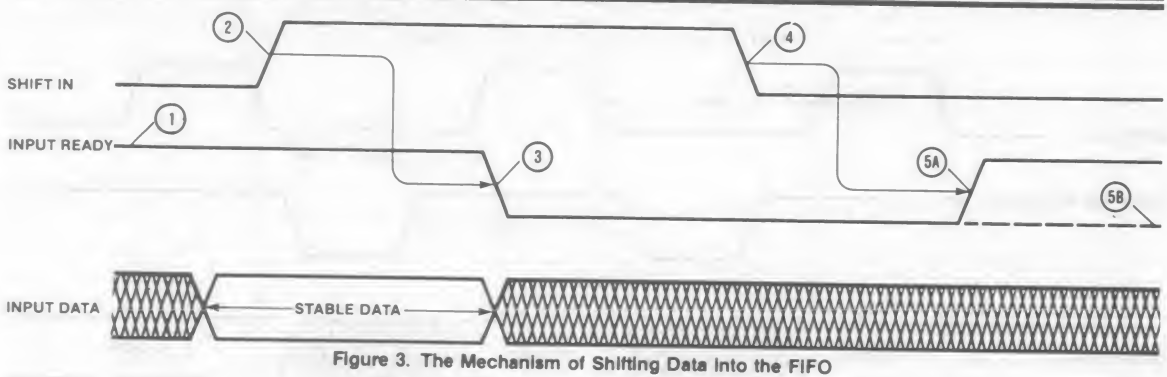


Figure 3. The Mechanism of Shifting Data Into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied

(2) Input Data is loaded into the first word

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 4).

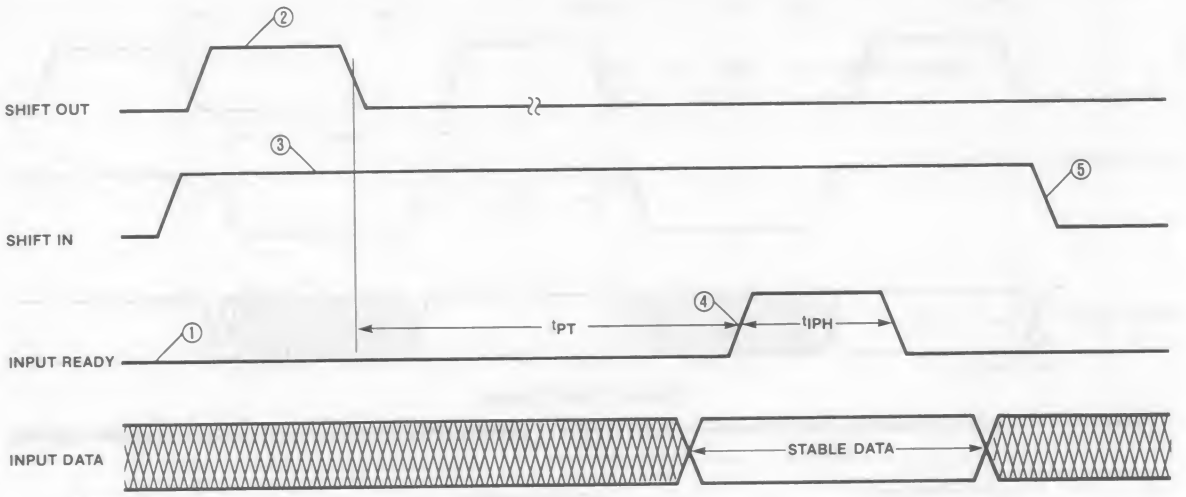


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

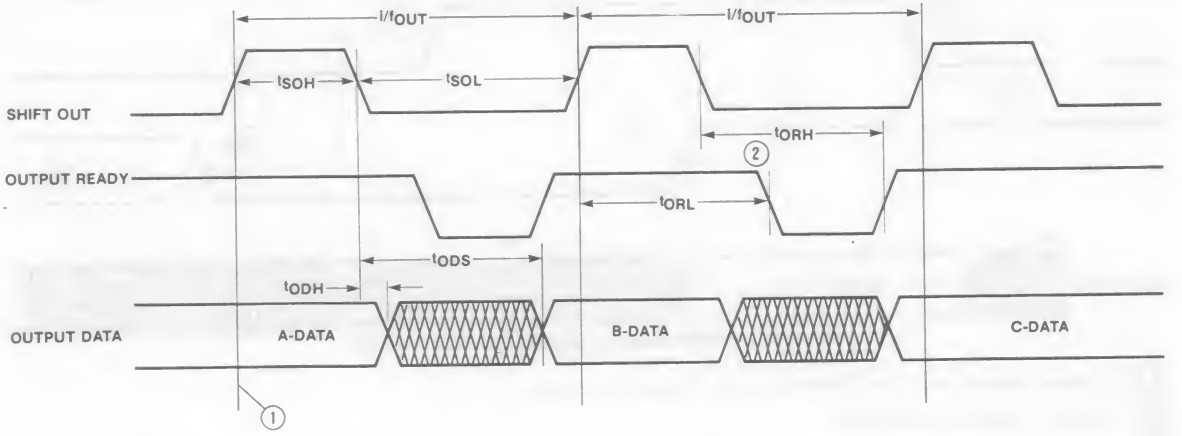
(1) FIFO is initially full

(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.

(3) Shift In is held HIGH

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word

(5) The Data from the first word is released for "fall through" to second word



(1) The diagram assumes that at this time words 63, 62, 61 are loaded with A, B, C Data respectively

(2) Data is Shifted Out when Output Ready is HIGH and Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

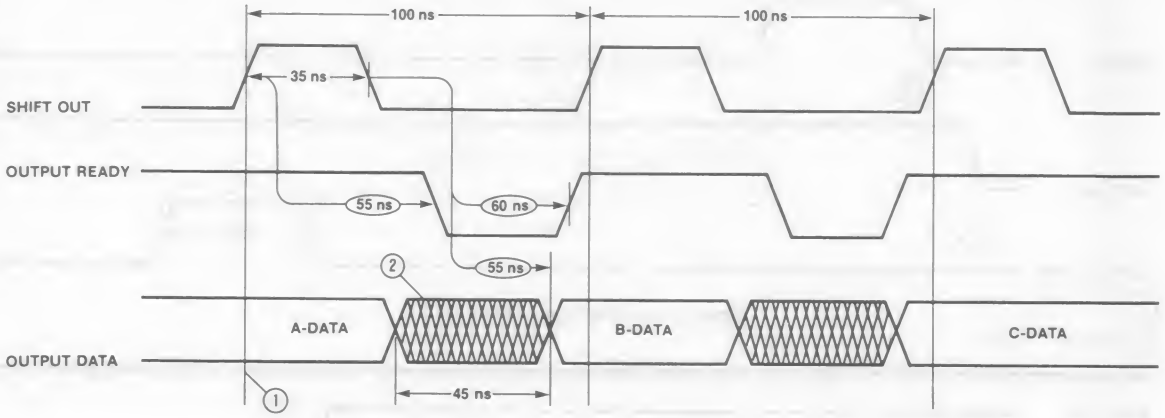


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

(2) Data in the crosshatched region may be A or B Data.

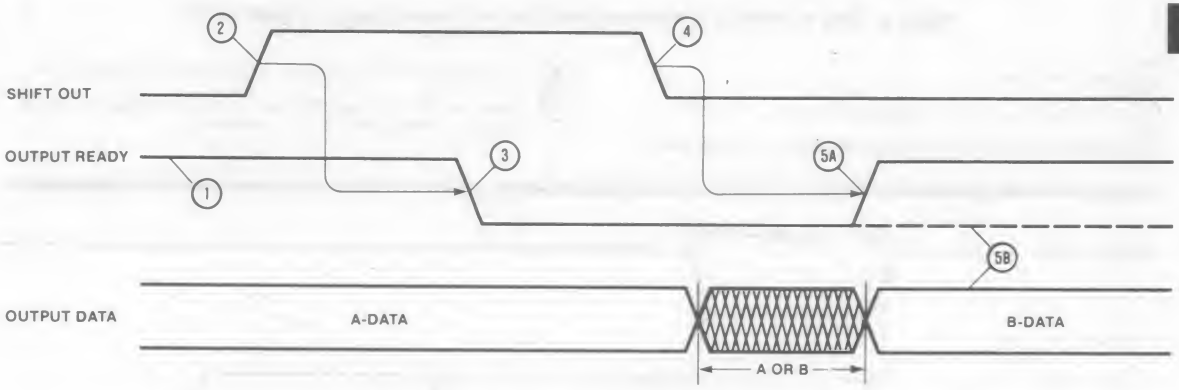


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied

(2) Shift Out goes HIGH causing the next step.

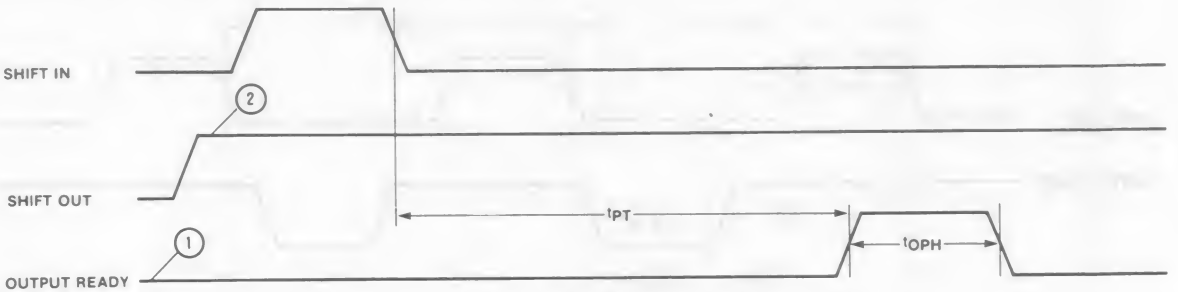
(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.



1. FIFO initially empty.
2. Shift Out held HIGH.

Figure 8. t_{PT} and t_{OPH} Specification

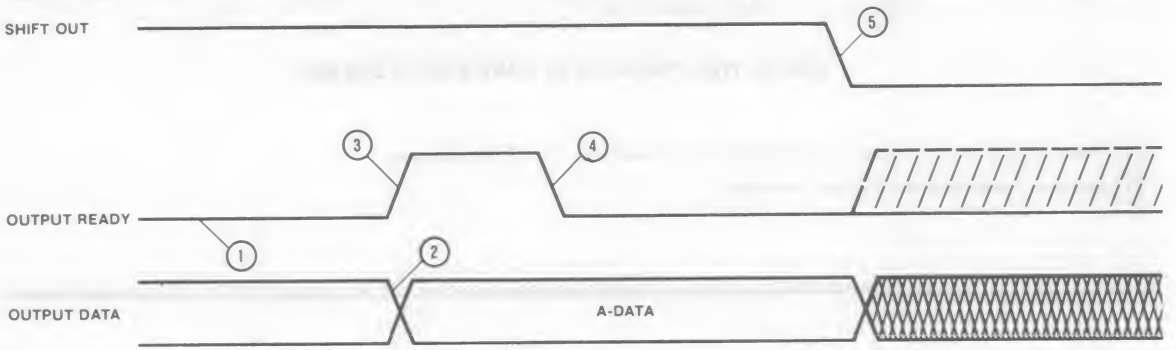
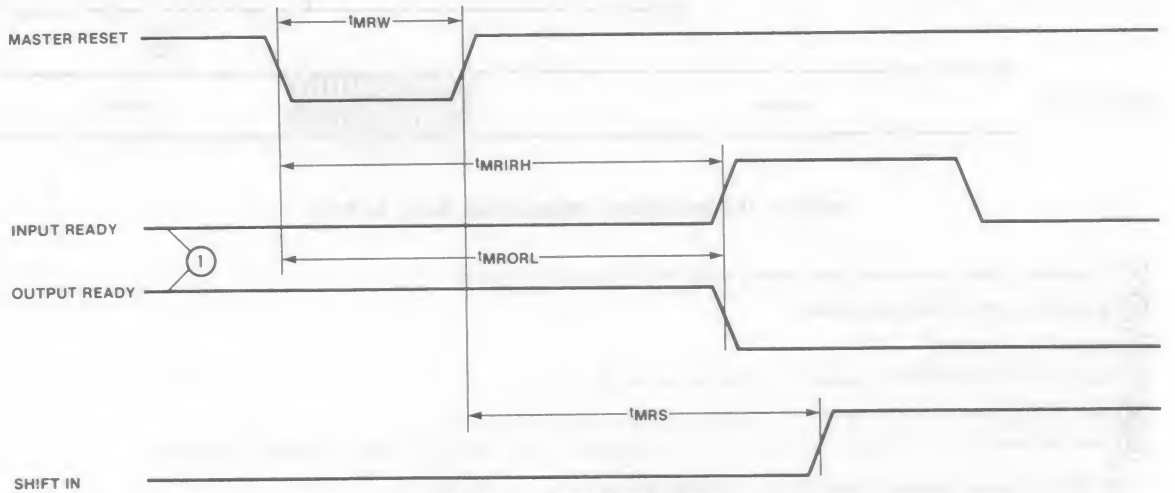


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH. Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1. FIFO initially full.

Figure 10. Master Reset Timing

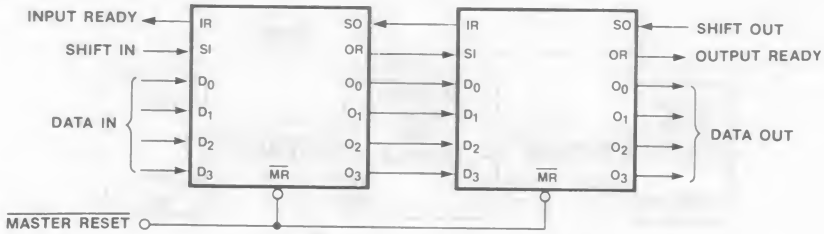


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

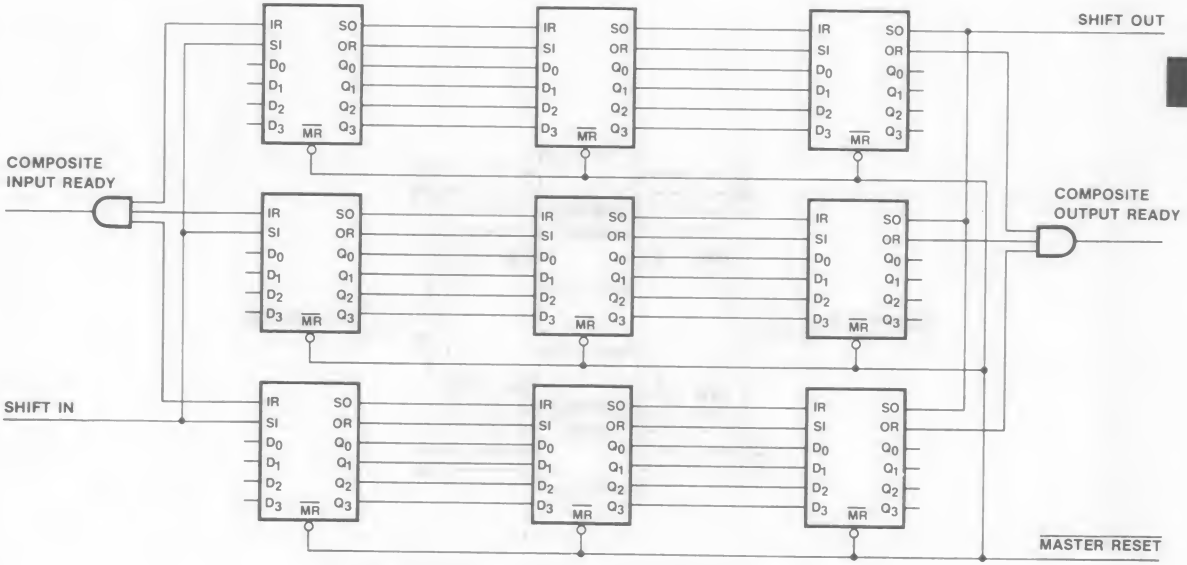
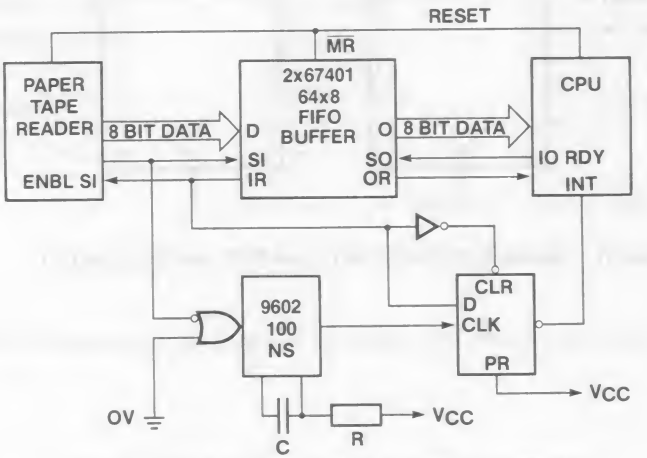


Figure 12. 192x12 FIFO with C5/C67401/1A/1B

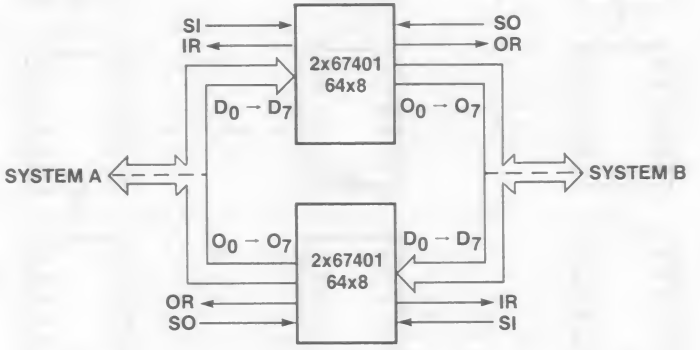
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

Applications



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

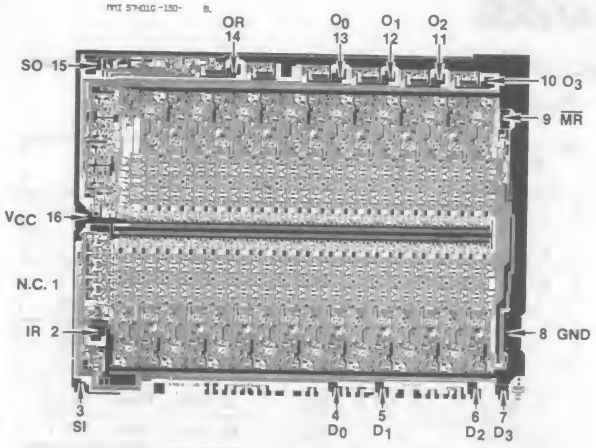
Figure 13. Slow Steady Rate to Fast "Blocked" Rate

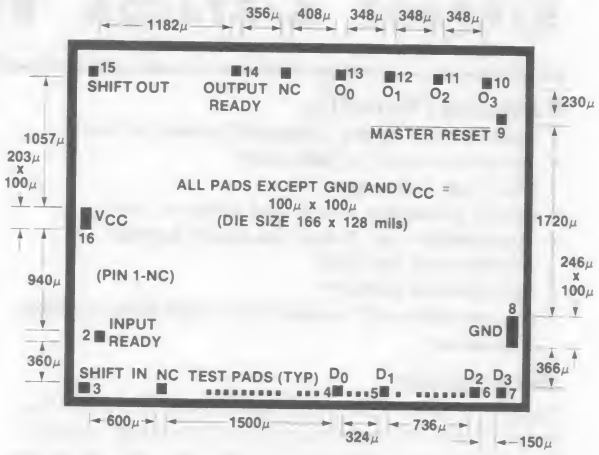


NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

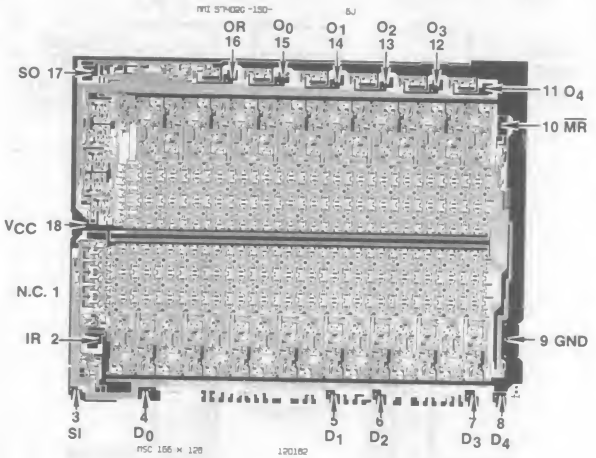
Figure 14. Bidirectional FIFO Application

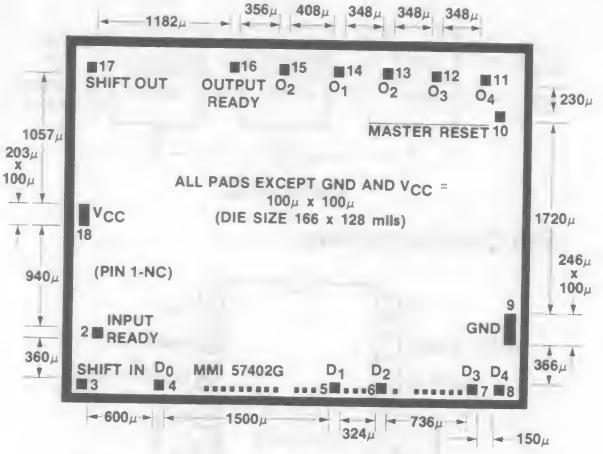
57401 Die Pattern
Step: G
Size: 128x166 mils





57402 Die Pattern
Step: G
Size: 128x166 mils





9

First-In First-Out (FIFO) 64x4 64x5
Standalone Memory

5/67401 5/67401A 67401B
5/67402 5/67402A 67402B

Features/Benefits

- Choice of 16.7, 15, and 10 MHz shift out/shift in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

The 5/67401B/2B/1A/2A/1/2 are "fall-through" high speed First-in First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

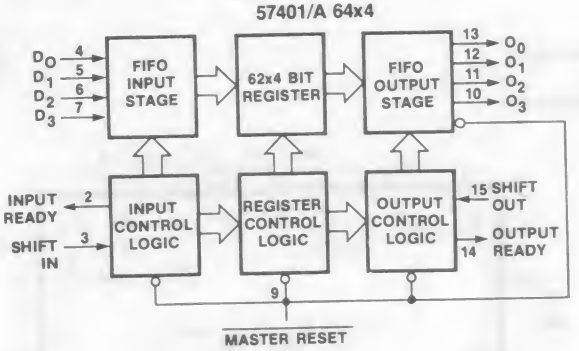
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
57401	J, F, L, *N	MIL	7 MHz 64x4 FIFO
67401	J,N	COM	10 MHz 64x4 FIFO
57402	J, F, L, *N	MIL	7 MHz 64x5 FIFO
67402	J,N	COM	10 MHz 64x5 FIFO
57401A	J, F, L,*	MIL	10 MHz 64x4 FIFO
67401A	J	COM	15 MHz 64x4 FIFO
57402A	J, F, L,*	MIL	10 MHz 64x5 FIFO
67402A	J	COM	15 MHz 64x5 FIFO
67401B	J	COM	16.7 MHz 64x4 FIFO
67402B	J	COM	16.7 MHz 64x5 FIFO

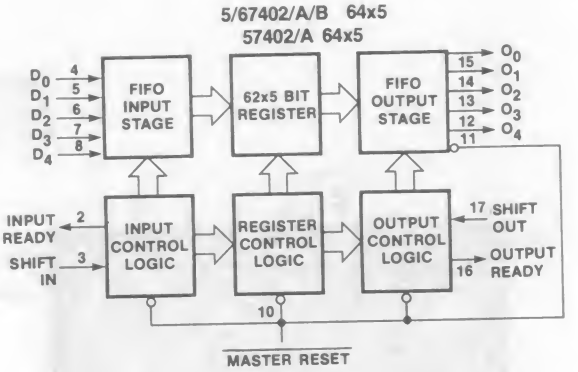
* LCC — contact the factory

Block Diagrams

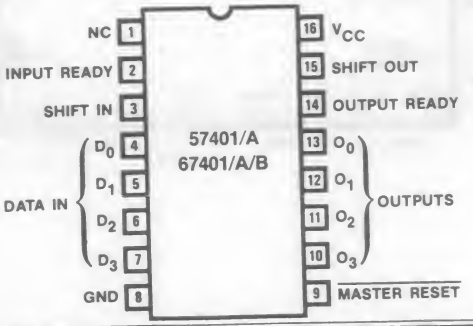
67401/A/B 64x4
57401/A 64x4

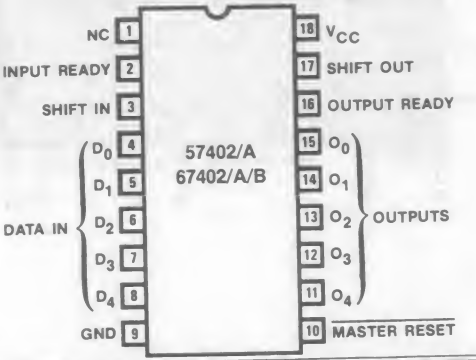


5/67402/A/B 64x5
57402/A 64x5



Pin Configurations





2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -1.5 to 7V
Input voltage ..... -1.5 to 7V
Off-state output voltage ..... -.5 to 5.5V
Storage temperature ..... -65° to +150°C

Operating Conditions 67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL A MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH} †	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data set up	1	5			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH} †	Shift Out HIGH time	5	18		20†	ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

* Case temperature.

9

Switching Characteristics 67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL A MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to input ready LOW	1			35	ns
t_{IRH}	Shift In to input ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL} †	Shift Out to Output Ready LOW	5			38	ns
t_{ORH} †	Shift Out to Output Ready HIGH	5			44	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4,8			1.3	μs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}	Input Ready pulse HIGH	4	15			ns
t_{OPH}	Output Ready pulse HIGH	8	15			ns

†See A.C Test and High Speed Application Note.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... —.5V to 7V
Input voltage ..... —1.5V to 7V
Off-state output voltage ..... —.5V to 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions 5/67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY A			COMMERCIAL A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23		28†	ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data set up	1	5			5			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23		28†	ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature

Switching Characteristics 5/67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY A			COMMERCIAL A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

† See AC test and High Speed application note.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -.5 to 7V
Input voltage ..... -1.5 to 7V
Off-state output voltage ..... -.5 to 5.5V
Storage temperature ..... -65° to +150° C

Operating Conditions 5/67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		-55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data set up	1	10			5			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			35			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse†	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature.

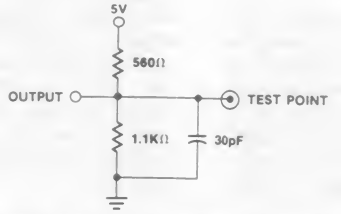
Switching Characteristics 5/67401/2

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to input ready LOW	1			60			45	ns
t_{IRH}†	Shift In to input ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4,8			4			3	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

†See AC test and high speed application note.

Standard Test Load



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% to 90%)
2 - 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0–D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open.	57/67401			160	
				5/67402			180	
				5/67401A			170	
				5/67402A			190	
				67401B			180	
				67402B			200	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second
†There are absolute voltages with respect to degree GND (PIN 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_x inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_x outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_x remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App.Notes

Since the FIFO ia a very high speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. MMI recommends a monolithic ceramic capacitor of 0.1μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift In pulse is not recognized until Input Ready is High. If Input Ready is not high due to (a) too high a frequency, (b) too wide a Shift In pulse at that frequency, or (c) FIFO being full or effected by Master Reset, the Shift In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold Time (TIDH) and the next activity of Input Ready (TIRL) to be extended relative to Shift ingoing High. This same type of problem is also related to TIRH, TORL and TORH as related to Shift Out.

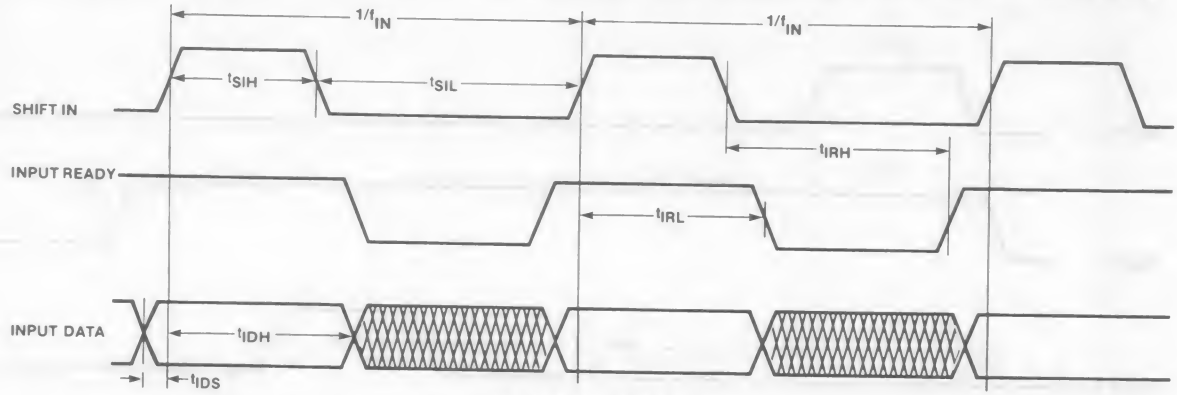


Figure 1. Input Timing

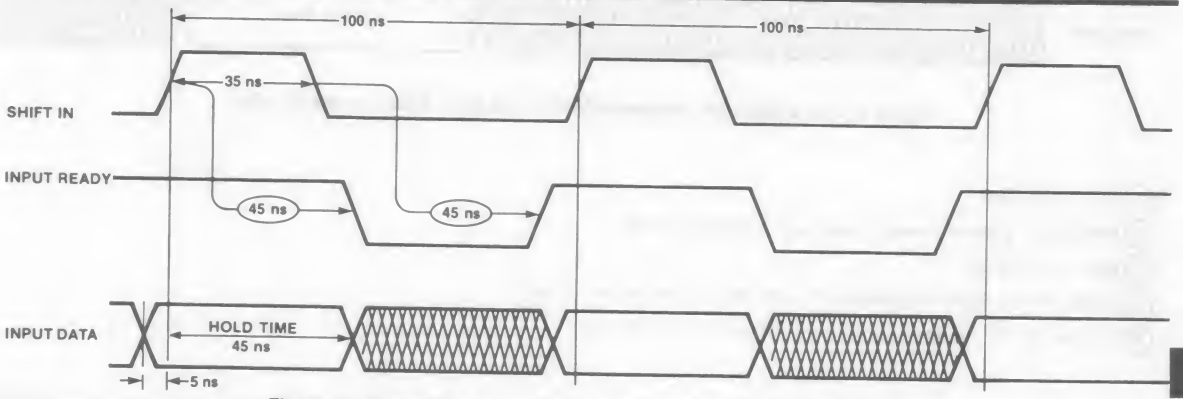


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)

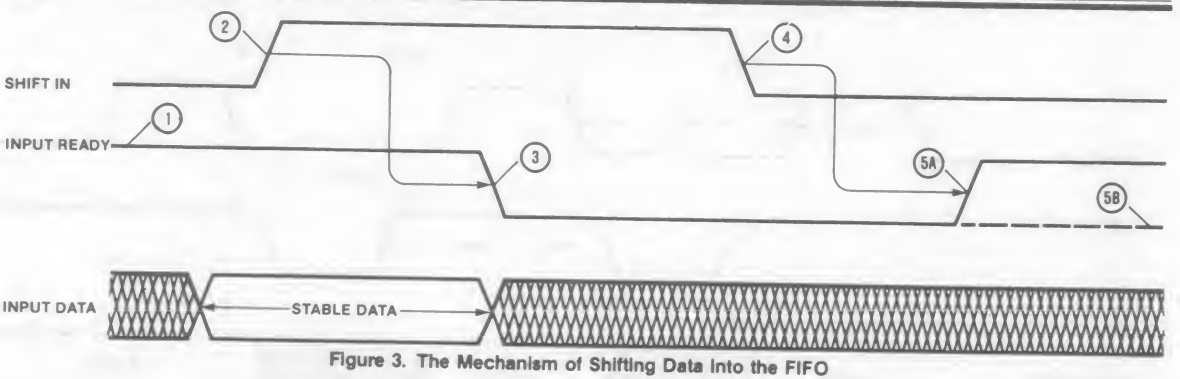


Figure 3. The Mechanism of Shifting Data Into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)

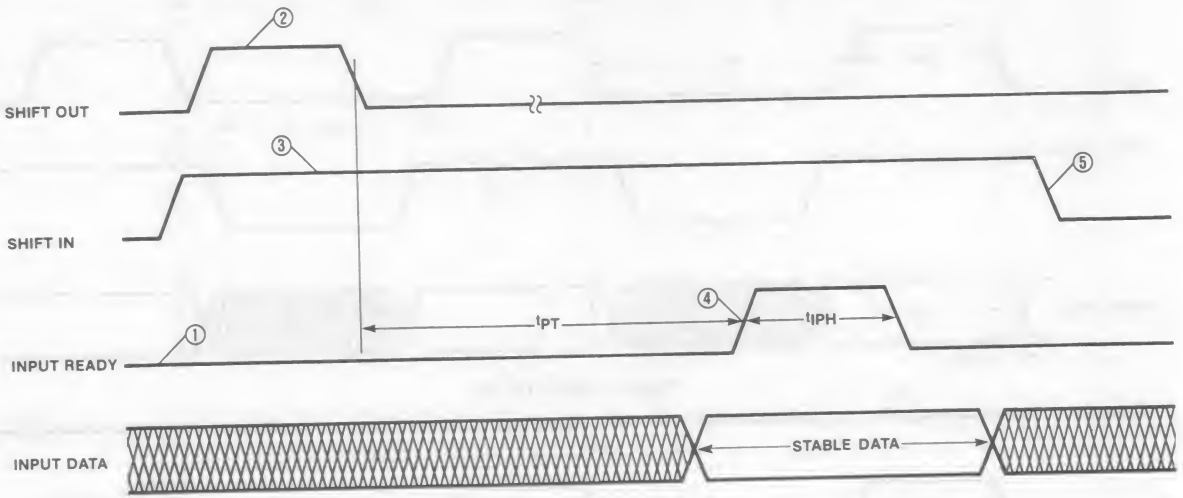


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.

(3) Shift In is held HIGH

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word

(5) The Data from the first word is released for "fall through" to second word

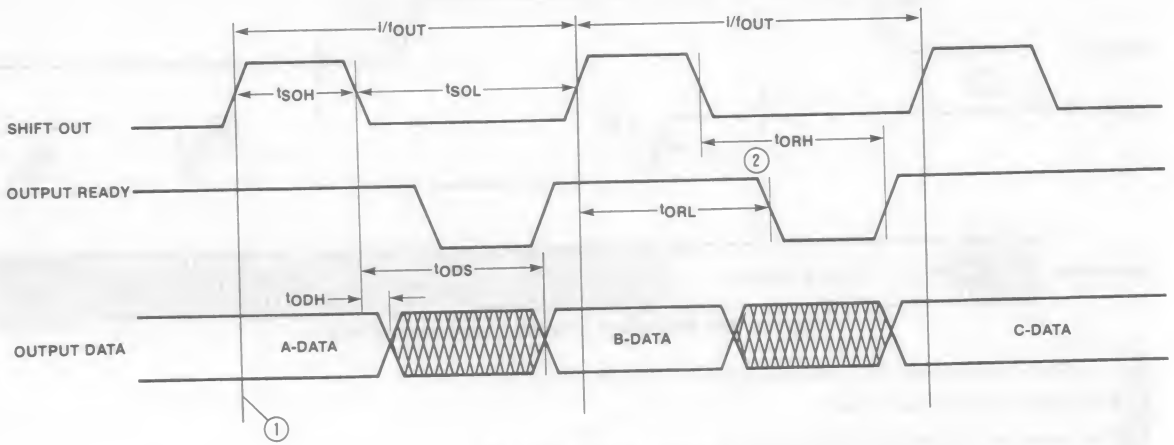


Figure 5. Output Timing

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

(2) Data is Shifted Out when Output Ready is HIGH and Shift Out makes a HIGH to LOW transition.

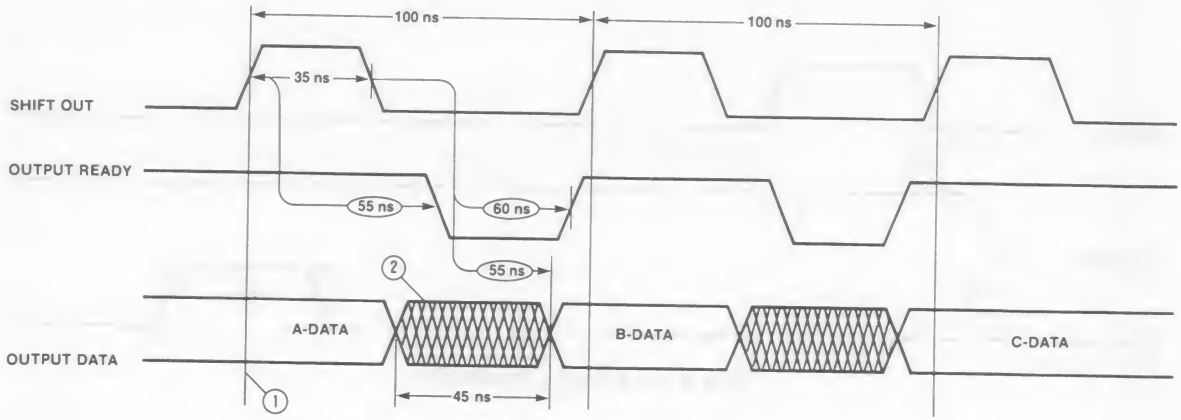


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

(2) Data in the crosshatched region may be A or B Data

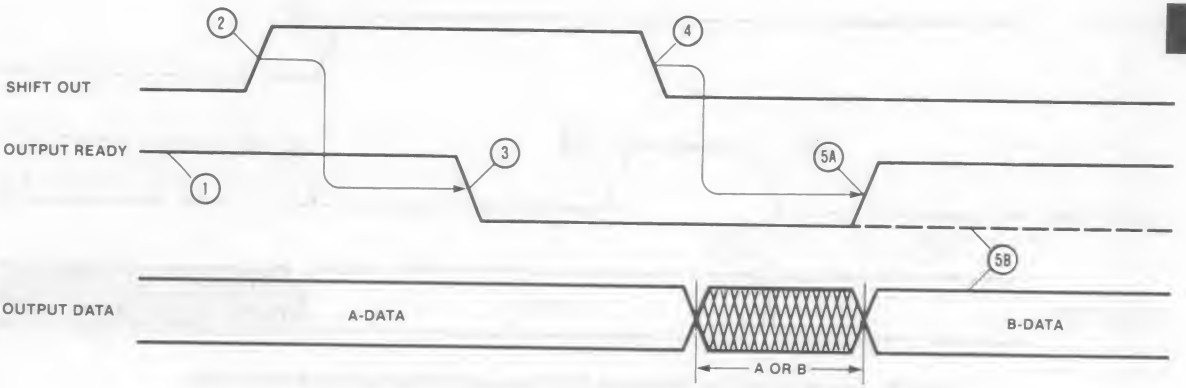


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

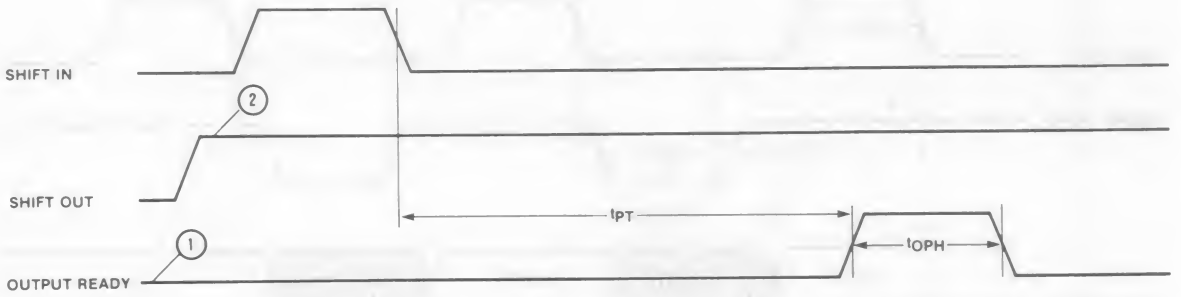


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.
(2) Shift Out held HIGH.

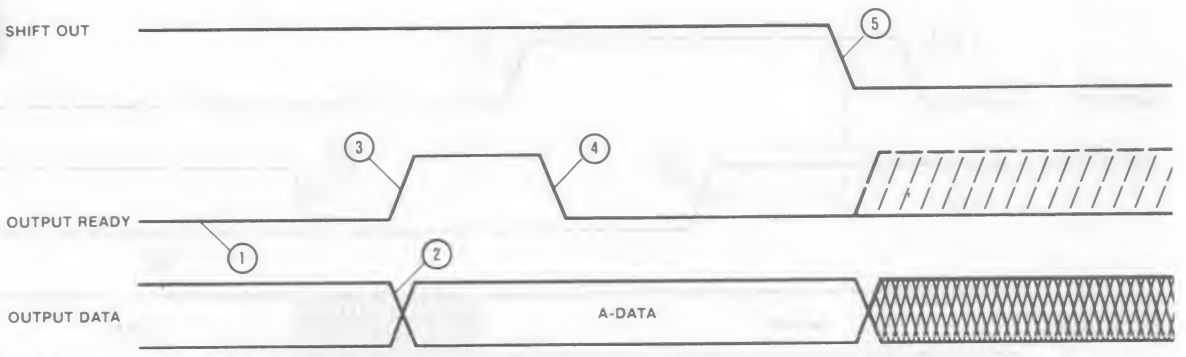


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

(1) Word 63 is empty.
(2) New data (A) arrives at the outputs (word 63).
(3) Output Ready goes HIGH indicating the arrival of the new data.
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

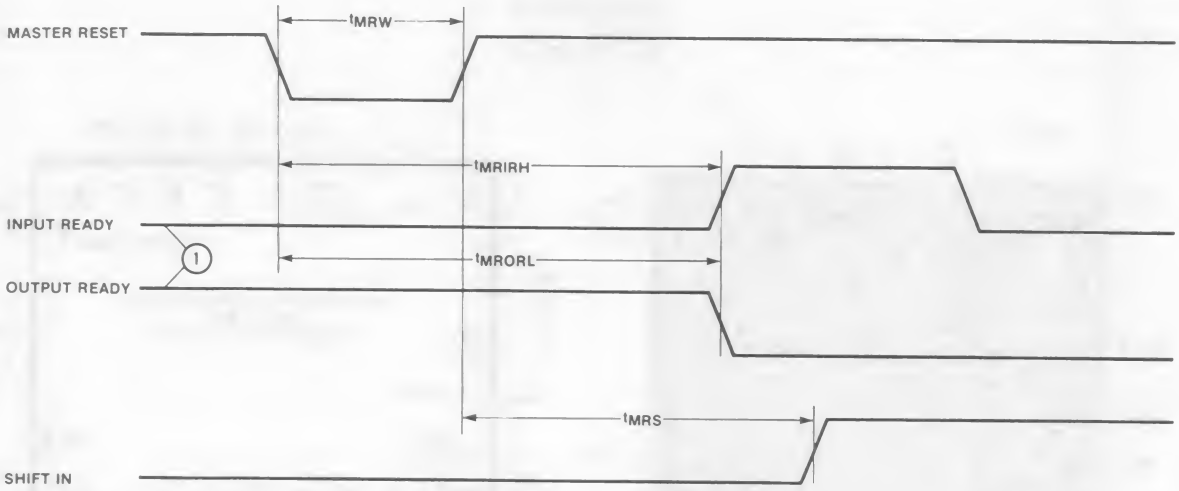
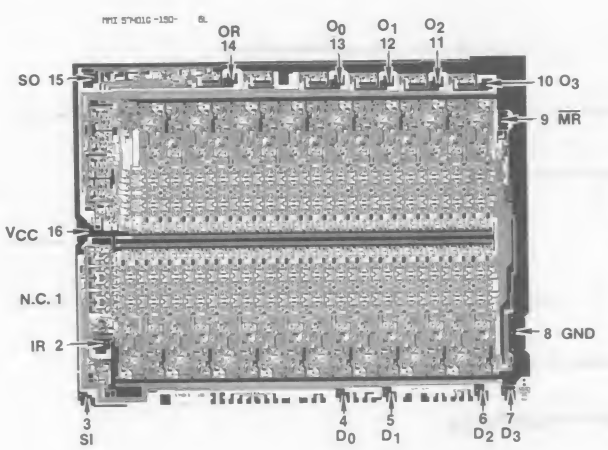
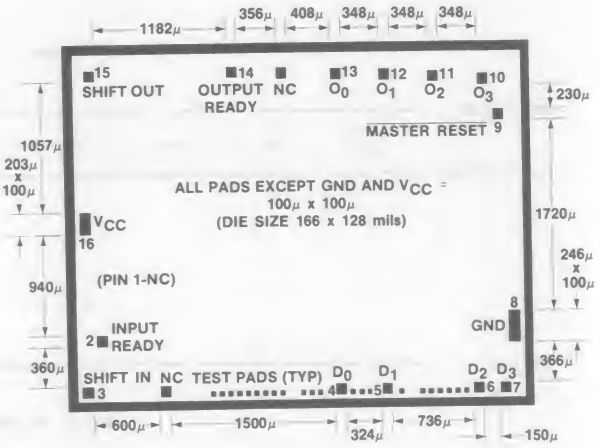


Figure 10. Master Reset Timing

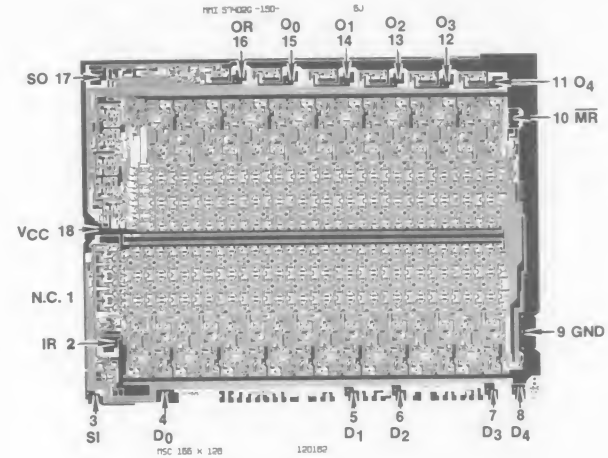
(1) FIFO initially full

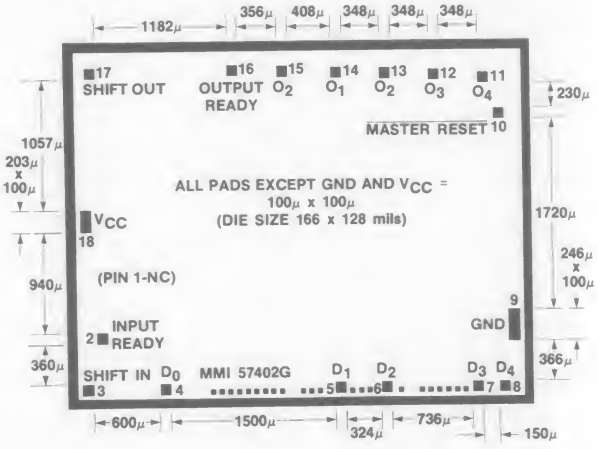
57401 Die Pattern
Step: G
Size: 128x166 mils





57402 Die Pattern
Step: G
Size: 128x166 mils





Low Power First-In First-Out (FIFO) 64x4 Cascadable Memory 67L401

Features/Benefits

- Guaranteed 5 MHz shift in/Shift out rates
- Low Power Consumption
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and much faster

Description

The 67L401 is a low-power First In/First Out (FIFO) memory device with TTL speed. This device is organized in a 64x4-bit structure and easily cascadable with similar FIFOs to any depth or width. A 5MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. FIFOs can be cascaded to any depth in a handshake mode. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

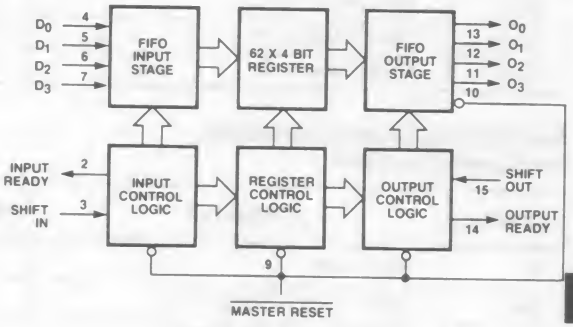
Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L401 is particularly useful where low-power consumption is critical.

Ordering Information

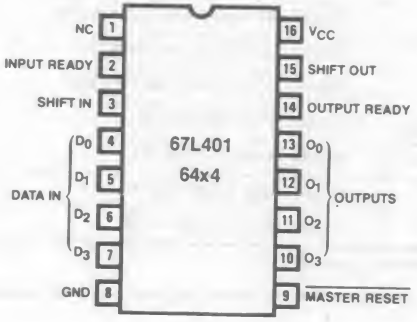
PART NUMBER	PKG	TEMP	DESCRIPTION
67L401	N	COM	5 MHz 64x4 FIFO
67L401	J	COM	5 MHz 64x4 FIFO

Block Diagram

67L401 64x4



Pin Configuration



9

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -.5V to 7V
Input voltage ..... -1.5V to 7V
Off-state output voltage ..... -.5V to 5.5V
Storage temperature range ..... -65° C to + 150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data set up	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics

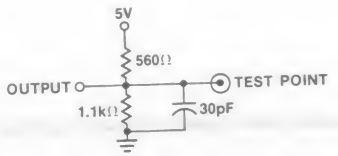
Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			95	ns
t_{PT}	Data throughput or "fall through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.

Standard Test Load



Input Pulse = 3V
Input Rise and Fall Time (10% – 90%) 2 – 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18mA			-1.5	V
I_{IL1}	Low-level input current	D_0-D_3 MR	V_{CC} = MAX	V_I = 0.45V			-0.8	mA
I_{IL2}		SI, SO					-1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_0 = 0V	-20		-90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		95	110	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

9

AC Test and Application Note

Since the FIFO is a high-speed device care must be exercised in design of the hardware and the timing. Though the external data rate is 5MHz, internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation as the FIFO is sensitive to very small glitches caused by long reflective lines, high capacitances, and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1μF directly between V_{CC} and GND with a very short lead length. In addition, care must be exercised in timing set-up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination as well as the Shift Out-Output Ready Combination, timing measurements may be misleading. i.e., Rising edge of the Shift-In pulse is not recognized until Input-Ready is high. If Input-Ready is not high due to (a) too high a frequency, (b) too wide a Shift-In pulse at that high frequency, or (c) FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will effect the device from a functional standpoint and will cause the "effective" timing of Input Data Hold Time (TIDH) and the next activity of Input Ready (TIRL) to be extended relative to Shift-In going high.

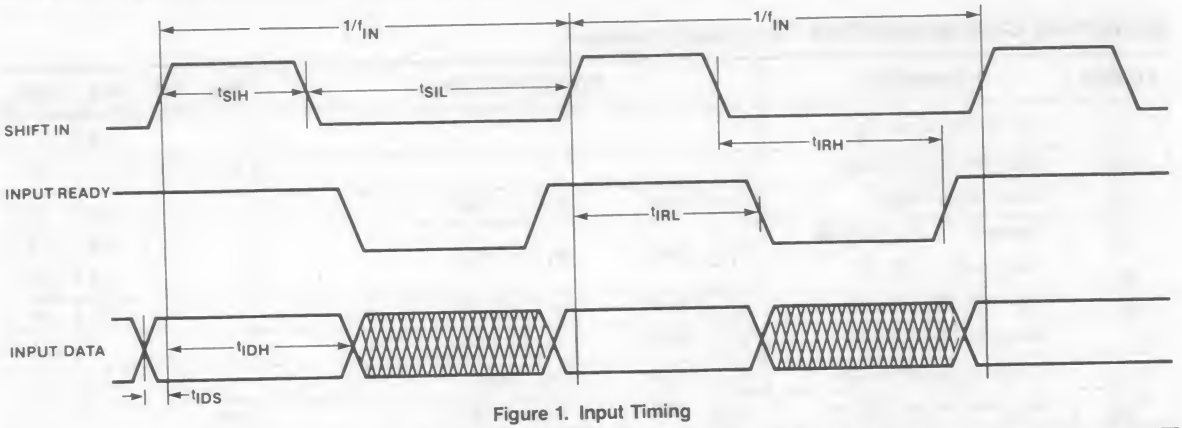


Figure 1. Input Timing

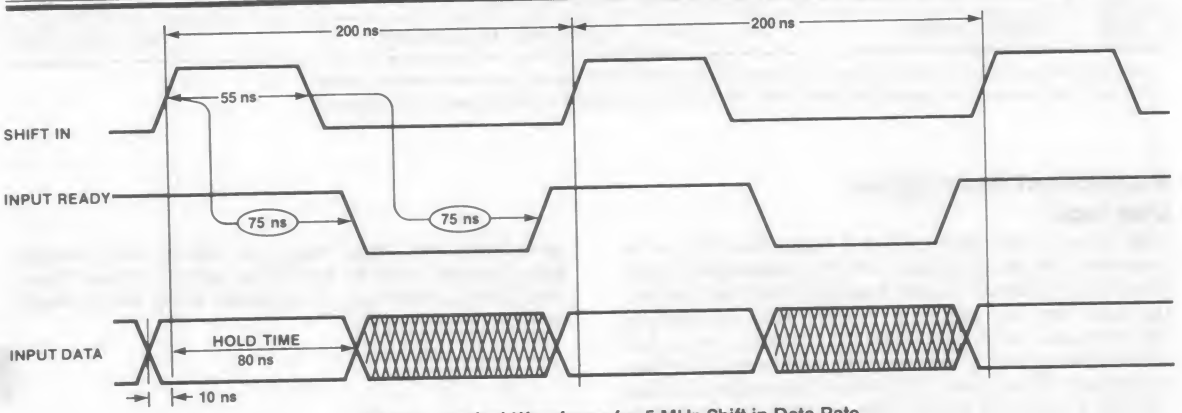


Figure 2. Typical Waveforms for 5 MHz Shift in Data Rate

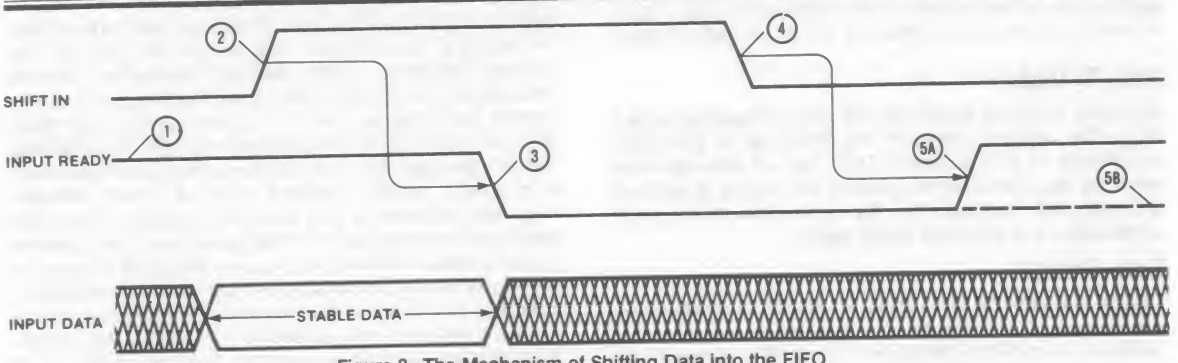


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

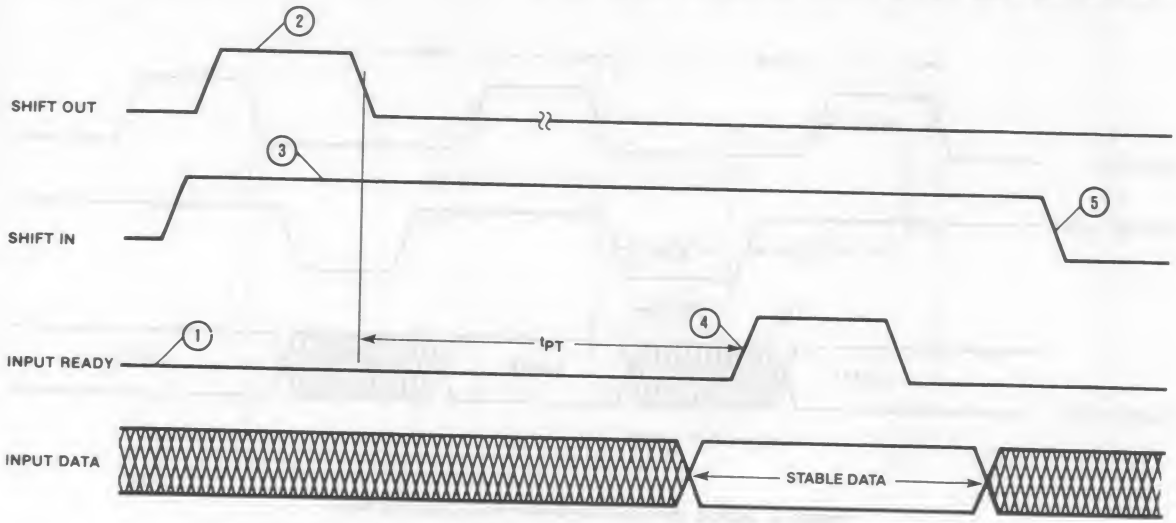


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.

(3) Shift In is held HIGH.

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

(5) The Data from the first word is released for "fall through" to second word.

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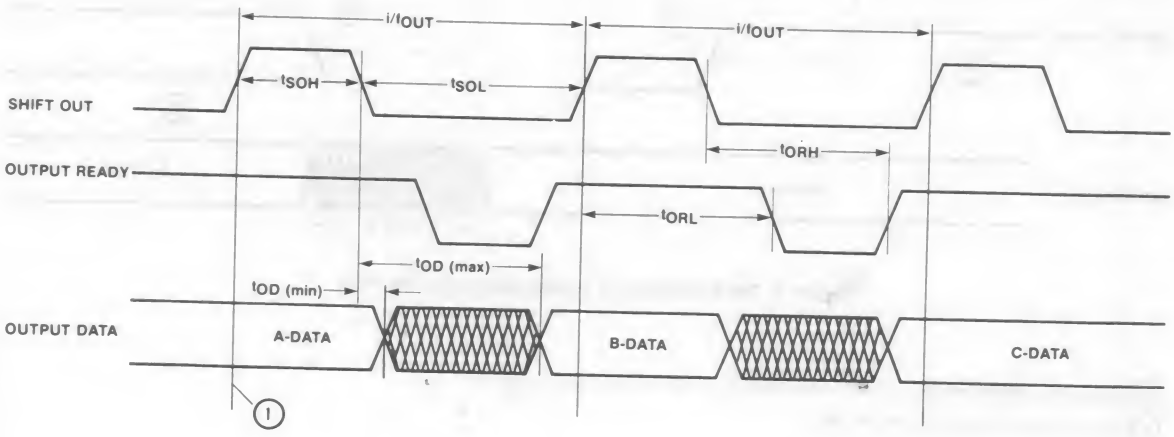


(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

Figure 5. Output Timing

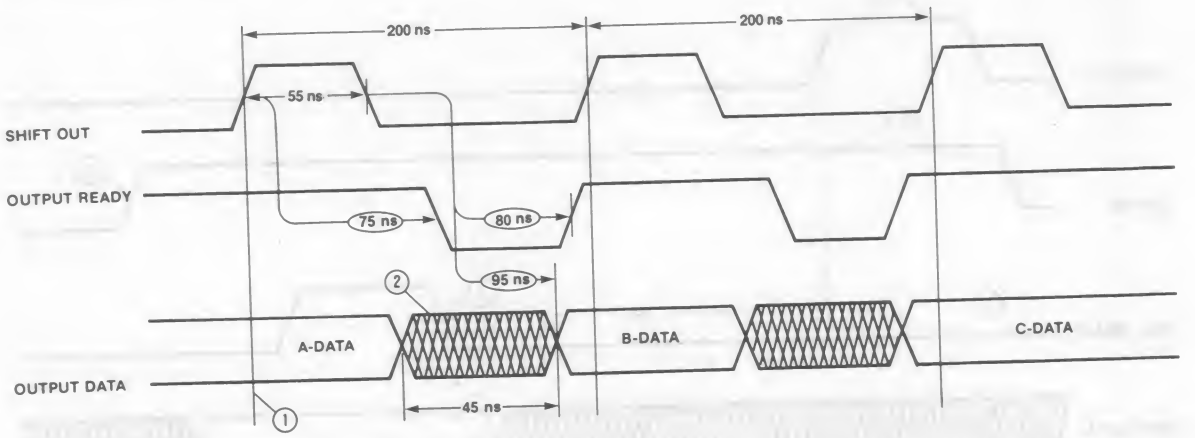


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

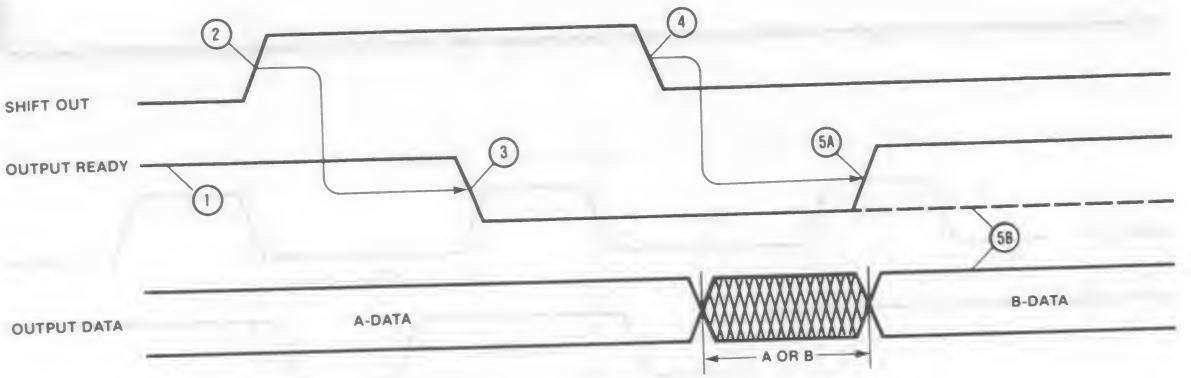


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

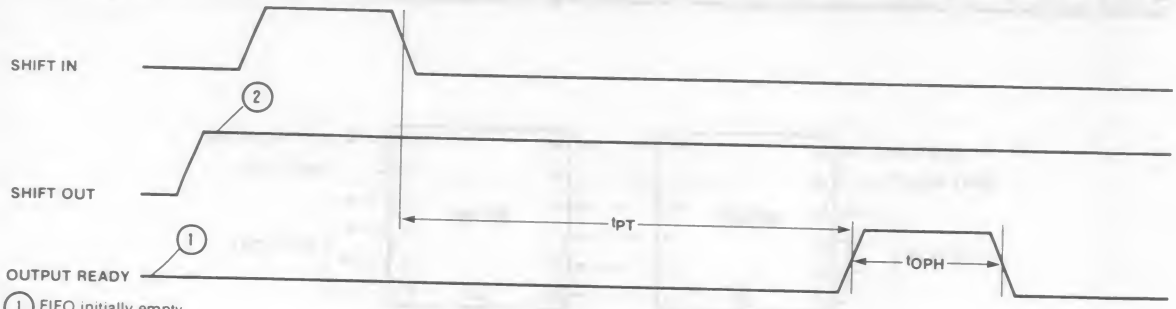
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



1. FIFO initially empty
2. Shift Out held HIGH

Figure 8. t_{PT} and t_{OPH} Specification

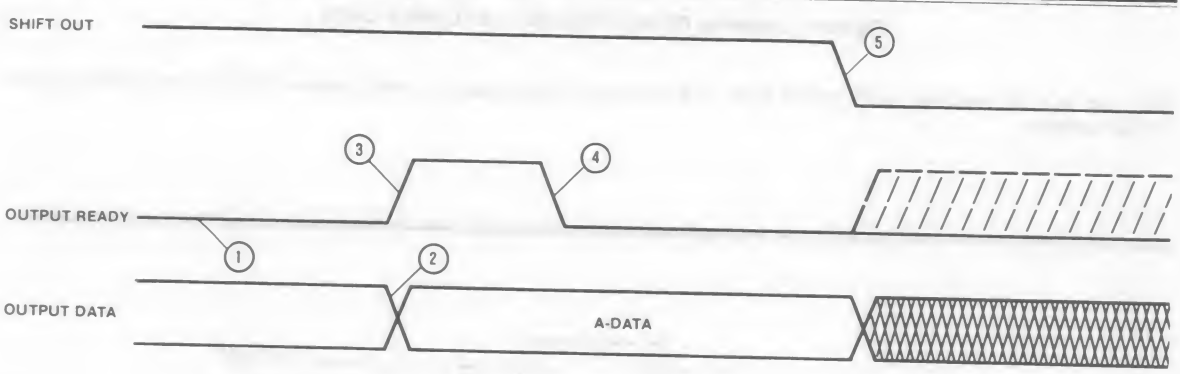
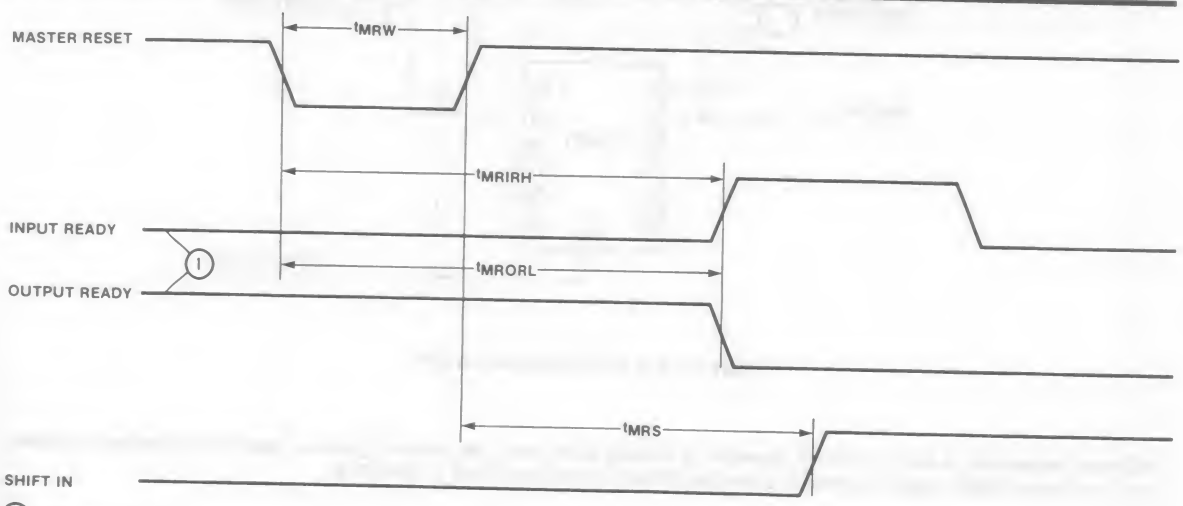


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty
2. New data (A) arrives at the outputs (word 63)
3. Output Ready goes HIGH indicating the arrival of the new data
4. Since Shift Out is held HIGH. Output Ready goes immediately LOW
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready



1. FIFO initially full.

Figure 10. Master Reset Timing

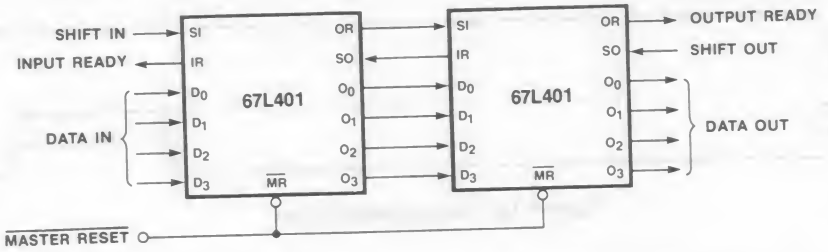


Figure 11. Cascading FIFOs to Form 128 x 4 FIFO with 67L401's

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

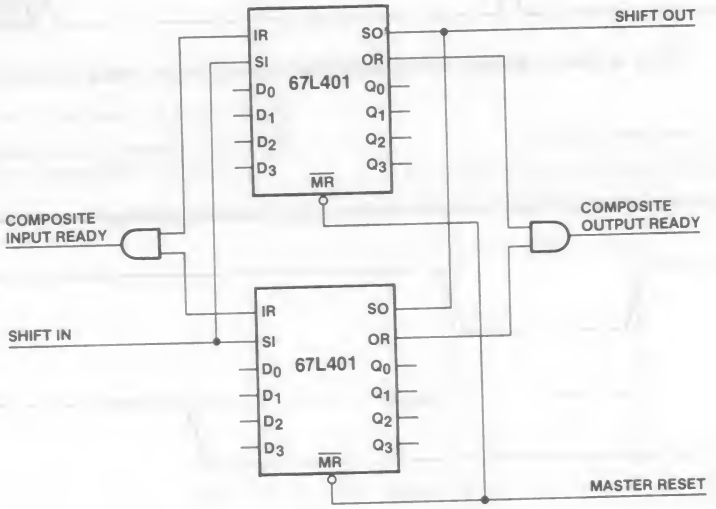


Figure 12. 64 x 8 FIFO with two 67L401's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.

The 67L401's can also be used in a bidirectional operation as shown in Figure 14.

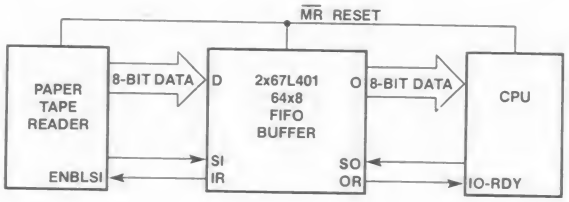
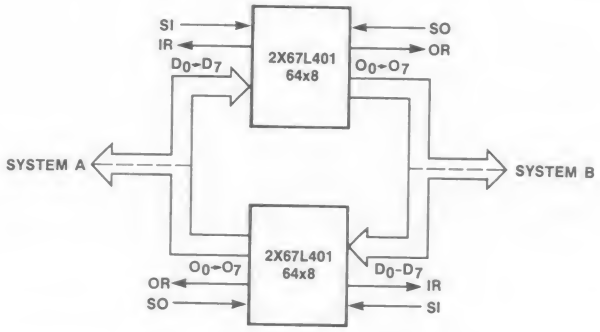
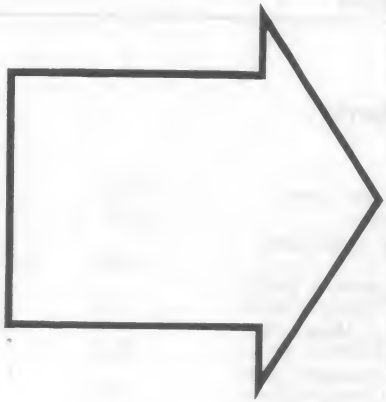


Figure 13. FIFO as data buffer between slow steady rate and fast 'burst' rate.



NOTE: Both depth and width expansion can be used in this mode.

Figure 14. Bidirectional FIFO application.



Memory Support Series Selection Guide

Dynamic RAM Controllers

DESCRIPTION	PART NUMBER	APPLICATIONS	PINS
Multi-mode DRAM Controller/Driver	SN74S408-3 SN74S408-2 SN74S408	16K 64K DRAMs	48
Multi-mode DRAM Controller/Driver	SN74S409-3 SN74S409-2 SN74S409	16K, 64K, 256K DRAMs	48

Octal Dynamic-RAM Drivers

DRAM Drivers with complementary Enables	SN54/74S700/731	Plug compatible with 'S210/241	20
DRAM Drivers with assertive Low Enables	SN54/74S730/734	Replaces Am2965/66 also pin compatible with 'S240/244	20

Power-Strobe Device

Quad Power/Logic Strobe	HD1-6600-8/HD1- 6605-8 HD1-6600-5/HD1-6605-5 HD1-6600-2/HD1-6605-2	Useful to "power down" devices to reduce total system power	16

Contents

Improving Your Memory With 'S700-Family MOS Drivers

Chuck Hastings and Suneel Rajpal

Introduction

Today, fast-access-time high-density dynamic random-access-memory integrated circuits (DRAMs) are where it's at in the design of commercial computer memories of any size, from tabletop personal-computer memories to giant mainframe memories; magnetic cores are, now, "but a distant memory." As a computer-scene corollary to Parkinson's First Law[r1], "Work expands to fill the time available," it is observably **always** true that "**Computer software expands to fill the memory available.**" Thus, the rapid advancements which have been made in the cost, density, availability, second-source standardization, and reliability of DRAMs have generally come just in the nick of time to keep up with the computer industry's insatiable demand for ever-larger main memories. To pick but one example, the Hewlett-Packard 3000-series minicomputer family was originally introduced with a maximum main-memory configuration of 131,072 bytes; today, the maximum configuration is 8,388,608 bytes, and plans for even larger configurations are already taking shape.

Unfortunately, the technological advancements in the **peripheral** integrated circuits needed to drive all of these DRAMs have, to say the least, been noticeably less rapid. The usual design practice has been to drive large DRAM arrays with high-current buffers such as 'S240s, coupled with external series resistors in the driven signal lines. Now, with the introduction of the Monolithic Memories 'S700/730/731/734 MOS drivers, the memory designer's task is greatly simplified.

The 'S700, 'S730, 'S731, and 'S734 are fast and powerful Schottky-technology TTL 8-bit buffers, specialized to drive large numbers of dynamic RAMs. Their internal design is particularly well adapted to driving signal lines with lots and lots of **distributed capacitance.** They are **drop-in, pin-compatible replacements** for the respective first-generation 'S240-family high-current drivers — 'S210, 'S240, 'S241, and 'S244, which excel for their intended high-current applications or even for lumped-capacitance applications but can be awkward to use in typical DRAM memory-board designs.

"...THE MONOLITHIC MEMORIES 'S700, 'S730, 'S731, AND 'S734 ARE...SPECIALIZED TO DRIVE LARGE NUMBERS OF DYNAMIC RAMS..."

So that you understand the essentials of what you need to know to design memory boards which work, we'll first take a quick glance at the electrical situation, complete with equations. Don't worry — we won't actually **derive** these equations here; derivations are readily available in the literature[r2, r3], and our purpose is simply to motivate some otherwise arbitrary-sounding statements as to what constitutes good layout practice. Following that, we'll present the rationale behind the various members of the family and their differing functional behavior or "architecture." Finally, we'll discuss some pragmatic design issues; how to avoid information loss due to glitches in battery-backup-protected memory systems during power failure, and when and where to use the 'S700 and 'S731 complementary-enable parts.

The Memory-Board Design Problem

The central problem facing the designer of a memory board is to drive a large number of highly-capacitative DRAM address, data, and control inputs just as fast as they can safely be driven, since memory speed (like memory size) is something which computer-system designers can never get quite enough of. Typically, a designer places **from 70 to 300 DRAMs on a single board.** Now, the address and data inputs of a DRAM have very non-negligible input capacitances — 3.5 picofarads (pf) typical, and 5 or even 7 pf worst-case; the control inputs may have as much as 10 pf worst-case. Assuming 5 pf, the total capacitance per address or data line per board must by simple multiplication fall between 350 pf and 1500 pf — even more when the capacitance of the printed-circuit-board (PCB) wiring traces is reckoned with. These numbers are not at all the sort of numbers you normally see on the data sheets for most of the industry-standard 8-bit buffers — those have for many years conventionally been specified by all vendors at 15 pf, 50 pf, etc. apparently according to the proposition that "small is beautiful," i.e., the logic delays and waveforms come out more agreeably at those numbers.

In keeping with motherhood and apple pie, the memory-board design obviously must be optimized for speed, reliability, physical area, and dollar cost; the **topology** (the physical organization and length of the wiring traces) and the number of drivers are chosen accordingly. Since contemporary DRAMs receive their complete addresses in **two** pieces, a "row address" and a "column address" (corresponding to the cell layout within the DRAM chip), the speed of the address-driving circuits is **particularly** critical since the bit pattern transmitted on the address lines must be changed **twice** during each complete memory read or write cycle. In DRAM "architecture," the row and column addresses are of equal length, say n bits, and the width of the data word within the DRAM is one bit in most contemporary parts. The first DRAMs with this architecture, in the mid-1970s, had n = 6, and thus were 2^{12}x1 = 4096x1 or "4K" DRAMs. By now, of course, such tiny DRAM sizes are

obsolete, and even 16K (16384x1) DRAMs are a super-low-cost commodity. Much commercial design today is being done with 64K (65536x1) DRAMs, and even larger DRAMs are coming soon; 256K (262144x1) DRAMs pin-compatible with the usual 64K types have been announced.

When all of these factors are taken into account, the practical upper limit to how many DRAM inputs can be hung on one trace is usually thought to be in the range of 80 to 100. This limit has some implications with respect to word length and word organization. The combined effect of the system word length as seen by the computer programmer, the number of check-code bits used for whatever checking scheme is employed, and the number of different words simultaneously accessed on one memory operation is to make certain odd-sounding total word lengths popular:

Organization	Total Word Length	Data Word Length	Check Bits/ Word	Checking Scheme
17x4	68	16	1	Simple parity
72x1	72	64	8	Hamming code
39x2	78	32	7	Hamming code
22x4	88	16	6	Hamming code

Table 1. Common DRAM Memory-Board Organizations

Assumptions and Equations

The key to good memory-board design is optimization of the layout and impedance of the wiring traces, and the choice of efficient RAM drivers. In prototype wirewrapped boards, the characteristic impedance of a wire which is at a varying distance from a ground plane as it crosses hill-and-dale over other wires may be difficult to control or predict, but is likely to be within the range of 100 to 120 ohms. In production memory boards, however, it is often a good approach to use **microstrips** to interconnect the array of DRAMs. A microstrip is simply a PCB wiring trace over a ground plane, separated from that ground plane by a thin layer of insulating medium such as fiberglass. A cross section of a microstrip is shown in Figure 1.

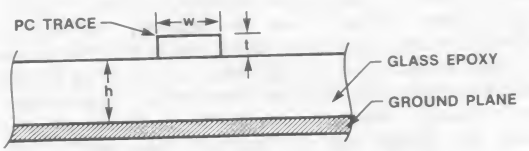


Figure 1. Microstrip Cross Section

The equations needed to design a memory board for a DRAM array interconnected by microstrips are listed below. Their rationale and derivation can be found in references on the application of electromagnetic field theory to circuit-board design[r2, r3].

Z_o = the characteristic trace impedance.

$$= \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \text{ ohms}$$

T_d = the trace propagation velocity.

$$= 0.0848 \sqrt{0.475e_r + 0.67} \text{ nsec/inch}$$

C_o = the trace capacitance.

$$= 1000 (T_d/Z_o) \text{ pf/inch}$$

C_d = the equivalent trace capacitance associated with each DRAM. It takes 0.5 inches to interconnect one DRAM.

$$= 3.5 \text{ pf}/0.5 \text{ inch} = 7 \text{ pf/inch}$$

Z'_o = the modified trace impedance due to the capacitive loading of the DRAMs.

$$= \frac{Z_o}{\sqrt{1 + C_d/C_o}}$$

T'_d = the modified trace propagation time due to the capacitive loading of the DRAMs.

$$= T_d \sqrt{1 + C_d/C_o}$$

Where:

e_r = the relative dielectric constant of the PC board.
h = the distance from the trace to the ground plane.
w = the width of the trace.
t = the thickness of the trace.

Design Approaches and Their Consequences

Very well then, let's charge right in and see what these formidable-looking equations predict will happen when a memory board is laid out in an obvious, common-sense manner. To make the example specific, we choose the 39x2 organization, so that from a circuit point of view the word length on the memory board is 78 bits. Now, each wiring trace has a capacitance (C_{TRACE}) and an inductance (L_{TRACE}) per DRAM; assuming that the DRAMs are deployed at uniform intervals along the trace, these values are determinable easily from the values per-unit-length from the microstrip equations just presented, once the spacing in inches between DRAMs has been specified. (The value for L_{TRACE} has been buried in the equation for Z_o above and won't appear in any subsequent equations.) To be specific, we'll make the realistic assumption of one DRAM per 1/2 inch of trace. Each DRAM input also has a capacitance (C_{DRAM}) and an inductance (which we're justified in neglecting); we'll assume that these are uniform, although the most sophisticated designers consider **distributions** of DRAM capacitances. The electrical situation which results is shown in Figure 2:

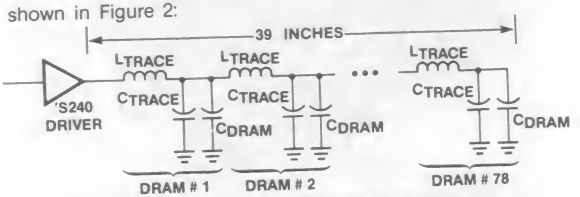


Figure 2. Transmission-Line Equivalent of a Single DRAM Wiring Trace

Typically, this trace has the following characteristics:

e_r = 5 (for G10 glass epoxy)
h = 30 mils
w = 15 mils
t = 3 mils

The following values can then be calculated using the appropriate equations:

Z_o = 85 ohms
T_d = 0.15 nsec/inch
C_o = 1.76 pf/inch
Z_o' = 38 ohms
T_d' = 0.35 nsec/inch

If we just string the DRAMs right down the trace like Christmas-tree lights, it will take 39 inches of trace to connect all 78 of them. So the actual propagation delay of the drive signal as it surges down this trace will be T_d' times 39 inches, or 0.35x39 = 13.7 nsec.

Notice that we are embarked on a design which is **specific** to the properties, including C_{DRAM}, of the DRAMs which we are using; a final board design is inevitably, to some extent, "tuned" to a specific DRAM type. If C_{DRAM} changes, even in what might be considered the favorable direction (smaller, obviously!), the trace impedance gets changed and the design may no longer be "tuned." But we won't worry about that here.

Now, an 'S240 driver, such as we have assumed to be driving the trace, has a signal rise time or fall time of anywhere from 2 nsec to 10 nsec, depending on semiconductor manufacturing parameters. (The rise time is, to be precise, defined as the time it takes for the output voltage to go from 10% of full-scale to 90% of full-scale; the fall time is the obvious converse.) A good rule-of-thumb for circuit-board designers is that twice the propagation delay of the trace should be less than the rise time or fall time of the driver in order to avoid serious signal **reflections,** in which a "reflected" electromagnetic wave comes bouncing back from the other end of the trace. In other words, 2x 13.7 nsec = 27.4 nsec must be less than 2-to-10 nsec, which it obviously isn't. Hence there **will** be reflections on this line, and **ringing** of the signal will occur, resulting in a waveform in the trace which looks like that of Figure 3 for a High-to-Low transition at the 'S240 output. The amplitude of the ringing voltage in real systems may be as much as 2v or even 2.5v.

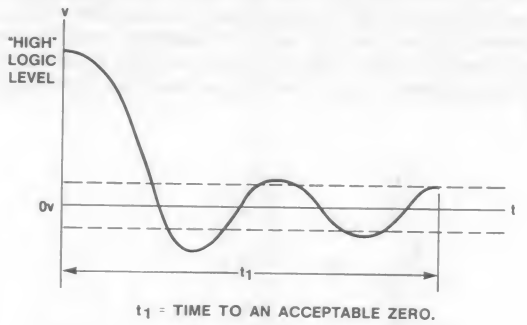


Figure 3. Line Ringing Due To Driver Mismatch

An 'S240 has a Schottky-driver output stage which may simplistically and approximately be represented as shown in Figure 4. When the 'S240 is driving to the logic High state, the switch S may be thought of as in position #1; when it is driving Low, S is in position #2. The effective output impedance of the 'S240 is thus about 30 ohms when driving from a previous Low state to High, but only about 10 ohms when driving from High to Low — a 3:1 difference. Thus, as the large lower transistor in the output "totem-pole" structure turns on very fast because of this low impedance, the fall time is **extremely** fast, and when ringing occurs the result may be **undershoot** — the voltage in the trace actually falls **below ground**.

An obvious consequence of ringing in the signal trace is that the system designer must allow much longer for the driver voltages, as seen by the DRAM inputs, to settle down after a transition since the ringing may be severe enough to repeatedly cross the switching threshold for the DRAMs. If this settling only had to happen once per memory access it would be bad enough, but it happens **twice** — remember that first the **row** address, and then the **column** address, gets transmitted over the address lines. Thus the allowances made for ringing cause memory performance, as measured by access time and/or cycle time, to significantly deteriorate.

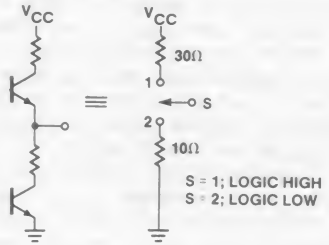


Figure 4. Typical Schottky-Driver Output Impedances

Even worse things can happen because of undershoot. First, if the voltage as seen by the DRAM inputs ever falls below -1.0v, that is, more than a volt below the steady-state PCB ground voltage at the DRAM ground pins, the contents of the "row-address registers" within the DRAMs can be altered. (**Some** DRAMs are supposed to be able to stand -2v for 20 nsec, but others just can't handle it.) Thus, if a write operation is in progress, the data word can get written helter-skelter into **different address locations in different DRAMs** (remember, each DRAM is just 1 bit wide!), so that the entire memory system very rapidly forgets everything it once knew. Second, the current surges resulting from severe undershoot may cause some 'S240-type drivers themselves to rather quickly self-destruct, which can be particularly annoying if they have been dip-soldered into place.

At this point it appears that our simple, common-sense first cut at memory-board layout is a naive recipe for disaster. So what can we do to improve on this naive approach and get the memory board to work?

First, we can **series terminate** the trace with a 10-ohm resistor to improve the impedance match. "Series termination" simply means that the resistor is located right **at** the 'S240 output, between it and the rest of the trace. 10 ohms is probably the minimum value for this resistor; other values of up to 33 ohms are also in use, according to the design context.

Second, much of our problem came about because of the sheer physical length of the trace, so we can modify the topology to cut that in half by having two "legs" rather than just

one off the driver output, which should essentially cut the propagation time for the trace in half.

Third, we also if need be could vary the trace **width** :w to change the trace impedance Z_0 to a value more to our liking, in order to fine-tune the design, but we won't pursue that possibility here.

The result is the significantly-different layout of Figure 5, with all of the cute little capacitors and inductors omitted for clarity (or actually for sheer laziness):

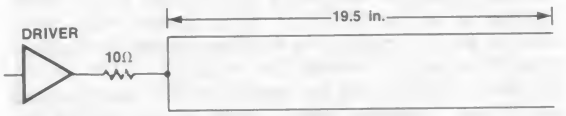


Figure 5. An Improved Layout

When the calculations are repeated, it turns out that the propagation delay down each leg of the trace is half as much, or 6.9 nsec; and the output impedances of the 'S240-plus-series-resistor are now 40 ohms when driving from Low to High, and 20 ohms when driving from High to Low, which is only a 2:1 difference. The trace impedance seen by this 'S240-plus-series-resistor is that of two 38-ohm legs in parallel, or 19 ohms, which is a very much better match to its effective output impedance. Also, the series resistor acts to slow down the exceedingly-rapid fall time of the 'S240, to the point where it may not be a great deal less than (or may even exceed) twice the trace propagation delay. So, obviously, we're a lot better off than we were.

Unfortunately, we're still not home free. We've also slowed down the **rise** time of the 'S240, i.e., the Low-to-High transition, which we weren't intending to do since it wasn't a problem. What we **really** would like is for the Low-to-High transition time and the High-to-Low transition time to become virtually the same, i.e., "symmetric." Now, DRAM addresses and data have a generally unpredictable salt-and-pepper mixture of ones and zeroes, and there is no way to take advantage under system conditions of a circuit design with one of these transition times much faster than the other. So computer-systems people, who have to be brutal realists rather than cockeyed optimists if their systems are to work reliably under real-world assumptions, normally just take whichever of these two transition times is "worse" (that is, longer) as the "logic delay" of the part as it operates within a system. Which is only reasonable! And thus it comes about that a deterioration in transition-time **symmetry** translates as a deterioration in net system **speed**.

So what do we do next? Well, we could try applying the same improvements a second time, by breaking the trace into **four** legs; however, physically interconnecting these four legs then will add more trace length, so that topology has to be traded off against interconnection efficiency. What would just get us out of this whole mess is if we could get **inside** the 'S240 and put the series resistor someplace where it will result in the effective output impedance of the driver being the same whether it is driving from Low to High or from High to Low. But we can't do **that**. Can we? Can we???

The 'S700-Family Drivers to the Rescue

Well, we can't exactly get **inside** an 'S240 and stick in a series resistor. We can, however, pull the 'S240 out of the socket it is occupying, and pop in an 'S730 — which is a **pin-compatible drop-in replacement**, and has the series resistor in exactly the right place. If we had been using a different 'S240-family driver, we could still have done the same thing — an 'S734 replaces an 'S244, an 'S700 replaces an 'S210, and an 'S731 replaces an 'S241; more on the various part types shortly.

When thus popped in as 'S240-type driver replacements, 'S700, 'S730, 'S731, and 'S734 drivers will generally speed up the total **effective** access and cycle times for most DRAM boards. This speed improvement is achieved by a sophisticated, rather than a brute-force, circuit-design approach. We've already let the cat out of the bag; they feature a new type of output stage, incorporating a **built-in** series limiting resistor, designed to efficiently drive highly-capacitative loads such as arrays of DRAM inputs interconnected by typical printed-circuit-board (PCB) wiring traces. This series resistor is located in the ideal place — between the collector of the lower output transistor in the totem-pole structure and the output pin. (See Figure 6.)

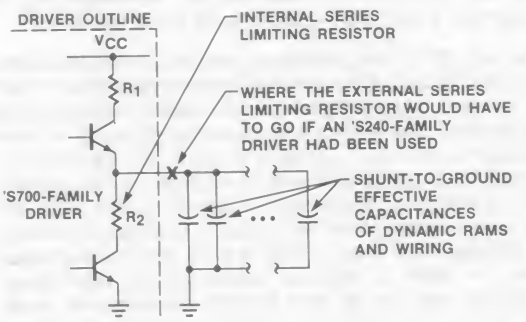


Figure 6. The Dynamic-RAM-Driver Circuit Output Stage

Now that the all-important resistor is safely inside the driver chip, its value is chosen as 20-25 ohms, so that the **in-system** Low-to-High and High-to-Low transition times of the resulting driver output stage remain symmetric, **with** the series resistor accounted for, under a wide range of circuit-loading conditions. The equivalent to Figure 4 for this new improved output stage is:

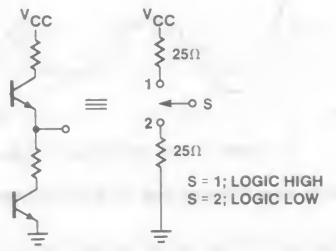
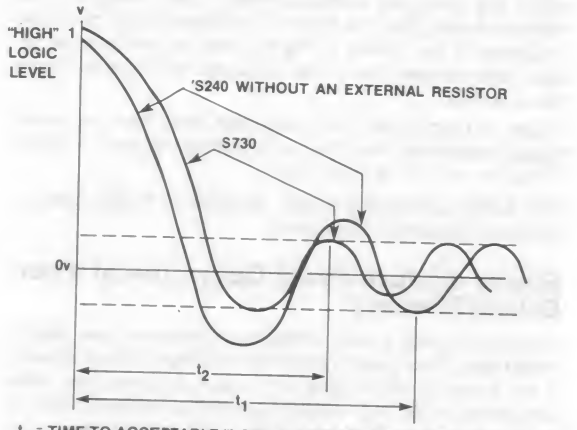


Figure 7. Driver Output Stage for 'S700-Series Buffers

What does that additional resistor in the transistor buy you? Plenty, when coupled with the other design features incorporated into the 'S700, 'S730, 'S731, and 'S734. First, there is a balanced impedance of about 25 ohms for either the Low-to-High transition or the High-to-Low transition. Since the effective impedance for the Low-to-High transition is now considerably higher than it was when using an 'S240, the undershoot problem goes away — the output voltage can never have an undershoot worse than 0.5v. Ringing **can** still occur; however, the time taken to reach an acceptable zero level is smaller than it was when using an 'S240, as shown in Figure 8.

Another advantage of the 'S700, 'S730, 'S731, and 'S734 is the high-state output voltage, now guaranteed to reach at least V_{CC}-1.15v. Certain MOS DRAM inputs are specified to require a minimum V_{IH} of 2.7 volts. More on this and other specification issues in just a minute.



t_1 = TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR THE 'S240 WITHOUT AN EXTERNAL RESISTOR.

t_2 = TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR THE 'S730.

Figure 8. Comparison of Undershoots; 'S240 and 'S730

Undershoot control, balanced High-state and Low-state output impedances, and appropriate voltage levels make the 'S700, 'S730, 'S731, and 'S734 very efficient RAM drivers. Consequently, although 'S240-family buffers may exhibit greater speed under light loading conditions and may even sink larger currents when operated in test jigs, 'S700-family buffers are likely to perform better under **realistic system conditions** when driving large capacitive loads is a major factor in the application. There may even be some **non-DRAM** bus-driving applications where such is the case!

And, as small added bonuses, the designer no longer has to find the physical space on his/her board for the external limiting resistors, and the resistors themselves no longer have to be paid for, and nobody has to be paid to stuff them into place on production copies of the board. All in all, an across-the-board "win-win" situation.

Keeping the Family Straight

Of the four new buffers in the 'S700 family, two — the 'S730 and 'S734 — are alternate-source versions of the Am2965 and Am2966 respectively. These two parts were originally introduced by AMD, which has also designated them alternatively as AmZ8165 and AmZ8166.

The other two buffers — the 'S700 and 'S731 — are **complementary-enable** versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244. Complementary-enable parts excel in driving buses where the information to be placed on the bus can come from two different but physically adjacent origins, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system, or row-address fields and column-address fields on a DRAM memory board; more on this later.

These four new 'S700-family buffers may be grouped with Monolithic Memories' other buffers in a 2x2 matrix chart or "Karnaugh map," with the dimensions of this map chosen to be the assertiveness of the second-buffer-group enable input E_2 (here across the top, or X-axis) and the polarity of the data-buffer logical elements themselves (here down the side, or Y-axis). This chart is Table 2 of "Pick the Right 8-bit or 16-bit Interface Part for the Job," in section 13 of this databook.

The logic symbols for each of these four parts are shown on the first page of the data sheet, in part-number order. Except for the differences already noted in the assertiveness of signal E_2, and in the output polarity of the data buffers, these parts are all mutually pin-compatible.

You will have an easier time keeping these four parts straight once you notice that the part number for one particular "architecture" of 'S700-series buffer is always the part number of the corresponding high-current buffer, **plus 490**. Since hundreds of 54/74 part numbers have already been assigned, even though not all of the corresponding parts are yet in production, obtaining part numbers with even **this** much method in the madness was not exactly a piece of cake! Anyhow, if you want to easily remember what the part number should be when you replace an 'S240-family buffer with an 'S700-family buffer, you must add 490 to its part number: e.g., 'S241 + 490 = 'S731, and so forth.

Like other Monolithic Memories 20-pin 8-bit interface circuits, the 'S700, 'S730, 'S731, and 'S734 come in the celebrated 300-mil SKINNYDIP™ package. They **also** come in eutectic-seal-flatpack and leadless-chip-carrier packages.

"...THE 'S700, 'S730, 'S731, AND 'S734 COME IN THE CELEBRATED 300-MIL 'SKINNYDIP™' PACKAGE..."

A Few Subtleties Regarding 'S700-Family Driver Specifications

If you are used to regular run-of-the-mill TTL data sheets, you should become sensitive to the fact that in several respects the Monolithic Memories 'S700-family data sheet (and, to be fair to a friendly competitor, AMD's Am2965/6 data sheet) represents a substantial departure from this norm.

First, since 'S700-family MOS drivers are obviously intended to mingle freely in the MOS world, they are specified to operate properly with as much as a ± 10% power-supply-level fluctuation over the entire commercial temperature range, instead of just the usual TTL ± 5%. The ± 10% standard is usual for MOS parts, but in the TTL world it is normally met only by selected military-version parts specified over the military temperature range. Thus, the V_{CC} seen by your commercial 'S700-series parts may fluctuate (even though you hope it won't) from 4.50v to 5.50v instead of only from 4.75v to 5.25v as for most commercial TTL.

Second, as already mentioned, an acceptable output logic High is considered to be V_{CC} -1.15v, or 3.85v assuming that your power supply really **is** under control after all. MOS parts are specified to think they're still seeing a Low up to 0.8v at an input, and to be seeing a High above either 2.4v or 2.7v; in between is, of course, the usual transitional or no-mans-land region. In keeping with the needs of the MOS world, 'S700-family Low-to-High logic propagation delays are measured from when the **input** crosses the usual TTL threshold somewhere in this no-mans-land (say 1.5v) to when the **output** crosses 2.7v — **not** merely to when the output crosses the TTL threshold. Likewise, 'S700-family High-to-Low logic propagation delays are measured from when the input crosses the TTL threshold to when the output crosses 0.8v. (See Figure 9).

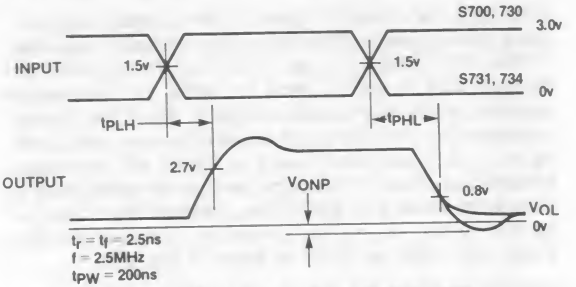


Figure 9. S700-Family Output-Voltage-Level Specification Conventions

Third, **both** minimum and maximum propagation delays are specified (at 25° C and 5v), so that you don't need to worry about any unwanted consequences in your system if your memory-access time for some bit positions turns out to be unexpectedly low relative to that for other bit positions. Worst-case skew between two buffer elements on the same chip is also specified.

Fourth, in keeping with the pledge that these parts can drive highly-capacitative lines, they are **specified** that way — at 500 pf loading, not only at 50 pf loading.

Fifth, unlike 'S240-family buffers, 'S700-family MOS drivers do **not** feature designed-in hysteresis.

Power-Failure-Proof Operation of Your DRAM Memory

It's generally nice if your computer, of whatever size, doesn't forget everything it was in the midst of doing and remembering if a-c power suddenly goes off. In fact, for large mainframe computers and for high-reliability control computers it may be downright critical. So, increasingly, memory designs include power-failure-protection logic, and DRAM "refresh" circuitry can run on battery-backup power. A typical design implementation is shown in Figure 10.

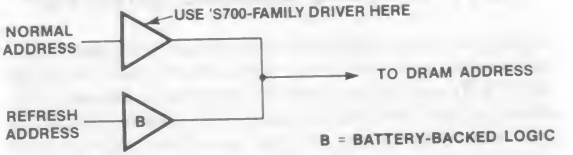
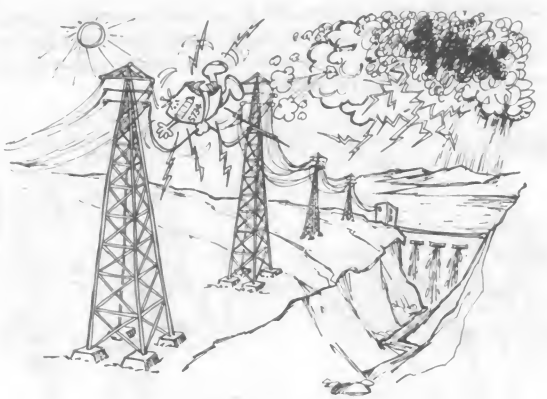


Figure 10. Battery Backup for Refresh-Address Logic

The refresh operations for the memory array must be **uninterrupted** during the transitions from a-c power to battery power and back, or else data will be lost; consequently, **all** of the logic associated with the DRAM refresh operations must be backed up. For economic reasons, other logic may **not** be backed up; hence, great care must be taken in the design at the DRAM interface, so that transients or oscillations are not introduced into the DRAM input lines by the non-backed-up logic thrashing around as a-c power goes down or comes back up.

Returning to Figure 10, note that it is the **normal** address path which is a potential source of DRAM input glitches, since the refresh-address-path buffer presumably never goes down. Again 'S700-family drivers can come riding to the rescue, since they are guaranteed to maintain glitch-free operation during either power-up or power-down.



"... 'S700 FAMILY MOS DRIVERS... ARE SPECIFIED TO OPERATE PROPERLY WITH AS MUCH AS A ±10% POWER-SUPPLY-LEVEL FLUCTUATION OVER THE ENTIRE COMMERCIAL TEMPERATURE RANGE, INSTEAD OF THE USUAL TTL ±5%..."

Where to Use Complementary-Enable MOS Drivers

Driving a dynamic-MOS RAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9 of "Pick the Right 8-bit or 16-bit Interface Part for the Job," in section 13 of this databook. This part is an inverting complementary-enable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.

First of all, a TTL inverting buffer normally has one less transistor —and hence one less delay — in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOS RAMs really don't care if their addresses come in "true" or "complemented" form as long as that form **never** changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here CAS or "Column Address Strobe") is tied directly to both $\overline{E}_1$ and E_2, and the two 4-bit groups of outputs are tied together.

Like other three-state buffers, these parts operate in a "break-before-make" manner — it is faster to disable an output than to enable an output, by design. (The worst-case data-sheet a-c parameters don't always imply "break-before-make" operation, but the parts themselves **do** operate that way.) So, if two outputs are tied together and exchange control of the bus, they can't "fight," i.e., try simultaneously to drive the bus in opposite directions; at any given instant, one of the two will always be "floating" in the hi-Z state.

The 8 data input lines to **each** 'S700 must, of course, be parceled out with 4 lines coming from the row address and 4 lines coming from the column address.

These same advantages continue to accrue when an 'S700 is used, for example, to select between instruction addresses and data addresses in a minicomputer, or between next-micro-instruction and branch addresses in a microengine, or between input and output addresses in a multiplexed input/output data channel, assuming that in each of these cases the address being produced is to go to the DRAMs without further ado. Notice that the 'S700s here are accomplishing **driving** (that is, power amplification and impedance matching) **and multiplexing simultaneously**. You could have used an MSI multiplexer part followed by an 'S730 to accomplish this very same thing, but with more logic delay.

If what you need in your application is a **non-inverting** driver, then everything we've just said above about the 'S700 continues to hold for the 'S731.

The Bottom Line

The 'S700, 'S730, 'S731, and 'S734, because of their unique output stage with an internal series resistor and balanced-impedance characteristics, can drive highly-capacitive loads of up to perhaps 100 dynamic-MOS RAM inputs. Since undershoot is limited to -0.5v already and so no **external** series limiting resistors are needed, the result is a net **system** speed gain, since Low-to-High and High-to-Low transition times remain symmetric. Otherwise, the logic delay would get degraded, since it must always be taken as the **worse** of these two transition times, and the use of an **external** series resistor greatly lengthens the Low-to-High transition time.

These second-generation MOS drivers also guarantee an output High voltage of V_{CC} -1.15v, and provide glitch-free operation during power-up and power-down. All of these features make them especially suitable for driving the address, data, and control lines of arrays of MOS DRAMs.

Credit Where Credit Is Due

A couple of years ago, many Monolithic Memories customers approached us with the emphatic suggestion that we should produce MOS drivers of this type, backed up by technical arguments which we have attempted herein to distil and present. In particular, the advice and assistance of Tak Watanabe of the Hewlett-Packard Computer Systems Division in Cupertino, California, has been utterly essential in the preparation of this application note.

Also, it was originally at Tak's suggestion that Monolithic Memories decided to produce the 'S700 and 'S731 complementary-enable drivers, as well as the 'S730 and 'S734 assertive-low-enable drivers. Tak's contributions, and those of other sage electronics-industry designers with whom we have spoken, are hereby gratefully acknowledged.

References

r1. *Parkinson's Law and Other Studies in Administration*, C. Northcote Parkinson, Houghton Mifflin Company, Boston, MA, 1957; also Ballantine Books, N.Y., 1964.

r2. *MECL System Design Handbook*, William R. Blood, Jr., Motorola Semiconductor Products Inc., Mesa, AZ, May 1980 (most recent edition); see in particular chapter 7.

r3. "Characteristics of Microstrip Transmission Lines," H. R. Kaupp, *IEEE Transactions on Electronic Computers*, April 1967 (Volume EC-16, Number 2); pages 185-193.

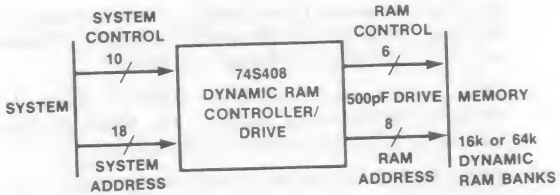
Dynamic RAM Controller/Driver

SN74S408/DP8408
SN74S408-2/DP8408-2
SN74S408-3/DP8408-3

Features/Benefits

- All DRAM drive functions on one chip have on-chip high capacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K and 64K DRAMS: Capable of Addressing up to 256K words
- Propagation delays of 25nsec typical at 500 Pf load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- 6 operating modes support externally controlled access and refresh, automatic access, as well as special memory initialization access
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- Direct replacement for National DP8408

MODE	MODE OF OPERATION
0,1,2	Externally controlled refresh
3	Externally controlled All-$\overline{RAS}$ write
4	Externally controlled access
5	Auto access, slow t_{RAH}
6	Auto access, fast t_{RAH}
7	Set end of count

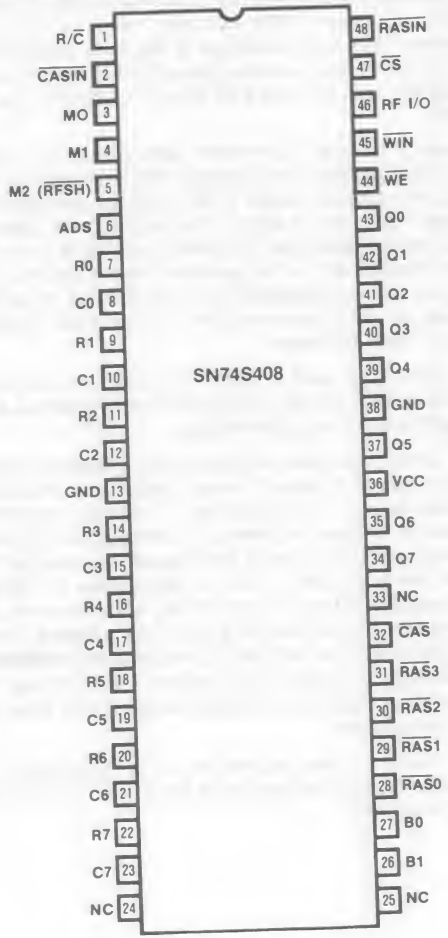


74S408 Interface Between System and DRAM Banks

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S408	N48, D48	COM
SN74S408-2	N48, D48	COM, SPEED OPTION
SN74S408-3	N48, D48	COM, AC OPTION

Pin Configuration



NC = NO CONNECTION

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

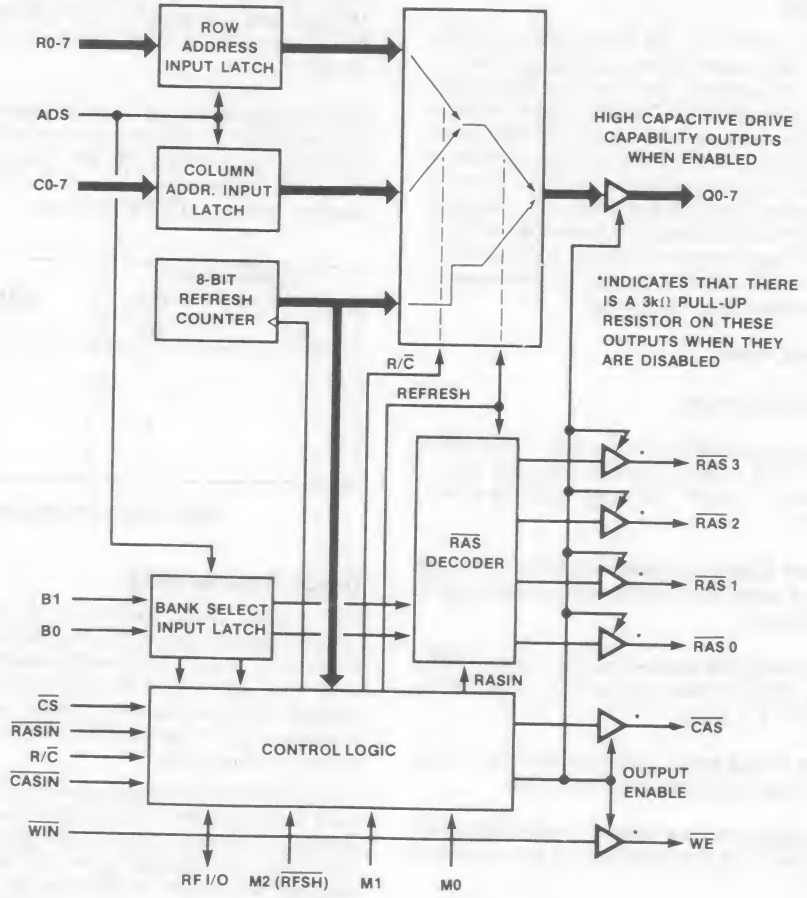


Figure 1. 74S408 Functional Block Diagram

Description

The 74S408 is a Multi-Mode Dynamic RAM Controller/Driver capable of driving directly up to 88 DRAMs. 18 address lines allow the 74S408 to drive all 16K and 64K DRAMs and addresses up to 256K words. Since the 74S408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews and saves in board space.

The 74S408's 6 operating modes offer externally controlled or on-chip automatic access and externally controlled refresh. An on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The 74S408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and 6 control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All address output drivers are capable of driving 500pf loads with propagation delays of 25nsec. The 74S408 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capitance.

The 74S408 can drive up to 4 banks of DRAMs, with each bank comprised of 16K's, or 64K's. Control signal outputs $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the data output in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to our read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—$V_{CC} = 5V \pm 5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. Recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R7: Row Address Inputs.

C0-C7: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3).

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS}_n$ outputs in modes 0, 1, 2 and 3.

R/$\overline{C}$: Row/Column Select Input—Selects either the row or column address input latch onto the output bus.

$\overline{CASIN}$: Column Address Strobe Input—Inhibits $\overline{CAS}$ output when high in Modes 4 and 3. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; Latches on high-to-low transition.

$\overline{CS}$: Chip Select Input—Three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in mode 0, 1, 2). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 6 modes of operation of the 74S408 as depicted in Table 1.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low when M2 = 0 (modes 0, 1, 2 or 3) and the End-of-Count output is at 127 or 255 (see Table 3).

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 5 and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3 and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-7), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS}_n$ outputs go low together following $\overline{RASIN}$ going low.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 1. Memory Bank Decode

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 4-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S408s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S408 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$, 500pF loads for Q_0-Q_7 and $\overline{WE}$, and 150 pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6). The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S408 Driving Any 16K, 64K or 256K DRAMs

The 74S408 can drive any 16K or 64K DRAMs. The on-chip 8-bit counter with selectable End-of-Count can support refresh of 128 or 512 rows while the 8 address and 4 $\overline{RAS}_n$ output can address 4 banks of 16K or 64K DRAMS.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and DATA at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S408, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S408 Functional Mode Description

The 74S408 operates in 6 different functional modes. The operating mode is selected by signals M_0, M_1, M_2. Selecting M_2, M_1, M_0 = 0,0,0 or 0,0,1 or 0,1,0 will result at the same operating mode designated as mode 0,1,2 (see Table 2).

MODE	($\overline{RFSH}$) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0,1,2	0	0	0	Externally controlled refresh	RF I/O = EOC
	0	0	1		
	0	1	0		
3	0	1	1	Externally controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count	See Table 3 for Mode 7

Table 2. 74S408 Mode Select Options

74S408 Functional Mode Descriptions

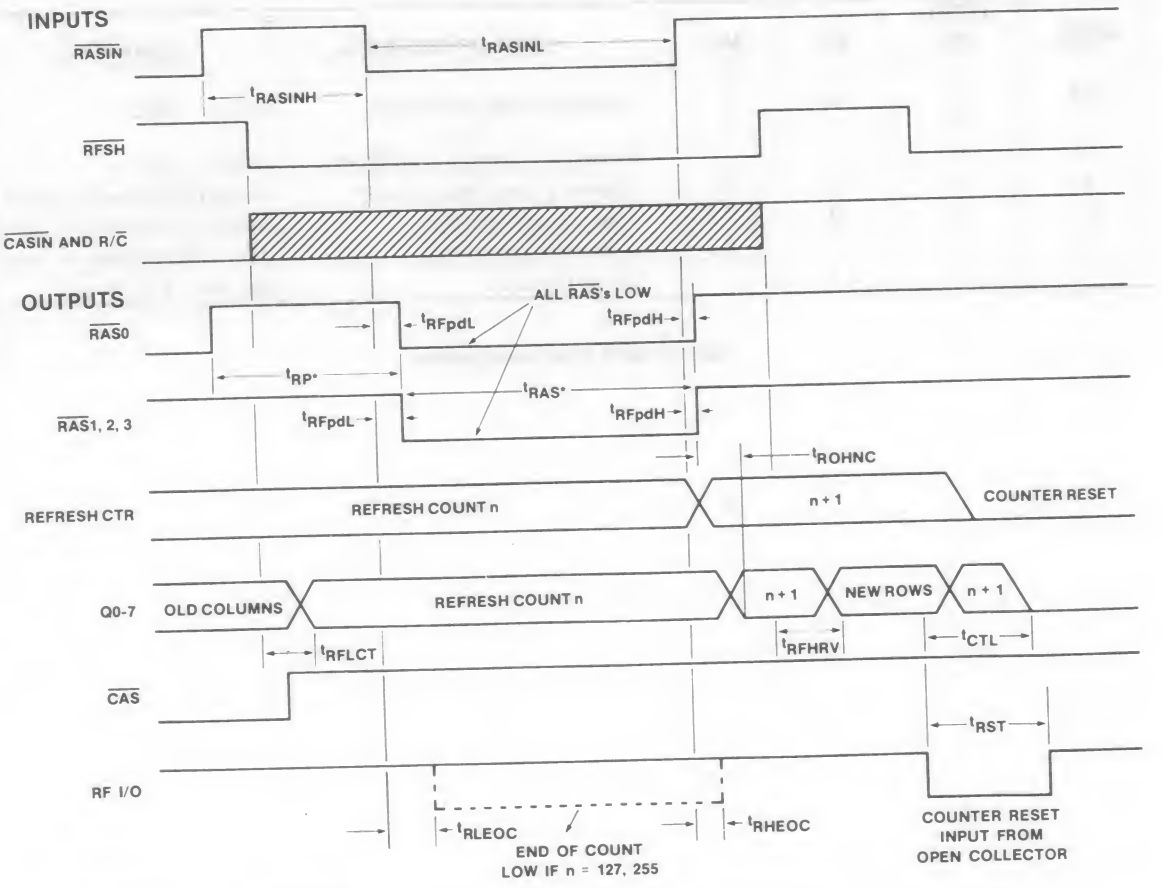
Modes 0, 1, 2—Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled onto R_0-R_7 outputs, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $M_2(\overline{RFSH})$ goes low-to-high while the other is low. RF I/O goes low when the count is 127 or 255 with $\overline{RASIN}$ and $\overline{RFSH}$ as set by End-of-Count (see Table 3), low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and $M_2(\overline{RFSH})$ can transition low simultaneously because the refresh counter becomes valid on the output but t_{RFLCT}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMS (see Figure 2). To perform externally controlled burst refresh $M_2(\overline{RFSH})$ initially can again have the same edge as $\overline{RASIN}$, but then can maintain a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

Mode 3—Externally Controlled All-$\overline{RAS}$ Write

This mode is useful at system initialization. The memory address is provided by the processor, which also perform the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S408 for the next write cycle.



*INDICATES DYNAMIC RAM PARAMETERS

Figure 2. External Control Refresh Cycle (Modes 0, 1, 2)

Mode 4—Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

Output Address Selection

Refer to Figure 4a. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q7. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/C. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 4b). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 20 ns after the column addresses are valid, or about 60 ns after R/$\overline{C}$ goes low (see Figure 4a). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay (t_{RPDL} + t_{RAH} − t_{RHA}) after RASIN goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

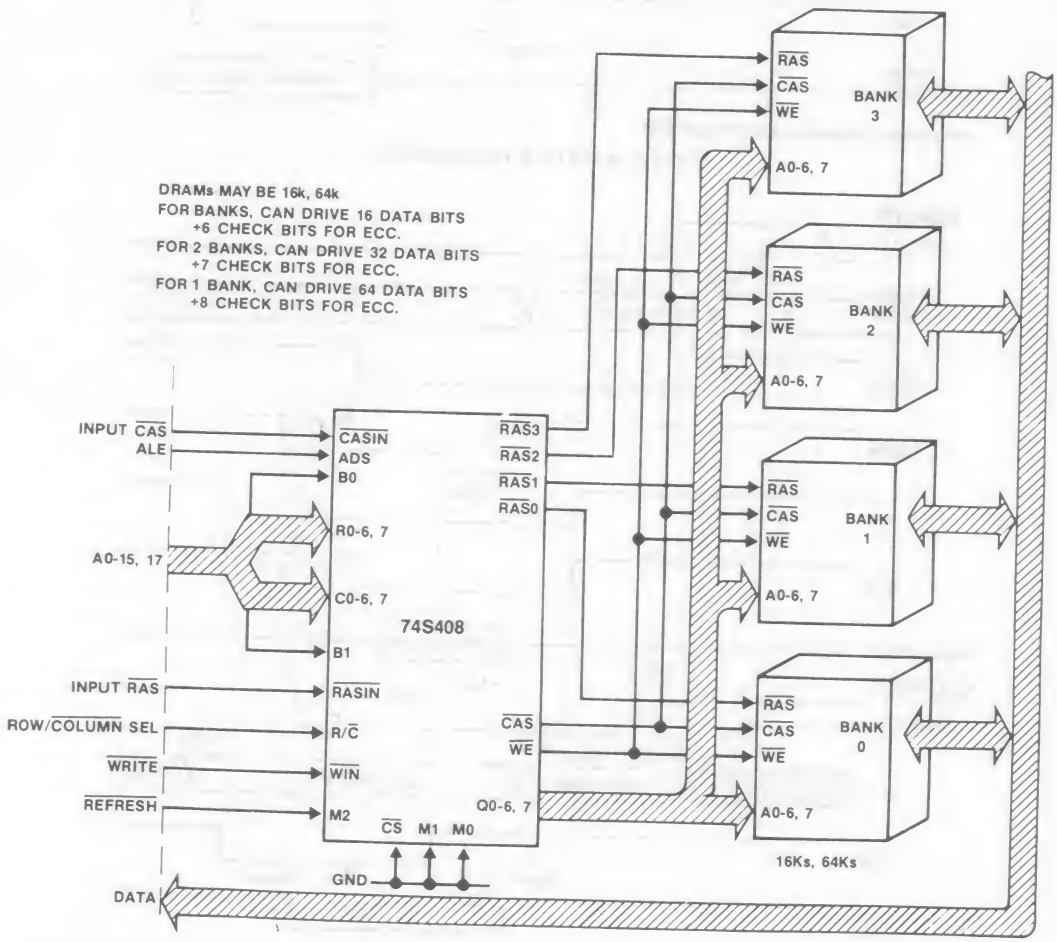
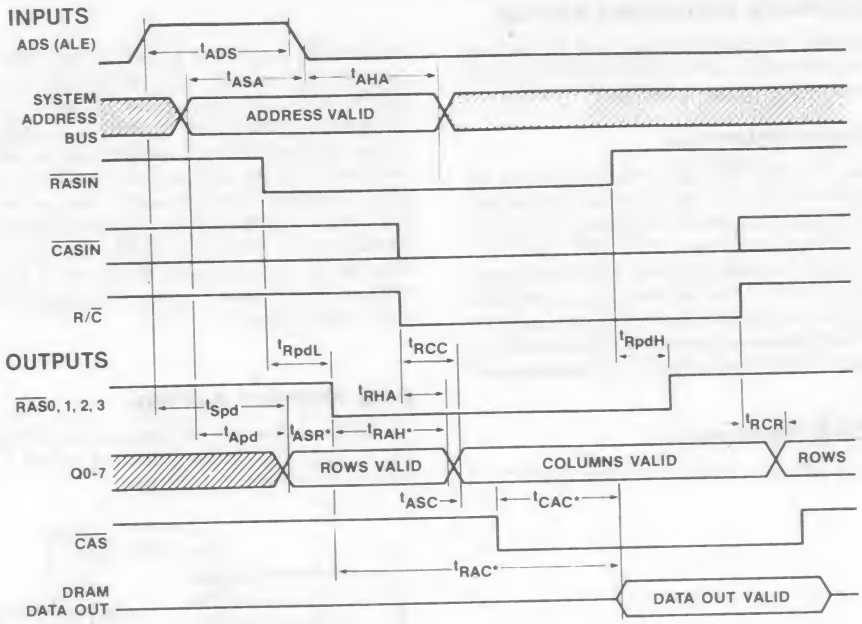
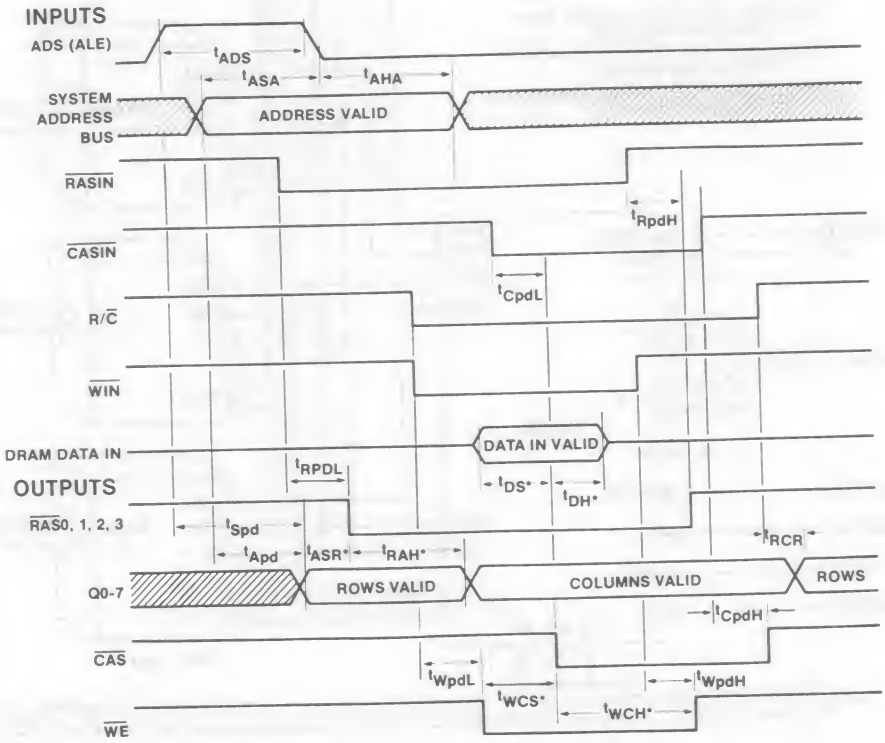


Figure 3. Typical Application of 74S408 Using Externally Controlled Access and Refresh in Modes 0 and 4



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4a. Read Cycle Timing (Mode 4)



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4b. Write Cycle Timing (Mode 4)

Mode 5—Automatic Access

In the Auto Access mode all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. Inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and the output control signals are derived internally from one input signal ($\overline{RASIN}$) minimizing timing-skew problems, thereby reducing memory access time substantially and allowing use of slower DRAMs.

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the 74S408 in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S408. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S408 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 5a).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

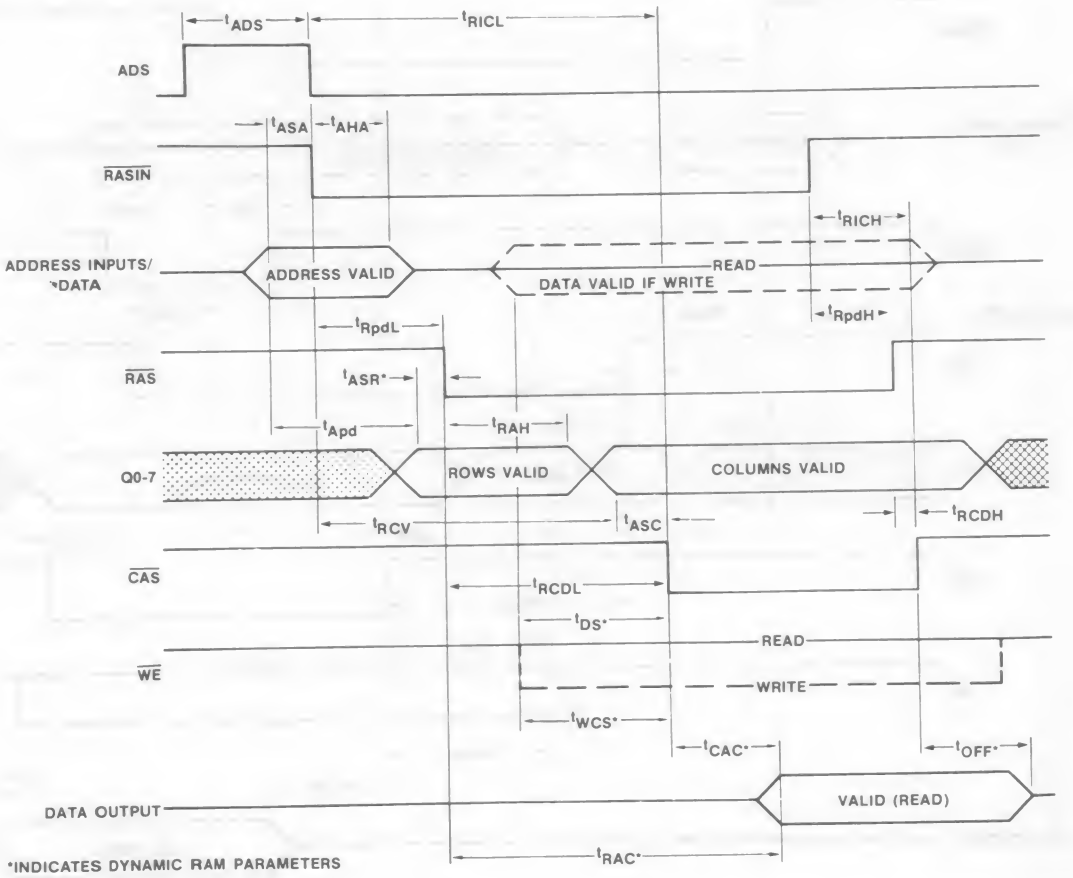


Figure 5a. Modes 5, 6 Timing ($\overline{CASIN}$ High in Mode 6)

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Mode 6—Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ pin is not used, but $\overline{CASIN}$ is used to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

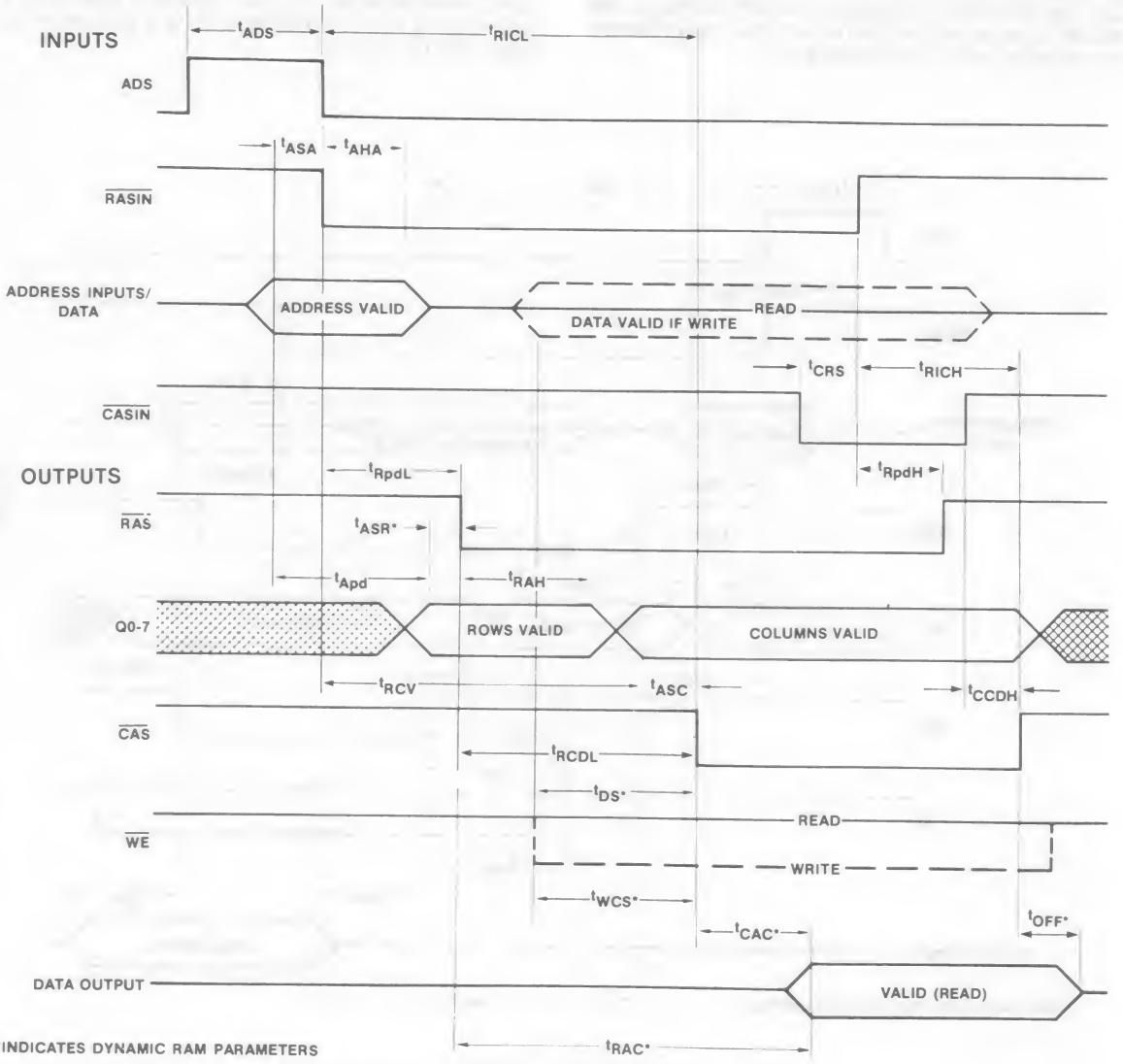


Figure 5b. Mode 6 Timing, Extended CAS

Mode 7—Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	127
1	1	127

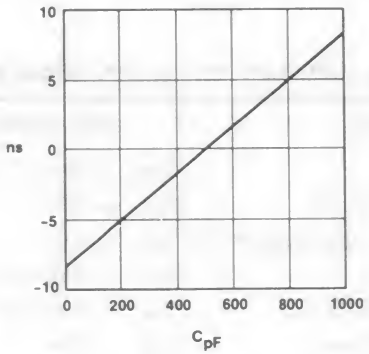


Figure 6. Change in Propagation Delay vs Loading Capacitance Relative to a 500pF Load

SN74S408/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC} ..... −0.5V to 7.0V
Storage Temperature Range ..... −65°C to +150°C
Input Voltage ..... −1.5V to 5.5V
Output Current ..... 150 mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75		5.25	4.25		5.25	V
T_A	Ambient temperature		0		+70	0		+70	°C
t_{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4a,4b,5a,5b	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4a,4b,5a,5b	30			30			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			50			ns
t_{RST}	counter reset pulse width	Figure 2	70			70			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 70°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only.	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_IRSI	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mA
I_ICTL	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0	V		
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_1D	Output high drive current except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_0D	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	THREE-STATE output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		210	285	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

Switching Characteristics: V_{CC} = 5.0V ±5.0%, 0°C T_A 70°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	40	48	60	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	50	63	80	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5b	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 5a		90	120		30	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figure 5a		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figure 4b,4a		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Fibure 4b,4a		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	30	60	15	30	60	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RiC) low in Mode 4)	Figure 4b	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 4b	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4a		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figure 4a,4b		40	58		40	58	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	CS = X , Figure 2		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figure 2		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figure 2		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80			80	ns
t_{RAHI}	Row address hold time (Mode 5)	Figure 5a	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 5a,5b	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 5a	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 5a,5b	6			3			ns
t_{RHA}	Row address held from column select	Figure 4a	10			10			ns
t_{CRS}	$\overline{Casin}$ setup time to $\overline{Rasin}$ high (Mode 6)	Figure 5b	35			35			ns

Switching Characteristics: (Cont.)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408			'S408-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from HI—Z	Figure 8 R1 = 3.5k, R2 = 1.5K		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15p, Figure 8 R2 = 1k, S1 open		20	40		20	40	ns
T_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figure 8 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figure 8 R1 = 1k, S2 open		25	50		25	50	ns
T_{HZH}	$\overline{CS}$ low to control output high from Hi-Z high	Figure 8 R2 = 750 Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output Hi-Z high from high	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		40	75		45	75	ns
t_{HZL}	$\overline{CS}$ low to control output low from Hi-Z high*	Figure 8, S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output Hi-Z high from low*	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		50	80		50	80	ms

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $\overline{WE}$ C_L = 500 pF; $\overline{RAS}$ C_L = 150 pF; $\overline{CAS}$ C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25° and V_C = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

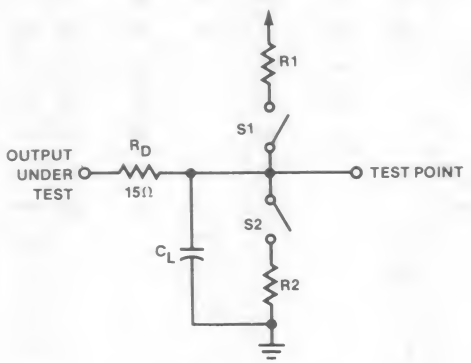


Figure 7. Standard Test Load

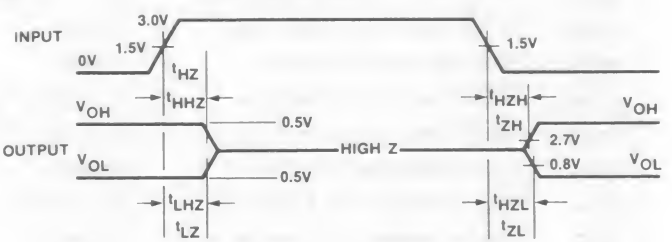


Figure 8. Waveform

SN74S408-3 Specifications:

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC} ..... −0.5V to 7.0V
Storage Temperature Range ..... −65°C to +150°C
Input Voltage ..... −1.5V to 5.5V
Output Current ..... 150 mA
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S408-3 MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
T_A	Ambient temperature		0		+70	°C
t_{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15			ns
t_{AHA}	Address hold time from ADS	Figures 4a,4b,5a,5b	15			ns
t_{ADS}	Address strobe pulse width	Figures 4a,4b,5a,5b	30			ns
t_{RHA}	Row address held from column select	Figure 4a	10			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			ns
t_{RST}	counter reset pulse width	Figure 2	70			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 70°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only.	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mA
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0	V		
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	THREE-STATE output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		210	285	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

1

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 70°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408-3 MIN	'S408-3 TYP	'S408-3 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 5a,5b		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 5a		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5a		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 5b	40	54	80	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 5a		90	140	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figure 5a		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4a,4b,5a,5b	15	23	37	ns
t_{APDL}	Address input to output low delay	Figures 4a,4b,5a,5b		25	46	ns
t_{APDH}	Address input to output high delay	Figures 4a,4b,5a,5b		25	46	ns
t_{SPDL}	Address strobe to address output low	Figure 4b,4a		40	70	ns
t_{SPDH}	Address strobe to address output high	Figure 4b,4a		40	70	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 4b	15	30	70	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RiC) low in Mode 4)	Figure 4b	32	41	67	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 4b	25	39	60	ns
t_{RCC}	Column select to column address valid	Figure 4a		40	67	ns
t_{RCR}	Row select to row address valid	Figure 4a,4b		40	67	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figure 2	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	CS = X , Figure 2		47	70	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figure 2		45	70	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figure 2		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2		80	ns	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80	ns
t_{RAHI}	Row address hold time (Mode 5)	Figure 5a	30			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 5a,5b	20			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 5a	8			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 5a,5b	6			ns
t_{RHA}	Row address held from column select	Figure 4a	10			ns
t_{CRS}	$\overline{Casin}$ setup time to $\overline{Rasin}$ high (Mode 6)	Figure 5b	35			ns

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C T_A 70°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S408-3 MIN	'S408-3 TYP	'S408-3 MAX	UNIT
	THREE-STATE PARAMETER					
t_{ZH}	$\overline{CS}$ low to address output high from HI—Z	Figure 8 R1 = 3.5k, R2 = 1.5K		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15p, Figure 8 R2 = 1k, S1 open		20	40	ns
T_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figure 8 R1 = 3.5k, R2 = 1.5k		35	50	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figure 8, R1 = 1k, S2 open		25	50	ns
T_{HZH}	$\overline{CS}$ low to control output high from Hi-Z high	Figure 8 R2 = 750 Ω, S1 open		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output Hi-Z high from high	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output low from Hi-Z high*	Figure 8, S1, S2 open		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output Hi-Z high from low*	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $\overline{WE}$ C_L = 500 pF; $\overline{RAS}$ C_L = 150 pF; $\overline{CAS}$ C_L = 600pF unless otherwise noted.

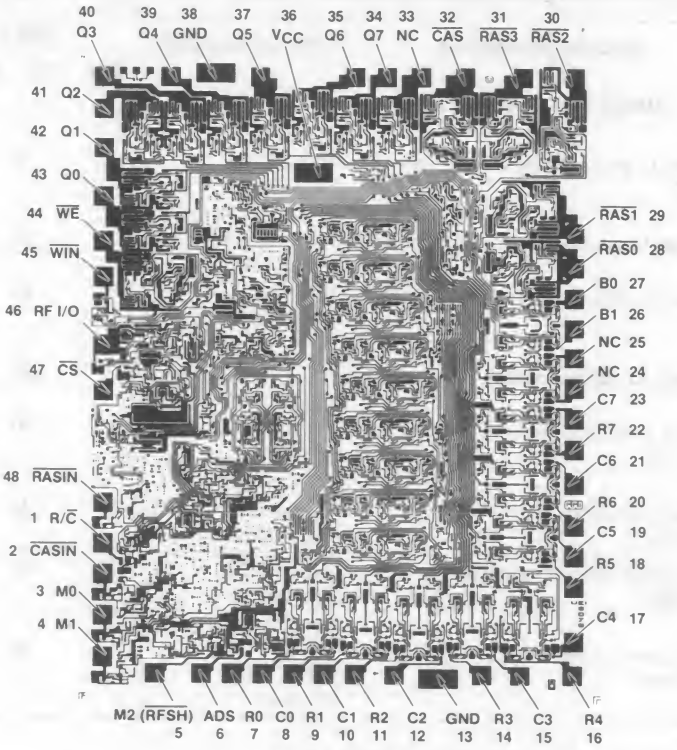
Note 2: All typical values are for T_A = 25° and V_C = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Die Configuration



DIE SIZE: 161 x 129 MIL

Multi-Mode Dynamic RAM Controller/Driver

SN74S409/DP8409
SN74S409-2/DP8409-2
SN74S409-3/DP8409-3

Features/Benefits

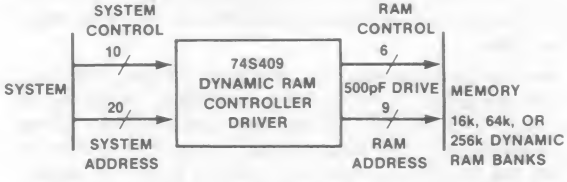
- All DRAM drive functions on one chip have on-chip high capacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K, 64K, and 256K DRAMs; capable of addressing up to 1M words
- Propagation delays of 25nsec typical at 500 pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- 8 modes of operation support externally controlled and automatic access and refresh, as well as special memory initialization access
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255, or 511)
- Direct replacement for National DP8409

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S409	N48, D48	COM
SN74S409-2	N48, D48	COM, SPEED OPTION
SN74S409-3	N48, D48	COM, AC OPTION

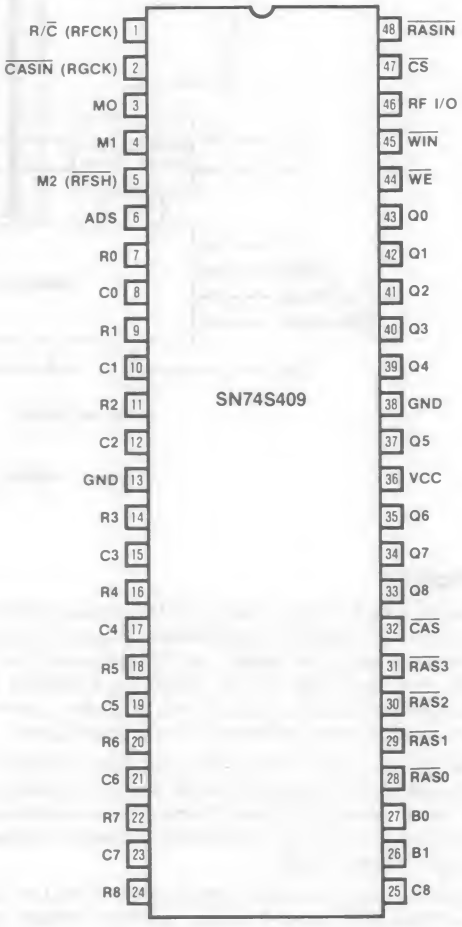
Operating Modes

0	Externally controlled fresh
1	Auto refresh – forced
2	Automatic burst refresh
3a	All-$\overline{RAS}$ auto write
3b	Externally controlled All-$\overline{RAS}$ write
4	Externally controlled access
5	Auto access, slow t_{RAH}, hidden refresh
6	Auto access, fast t_{RAH}
7	Set end of count



Interface Between System and DRAM Banks

Pin Configuration



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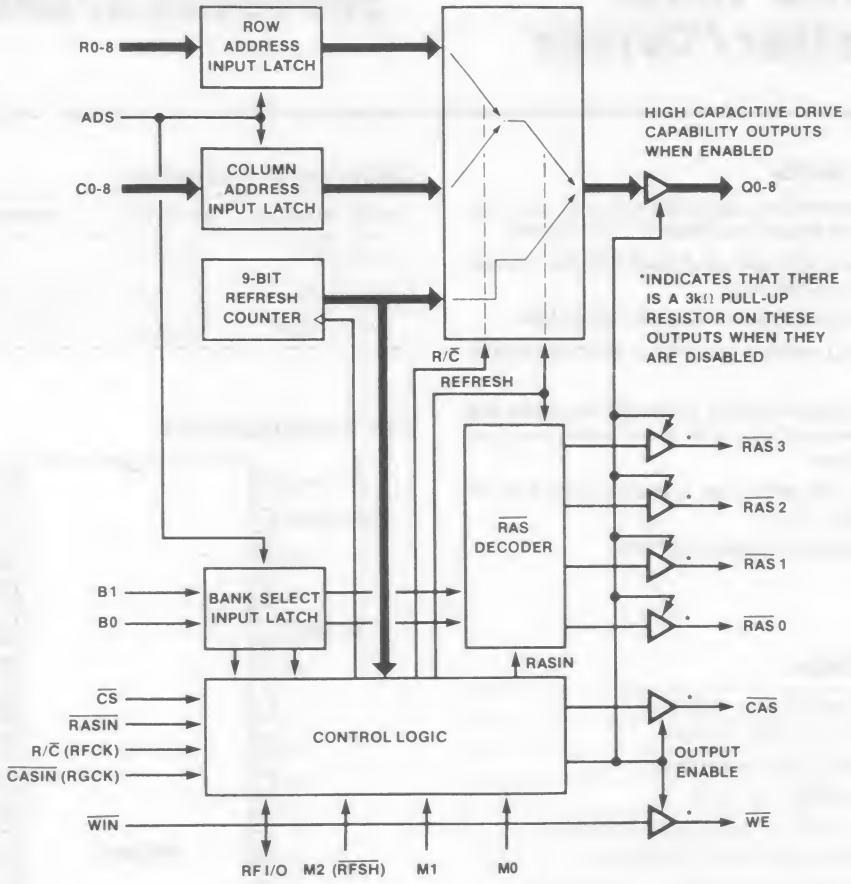

Figure 1. 74S409 Functional Block Diagram

Description

The 74S409 is a Multi-Mode Dynamic RAM Controller/Driver capable of directly driving up to 88 DRAMs. 20 address lines to the 74S409 allow it to address up to 1M words and it can drive 16K, 64K and 256K DRAMs. Since the 74S409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews and saves in board space.

The 74S409's 8 operating modes offer externally controlled or on-chip automatic access and refresh. An on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. The 74S409 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capacitance.

The 74S409 can drive up to 4 banks of DRAMs, with each bank comprised of 16K's, 64K's, or 256K's. Control signal outputs $\overline{CAS}$ and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the respective data outputs in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—V_{CC} = 5V ± 5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R8: Row Address Inputs.

C0-C8: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3), and select mode 3a or 3b.

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS}_n$ outputs in modes 0 and 3. $\overline{RASIN}$ input is disabled in modes 1 and 2.

R/$\overline{C}$ (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/$\overline{Column}$ Select Input, selecting either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK)—In modes 1, 2 and 3a, this pin is the $\overline{RAS}$ Generator Clock input. In all other modes it is $\overline{CASIN}$ (Column Address Strobe Input), which inhibits $\overline{CAS}$ output when high in Modes 3b and 4. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; Latches on high-to-low transition.

$\overline{CS}$: Chip Select Input—three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 2.

RF I/O ($\overline{RFRQ}$)—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0, 2 and 3a when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode (mode 5) it is the $\overline{Refresh}$ $\overline{Request}$ ($\overline{RFRQ}$) output.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 1. Memory Bank Decode

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 3a, 5, and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-6), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS}_n$ outputs go low together following $\overline{RASIN}$ going low in modes 0 and 3 and automatically in modes 1 and 2.

Input Addressing

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The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter.

The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid address until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the address is still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 3-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ goes high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S409 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$ and $\overline{WE}$, 500pF loads for Q_0-Q_8, and 150pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 14. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S409 Driving Any 16K, 64K or 256K DRAMs

The 74S409 can drive any 16K, 64K, or 256K DRAMs. The on-chip 9-bit counter with selectable End-of-Count can support refresh of 128, 256 and 512 rows while the 9 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K, 64K, or 256K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S409, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S409 Functional Modes Description

The 74S409 operates in 8 different functional modes selected by signals M_0,M_1,M_2. Mode 3 splits further to modes 3a and 3b determined by signals B_0,B_1 in mode 7.

Mode 0 and mode 1 are generally used as Refresh modes for mode 4 and mode 5 respectively, and therefore will be described as mode-pairs 0,4 and 1,5.

Mode 6 is a fast access made for very fast DRAMs and mode 7 is used only to determine choice of mode 3a or 3b and for setting End-of-Count for the refresh modes.

MODE	($\overline{RFSH}$) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0	0	0	0	Externally controlled refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto refresh—forced	RF I/O = Refresh request ($\overline{RFRQ}$)
2	0	1	0	Automatic burst refresh	RF I/O = $\overline{EOC}$
3a*	0	1	1	All-$\overline{RAS}$ auto write	RF I/O = $\overline{EOC}$; all $\overline{RAS}$ active
3b*	0	1	1	Externally controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}, hidden refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count; determines mode 3a or 3b	See Table 3 for Mode 7

*Mode 3a is selected by setting B_0,B_1 to 01, 00, or 10 in mode 7.
*Mode 3b is selected by setting B_1,B_0 to 11 in mode 7.

Table 2. 74S409 Mode Select Options

Mode 0 – Externally Controlled Refresh
Mode 4 – Externally Controlled Access

Modes 0 and 4 facilitate external control of all timing parameters associated with the DRAMs. These modes are independent modes of operation though generally used together in the same application as shown in Figure 2.

Mode 0 – Externally Controlled Refresh

In this mode the input address latches are disabled from the address outputs and the refresh counter is enabled. All $\overline{RAS}$ outputs go low following $\overline{RASIN}$ and refresh the enabled row in all four banks. $\overline{CASIN}$ and R/$\overline{C}$ inputs are not used and $\overline{CAS}$ is inhibited. The refresh counter increments when either $\overline{RASIN}$ or M2 ($\overline{RFSH}$) switch high while the other is still low.

RF I/O goes low when the count equals End-of-Count (as set in mode 7), when $\overline{RASIN}$ is low. The 9-bit counter will always roll-over to zero at 512, regardless of End-of-Count. However, the counter can be reset at any time by driving RF I/O low through an external open-collector.

During refresh, $\overline{RASIN}$ and M2 ($\overline{RFSH}$) can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after $\overline{RFSH}$ goes low, which is a shorter time than t_{RFPDL}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMs (see Figure 2.). To perform externally controlled burst refresh, $\overline{RFSH}$ initially can again have the same edge as $\overline{RASIN}$, but then maintains a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

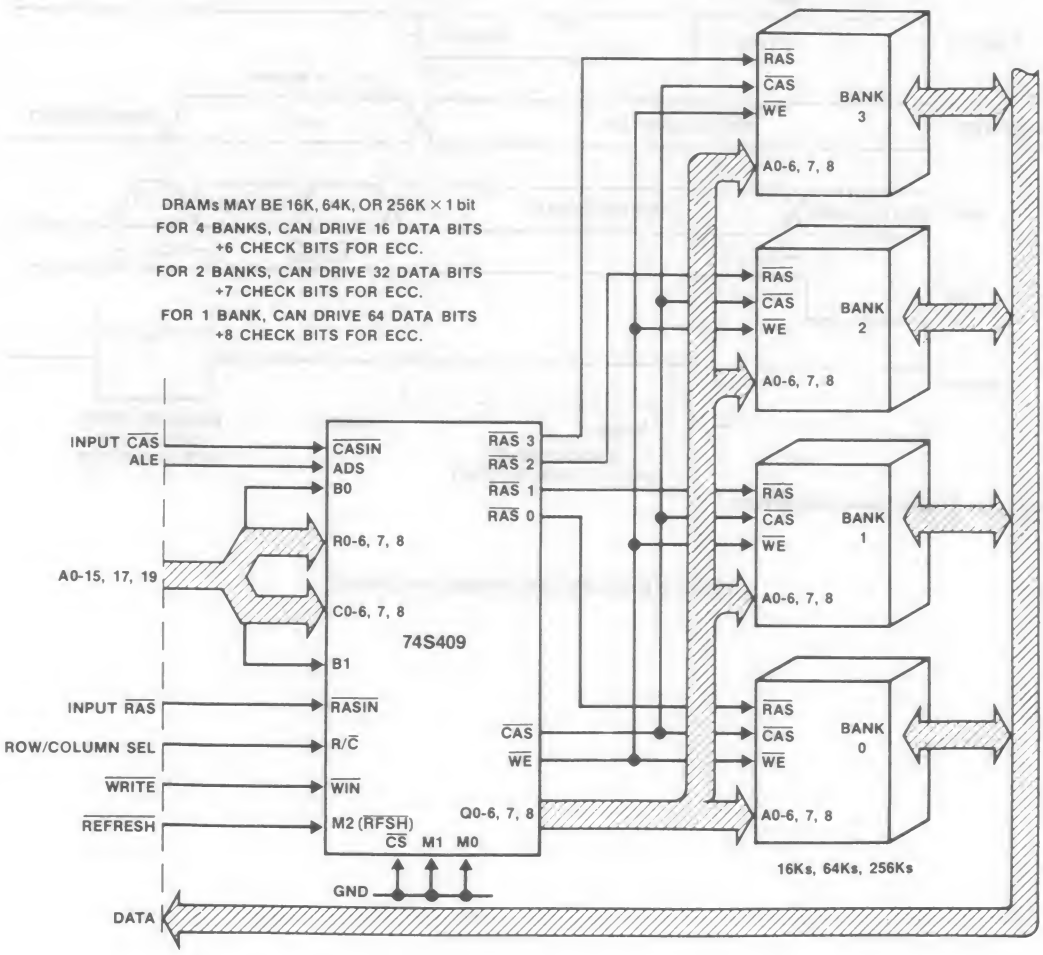


Figure 2. Typical Application of 74S409 Using Externally Controlled Access and Refresh in Modes 0 and 4

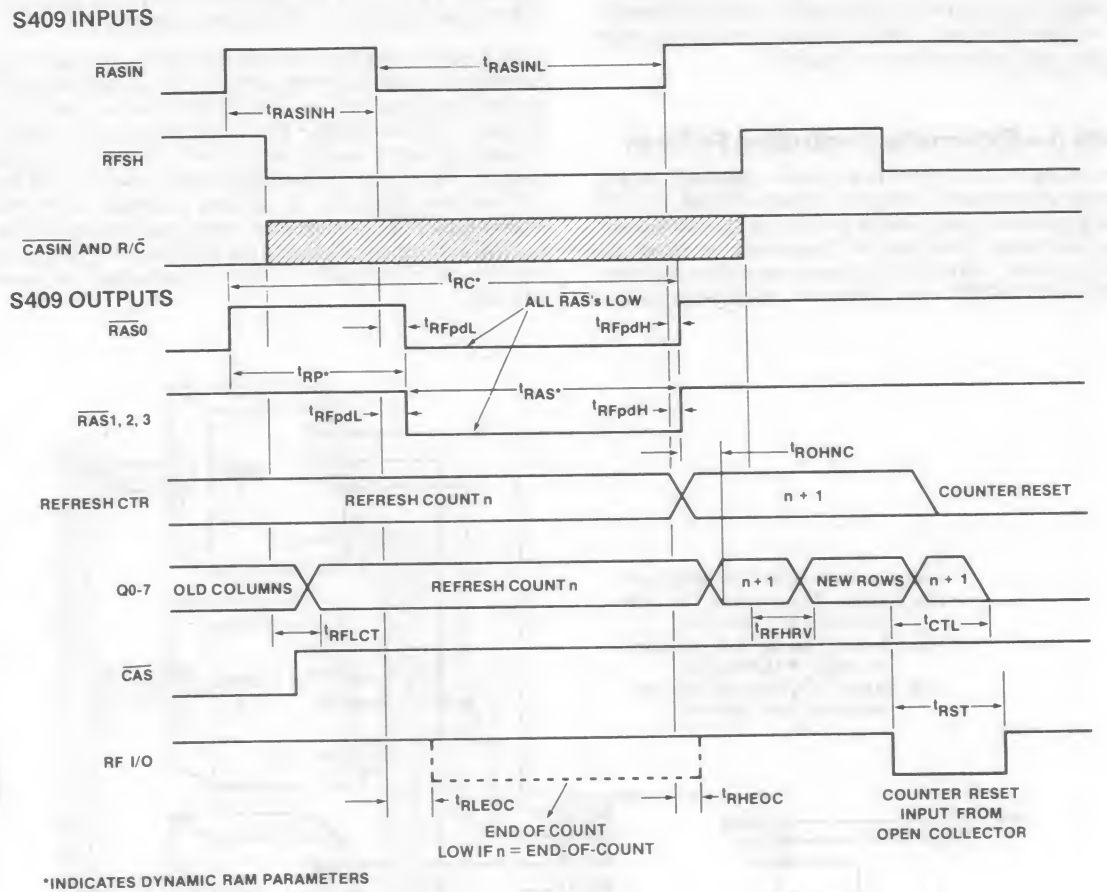


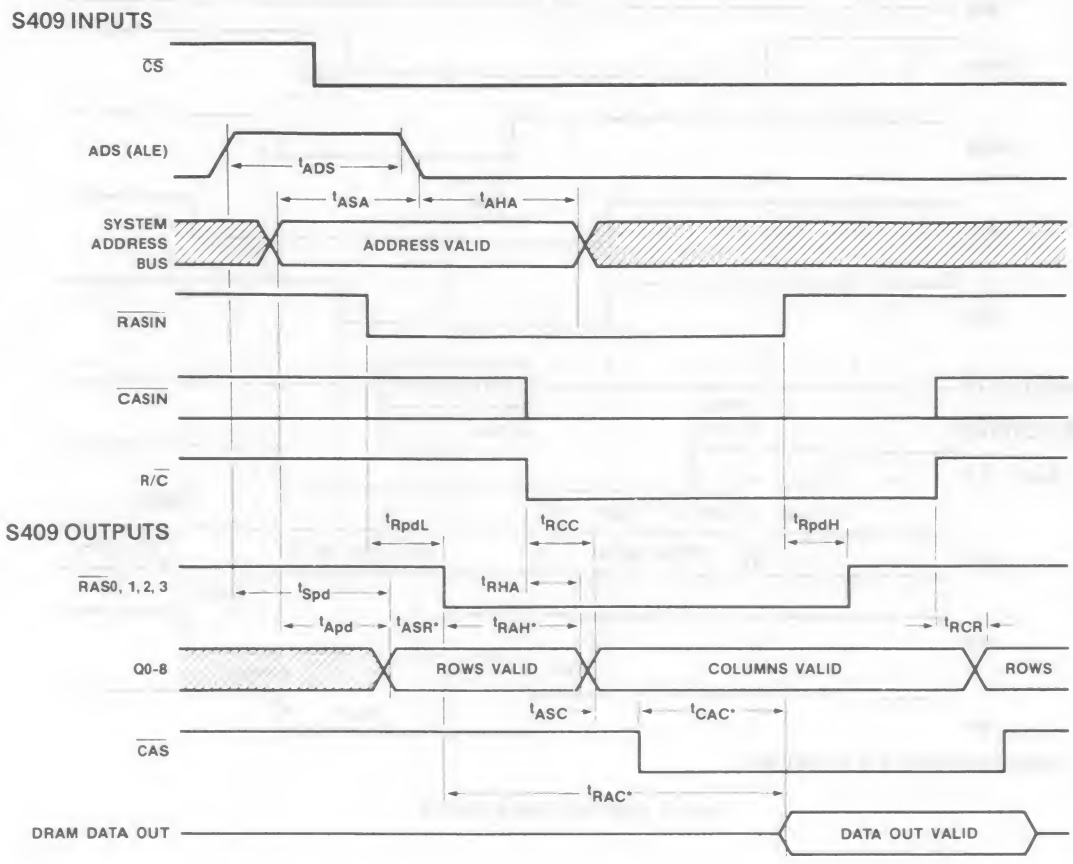
Figure 3. External Control Refresh Cycle (Mode 0)

Mode 4 – Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. Figures 4 and 5 show the timing for read and write cycles.

Output Address Selection

In this mode $\overline{CS}$ has to be low at least 50 nsec before the outputs will be valid. With R/$\overline{C}$ high, the row address latch contents are transfered to the multiplexed address bus output Q0-Q8. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q8 and enables one $\overline{RAS}$ output selected by signals B0, B1 to strobe the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 nsec later, the column address appears on the Q output.



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4. Read Cycle Timing (Mode 4)

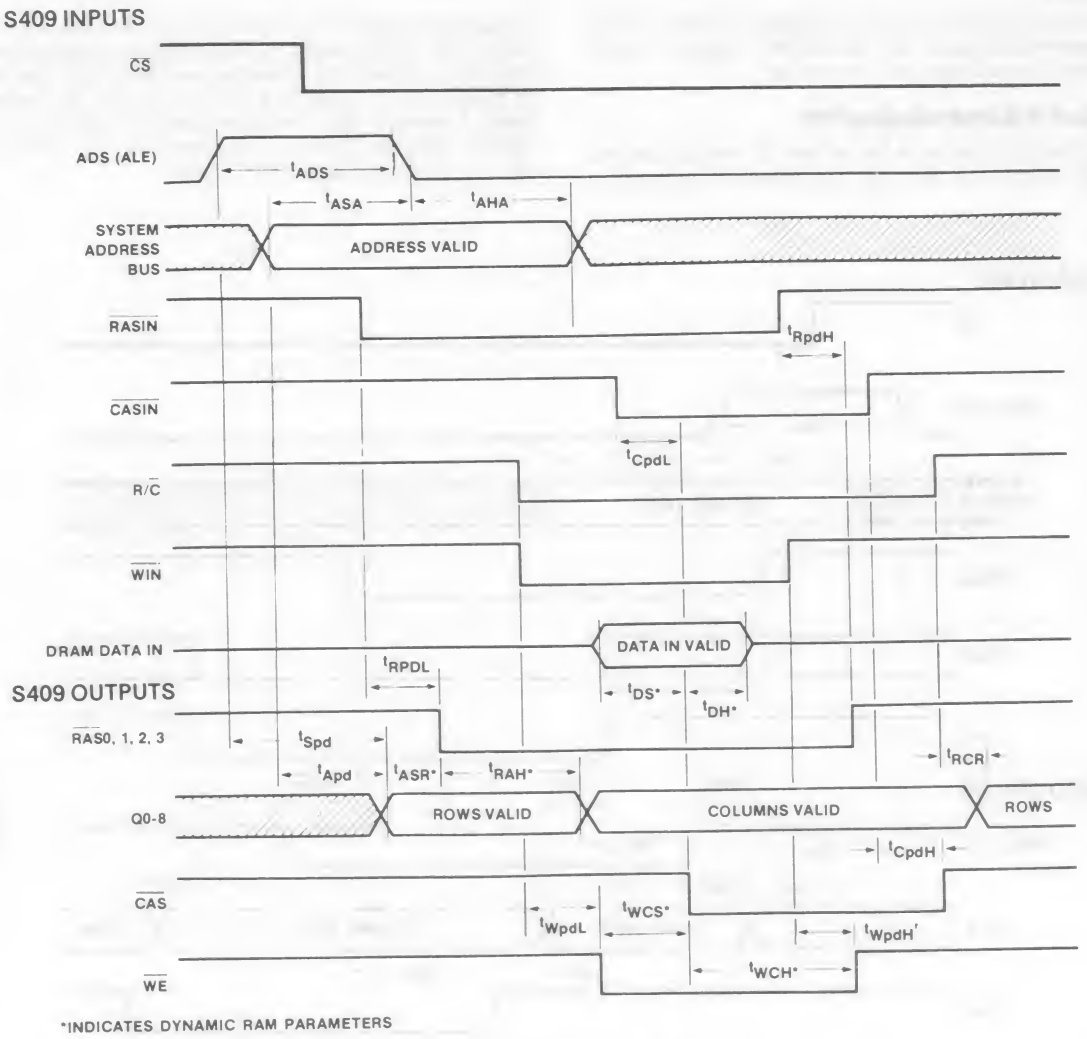


Figure 5. Write Cycle Timing (Mode 4)

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 5). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 60 ns after R/$\overline{C}$ goes low (see Figure 4). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay (t_{RPDL} + t_{RAH} − t_{RHA}) after $\overline{RASIN}$ goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

Mode 1 – Automatic Forced Refresh
Mode 5 – Automatic Access with Hidden Refresh

Mode 1 and Mode 5 are generally used together incorporating the advantages of the "hidden refresh" performed in mode 5 with the possibility to force a refresh, by changing to mode 1. An advantage of the Automatic Access over the Externally Controlled Access is the reduced memory access time due to the fact that the output control signals are derived internally from one input signal ($\overline{RASIN}$).

Hidden and Forced Refresh

Hidden Refresh is a term describing memory refresh performed when the system does not access the portion of memory controlled by the 74S409 ($\overline{CS} = 1$). A hidden refresh will occur once per Refresh Clock (RFCK) cycle provided $\overline{CS}$ went high and $\overline{RASIN}$ went low. If no hidden refresh occurred while RFCK was high, the RF I/O ($\overline{RFRQ}$) goes low immediately after RFCK goes low indicating to the system then a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low by driving M2 ($\overline{RFSH}$) low thereby changing mode of operation to mode 1.

The $\overline{\text{Refresh Request}}$ on RF I/O ($\overline{RFRQ}$) is terminated as soon as $\overline{RAS}$ goes low, indicating to the system that the foced refresh has been done. The system should then drive M2 ($\overline{RFSH}$) high changing mode of operation back to 5 (see Figure 6).

Mode 1 – Automatic Forced Refresh

In Mode 1, the R/$\overline{C}$ (RFCK) pin functions as RFCK (refresh cycle clock) instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high, then whenever M2 ($\overline{RFSH}$) goes low, an externally controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but can be set low externally through an open-collector driver, to reset the refresh counter.

If RFCK is an input clock, one and only one refresh cycle must take place every RFCK cycle. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O ($\overline{\text{Refresh Request}}$) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low The $\overline{\text{Refresh Request}}$ signal on RF I/O may be connected to a $\overline{\text{Hold}}$ or $\overline{\text{Bus Request}}$ input to the system. The system acknowledges the $\overline{\text{Hold}}$ or $\overline{\text{Bus Request}}$ when ready, and outputs $\overline{\text{Hold Acknowledge}}$ or $\overline{\text{Bus Request Acknowledge}}$. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the S409, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, strobing the refresh counter contents on the address ouputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock (RGCK) is requred for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low $t_{\overline{RFSRG}}$ before the next falling edge of RGCK. The $\overline{\text{Refresh Request}}$ on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may go high earlier than t_{FRQH} after RF I/O goes high and $\overline{RAS}$ will go high t_{RFRH} after M2.

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Mode 5 – Automatic Access with Hidden Refresh

In this mode all address outputs, $\overline{RAS}$ and $\overline{CAS}$ are initiated from $\overline{RASIN}$ making the DRAM access appear similar to static RAM access. The hidden refresh feature enables DRAM refresh accomplished with no time-loss to the system.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASR} before ADS went low (see Figure 7).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

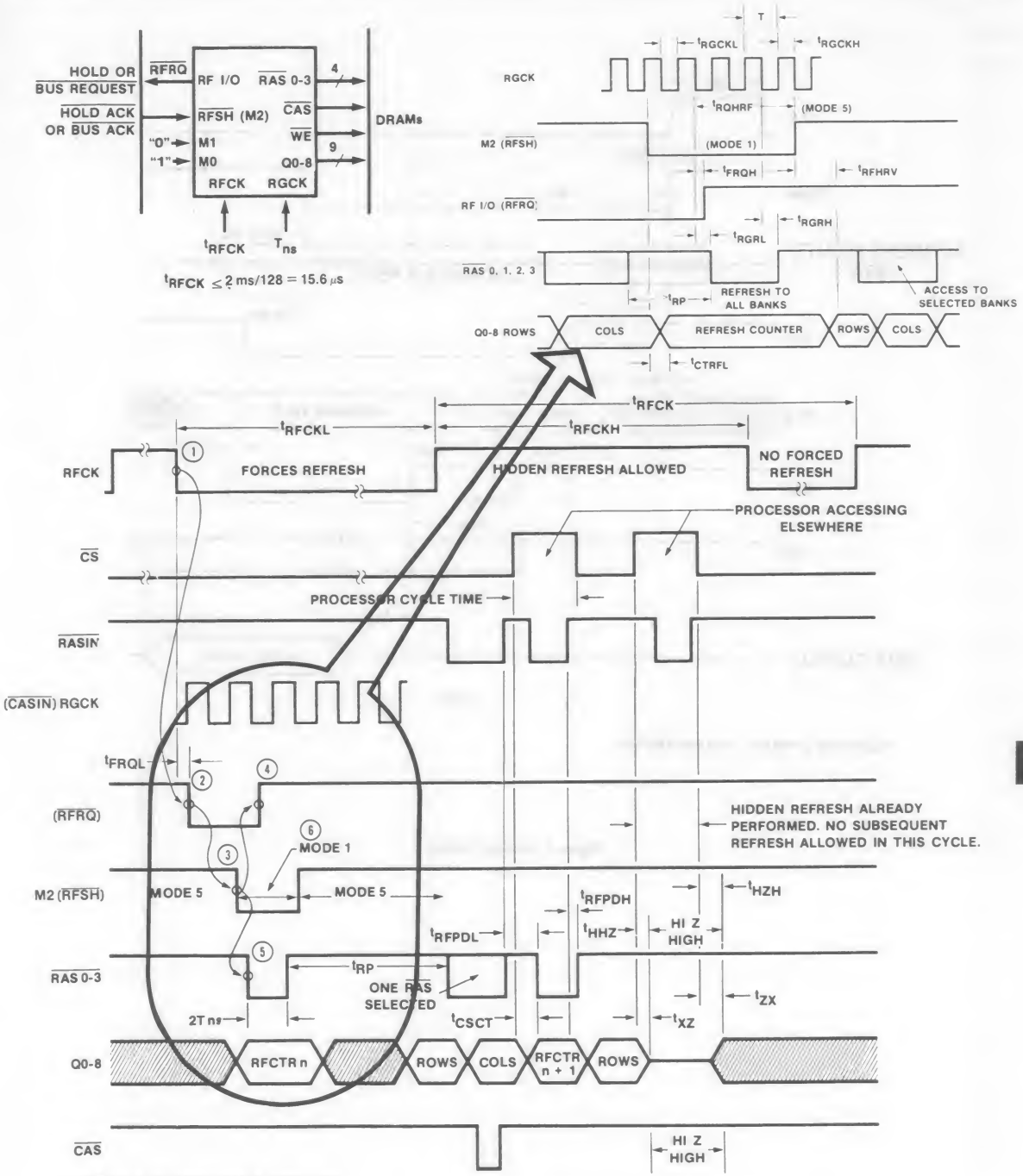
Refreshing

In this mode R/$\overline{C}$ (RFCK) functions as Refresh Clock and $\overline{CASIN}$ (RGCK) functions as $\overline{RAS}$ Generator Clock.

One refresh cycle must occur during each refresh clock period and then the refresh address must be incremented to the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16k and 64k DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flip-flop. First the 74S409 will attempt to perform a hidden refresh so that the system thruput will 74S409 goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flip-flop is reset so no further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK (see Figure 6). $\overline{RASIN}$ should go low at least 20 ns before RFCK goes low to ensure occurrence of the hidden refresh.

To determine the probability of a Hidden Refresh occurring, assume each system cycle takes 400 ns and RFCK is high for 8μs, then the system has 20 chances to not select the 74S409. If during this time a hidden refresh did not occur, then the 74S409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 6. The internal refresh request flip-flop is then reset.

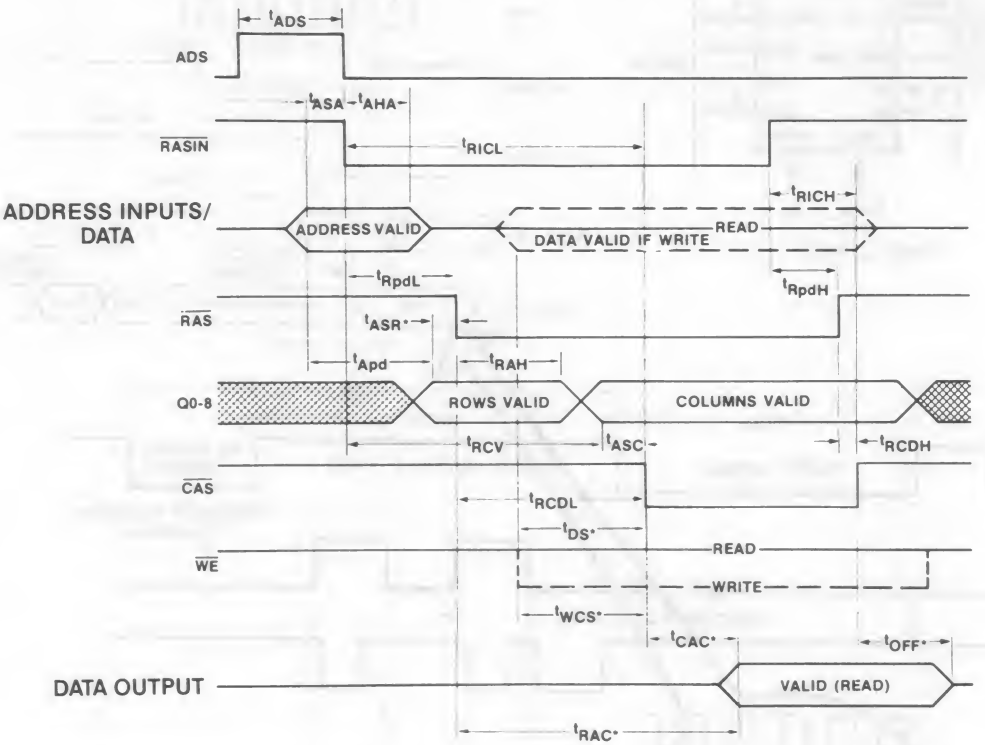
Figure 6 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go three-state until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50-percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.



*INDICATES DYNAMIC RAM PARAMETERS

1. RFCK GOES LOW
2. RFRQ GOES LOW IN NO HIDDEN REFRESH OCCURRED WHILE RFCK WAS HIGH
3. M2 (RFSH) DRIVEN LOW EXTERNALLY
4. REFRESH REQUEST RELEASED
5. RAS 0-3 GO LOW TO PERFORM REFRESH
6. M2 (RFSH) RELEASED

Figure 6. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing



*INDICATES DYNAMIC RAM PARAMETERS

Figure 7. Mode 5 Timing

Mode 2 – Automatic Burst Refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 8). When the 74S409 enters this mode, $\overline{CASIN}$ (RGCK) becomes the $\overline{RAS}$ Generator Clock (RGCK), and $\overline{RASIN}$ is disabled. $\overline{CAS}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{RAS}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four $\overline{RAS}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{RAS}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{RAS}$, starting from the count it contained when the mode was entered. If this was zero, then for a RGCK with a 100 ns period with End-of Count set to 127, RF I/O will go low after 128 x 0.4μs, or 51.2μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-burst occurs (after 26 μs) power can then be removed from the 74S409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the 74S409.

Mode 3a – All-$\overline{RAS}$ Automatic Write

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{RAS}$ outputs are activated, as in refresh, and so are $\overline{CAS}$ and $\overline{WE}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations. The refresh counter is used to address the rows and $\overline{RAS}$ is low for two RGCK cycles and high for two cycles.

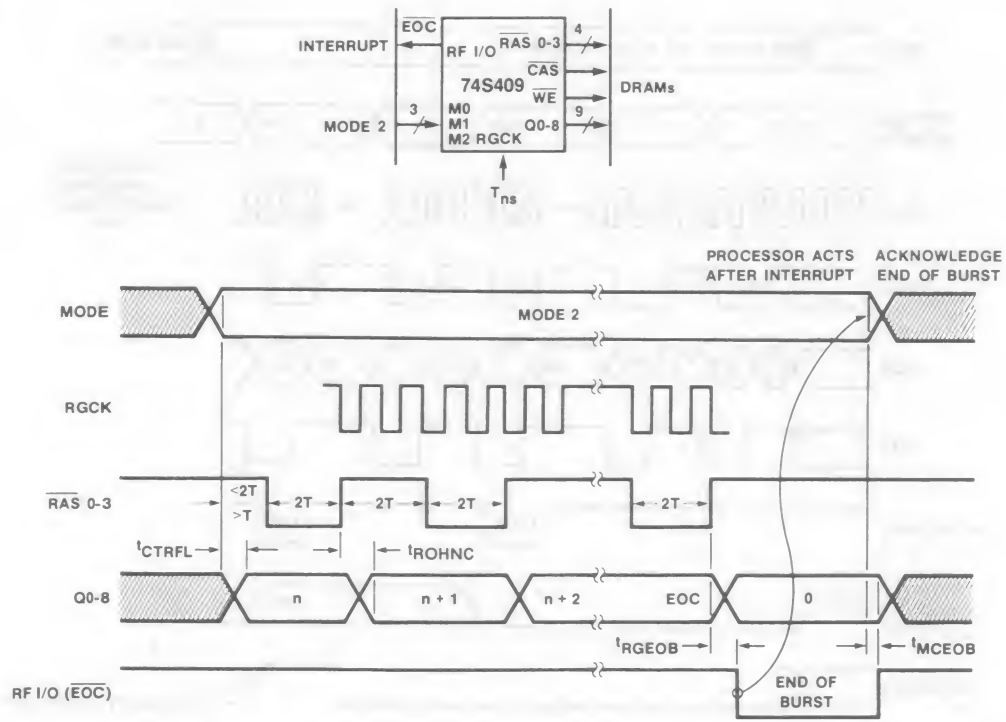
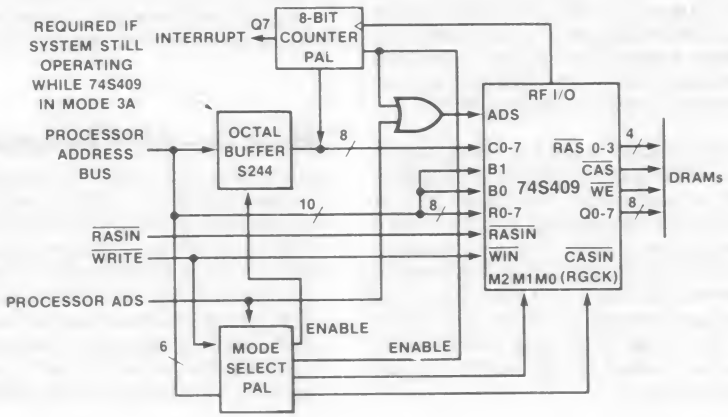


Figure 8. Auto-Burst Mode, Mode 2

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16K DRAMs, B1 and B0 are 00. For 64K DRAMs, B1 and B0 are 01.

In this mode, R/$\overline{C}$ is disabled, $\overline{WE}$ is permanently enabled low, and $\overline{CASIN}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{RAS}$ outputs are active.



74S409 Extra Circuitry Required for All-$\overline{RAS}$ Auto Write Mode, Mode 3a

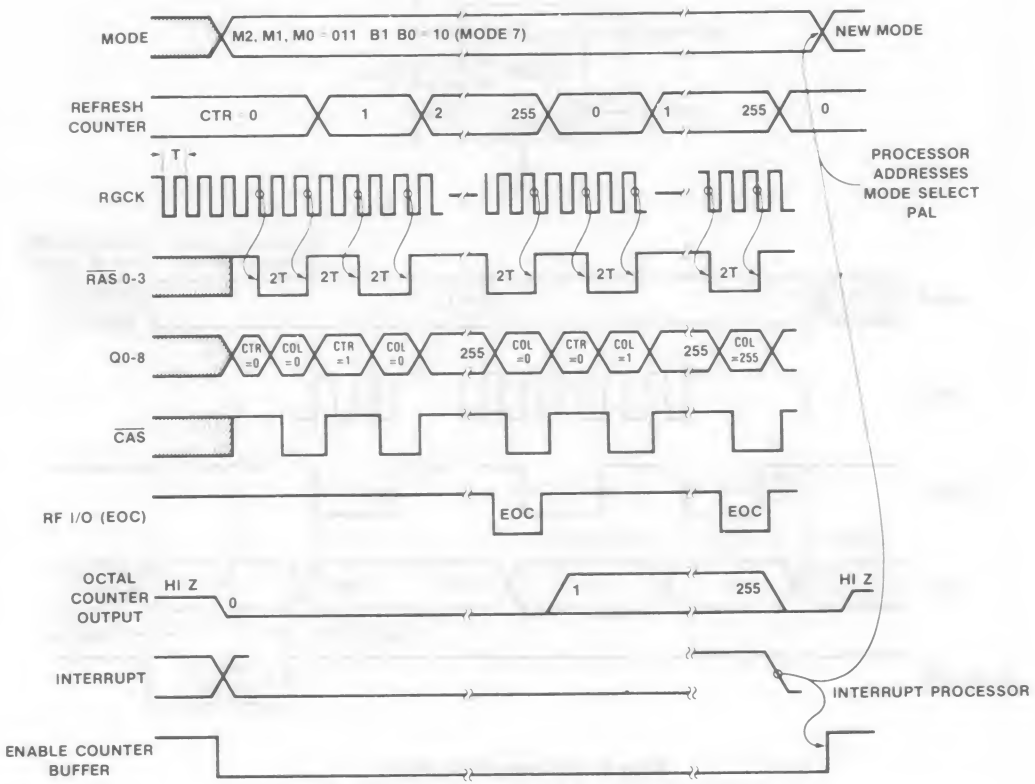


Figure 9. 74S409 All-$\overline{RAS}$ Auto Write Mode, Mode 3a, Timing Waveform

Mode 3b – Externally Controlled All-$\overline{RAS}$ Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

Mode 4 – Externally Controlled Access

Mode 4 is described in with mode 0 in section "Mode 0 and Mode 4."

Mode 5 – Automatic Access with Hidden Refresh

See description of mode 0 and mode 5.

Mode 6 – Fast Automatic Access

The Fast Automatic Access mode can only be used with fast DRAMs which have t_{RAH} of 10 nsec-15nsec. The typical $\overline{RASIN}$ to $\overline{CAS}$ delay is 105nsec. In this mode $\overline{CAS}$ can be extended after $\overline{RAS}$ goes high to extend the data output valid time. This feature is useful in applications with short cycle where $\overline{RAS}$ has to be terminated as soon as possible to meet the precharge (t_{RP}) requirements of the DRAM.

Mode 6 timing is illustrated in figures 10 and 11. Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 10).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (20 ns minimum); the column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 11.

Mode 7 – Set End-of-Count (3a, 3b select)

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

When B_1,B_2 are set to 11 in mode 7, mode 3b will be selected if mode 3 is selected (M_2, M_1, M_0 = 0, 1, 1). If B_1,B_2 is set to 00, 01 or 10 then mode 3a will be selected.

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

Table 3. Mode 7

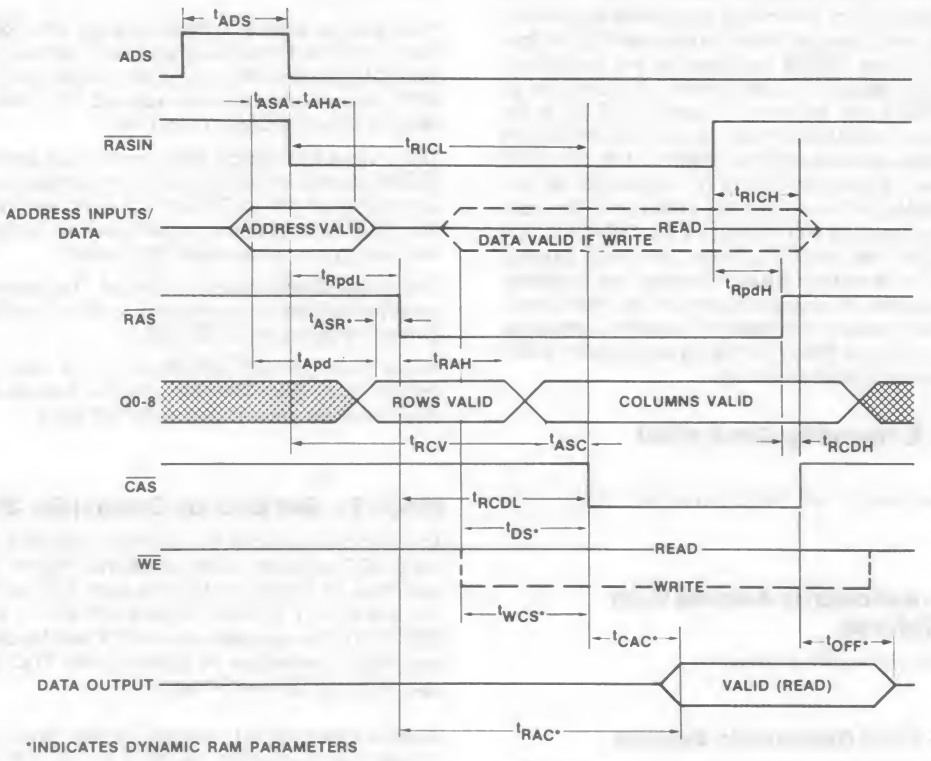


Figure 10. Mode 6 Timing ($\overline{\text{CASIN}}$ High)

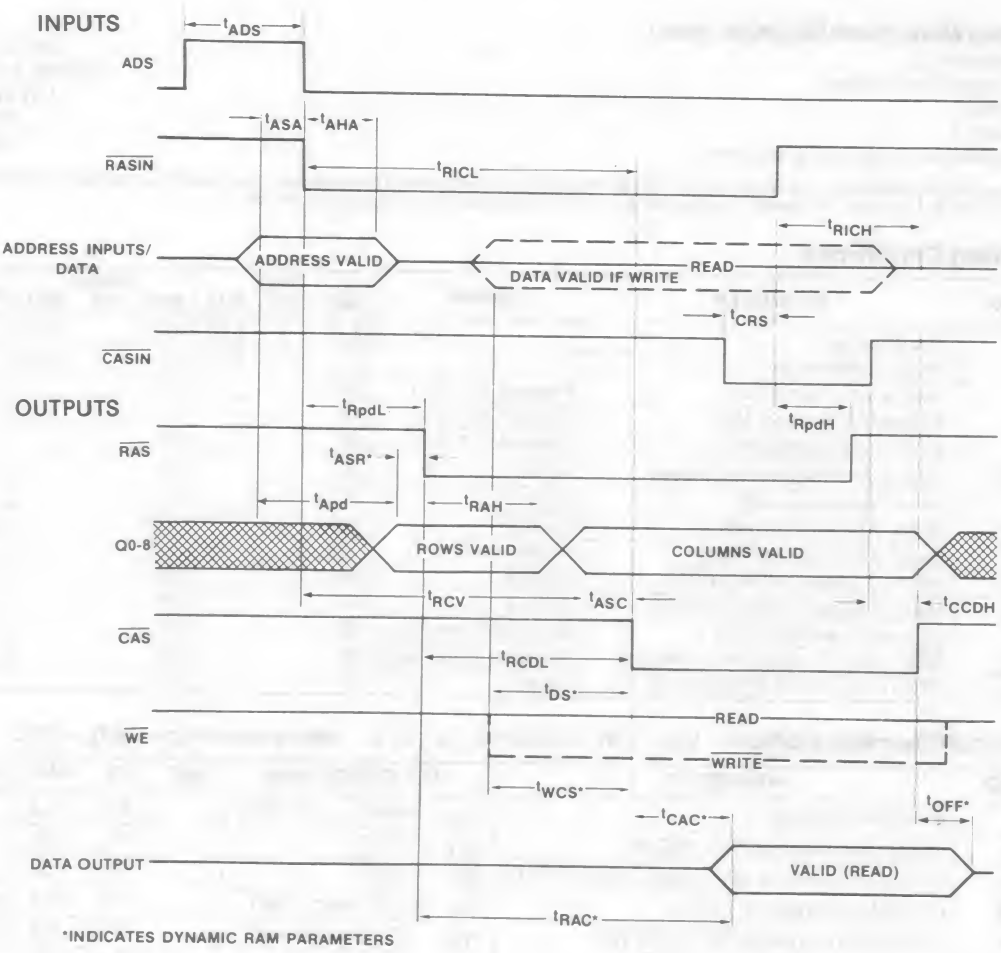


Figure 11. Mode 6 Timing, Extended $\overline{CAS}$

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SN74S409/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC} . . . . . −0.5V to 7.0V
Storage Temperature Range . . . . . −65°C to +150°C
Input Voltage . . . . . −1.5V to 5.5V
Output Current . . . . . 150 mA
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

*Note 1. "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Operating Conditions" provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
T_A	Ambient temperature		0		+70	0		+70	°C
t_{ASA}	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30			30			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 3	50			50			ns
t_{RST}	Counter reset pulse width	Figure 3	70			70			ns
$t_{RFCKL,H}$	Minimum pulse width of RFCK	Figure 6	100			100			ns
T	Period of $\overline{RAS}$ generator clock	Figure 6	100			100			ns
t_{RGCKL}	Minimum pulse width low of RGCK	Figure 6	35			35			ns
t_{RGCKH}	Minimum pulse width high of RGCK	Figure 6	35			35			ns
t_{CSRL}	$\overline{CS}$ low to access $\overline{RASIN}$ low	See Mode 5 description	10			10			ns
t_{RFSRG}	$\overline{RFSH}$ low set-up to RGCK low (Mode 1)	See Mode 1 description	35			35			ns
t_{RQHRF}	$\overline{RFSH}$ hold time from $\overline{RFRQ}$ (RF I/O)	Figure 6	2T			2T			ns

Electrical Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 70°C Typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS, R/C only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_IRSI	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mAV
I_ICTL	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselct		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS, R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	THREE-STATE output current (address outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

**These are absolute voltage with respect to pins 13 or 38 on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 70°C$ See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	ACCESS PARAMETER	FIGURE	'S409			'S409-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{RHA}	Row address held from column select	Figure 4	10			10			ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	40	48	60	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	50	63	80	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay Mode 6)	Figure 11	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figures 7, 10		90	120		80	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figures 7, 10, 11		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{APDH}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figures 4, 5		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Figures 4, 5		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	30	60	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ setup time to $\overline{RASIN}$ high (Mode 6)	Figure 11	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (R/C low in Mode 4)	Figure 5	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 5	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figures 4, 5		40	58		40	58	ns
t_{RAH}	Row address hold time (Mode 5)	Figures 7, 10	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 7, 10, 11	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figures 7, 10	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 7, 10, 11	6			3			ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	'S409			'S409-2			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{RFRQL}	RFCK low to forced $\overline{RFRQ}$ low	C_L = 50 pF, Figure 6		20	30		20	30	ns
t_{RFRQH}	RGCK low to force $\overline{RFRQ}$ high	C_L = 50pF, Figure 6		50	75		50	75	ns
t_{RGRL}	RGCK low to $\overline{RAS}$ low	Figure 6	50	65	95	50	65	95	ns
t_{RGRH}	RGCK low to $\overline{RAS}$ high	Figure 6	40	60	85	40	60	85	ns
t_{RFRH}	$\overline{RFSH}$ high to $\overline{RAS}$ high (encoding forced RFSH)	See Mode 1 description	55	80	110	55	80	110	ns
t_{CSCT}	$\overline{CS}$ high to $\overline{RFSH}$ counter valid	Figure 6		55	70		55	70	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 3			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	$\overline{CS}$ = X, Figures 3, 6, 8		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figures 3, 6		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figures 3, 8		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 3			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 3			80			80	ns
t_{RGEOB}	RGCK low to end-of-burst low	C_L = 50pF, Figure 8			95			95	ns
t_{MCEOB}	Mode change to end-of-burst high	C_L = 50pF, Figure 8			75			75	ns

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Switching Characteristics: (Cont'd)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 6, 13 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 6, 13 R2 = 1k, S1 Open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 6, 13 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 6, 14 R1 = 1k, S2 Open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-$\overline{3}$) high from Hi-Z high	Figures 6, 13 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-$\overline{3}$) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-$\overline{3}$) low from Hi-Z high	Figure 13 S1, S2 Open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-$\overline{3}$) Hi-Z high from low	C_L = 15pF, Figure 13, R2 = 750Ω, S1 open		50	80		50	80	ns

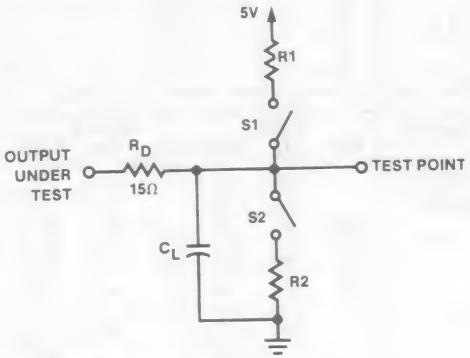
*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. C_L = 500pF; RAS0-RAS3, C_L = 150pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz. t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.



R1, R2 = 4.7K EXCEPT AS SPECIFIED.

Figure 12. Standard Test Load

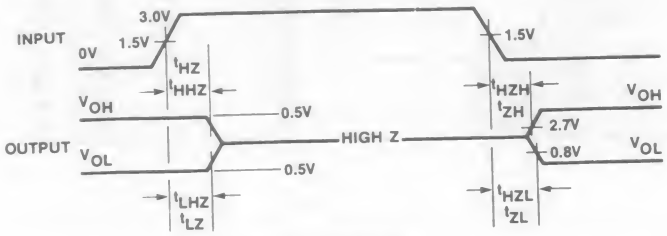


Figure 13. Waveform

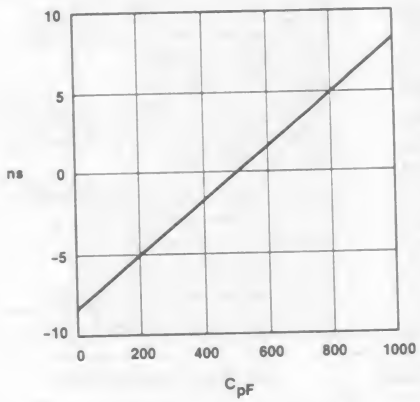


Figure 14. Change in Propagation Delay vs Loading Capacitance Relative to a 500 pF Load

SN74S409-3 Specifications:

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC} . . . . . −0.5V to 7.0V
Storage Temperature Range . . . . . −65°C to +150°C
Input Voltage . . . . . −1.5V to 5.5V
Output Current . . . . . 150 mA
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

*Note 1. "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Operating Conditions" provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S409-3 MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
T_A	Ambient temperature		0		+70	°C
t_{ASA}	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			ns
t_{AHA}	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			ns
t_{ADS}	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 3	50			ns
t_{RST}	Counter reset pulse width	Figure 3	70			ns
$t_{RFCKL,H}$	Minimum pulse width of RFCK	Figure 6	100			ns
T	Period of $\overline{RAS}$ generator clock	Figure 6	100			ns
t_{RGCKL}	Minimum pulse width low of RGCK	Figure 6	35			ns
t_{RGCKH}	Minimum pulse width high of RGCK	Figure 6	35			ns
t_{CSRL}	$\overline{CS}$ low to access $\overline{RASIN}$ low	See Mode 5 description	10			ns
t_{RFSRG}	$\overline{RFSH}$ low set-up to RGCK low (Mode 1)	See Mode 1 description	35			ns
t_{RQHRF}	$\overline{RFSH}$ hold time from $\overline{RFRQ}$ (RF I/O)	Figure 6	2T			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 70°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, $I_C = -12mA$		−0.8	−1.2	V
I_{IH1}	Input high current for ADS, R/C only	$V_{IN} = 2.5V$		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	$V_{IN} = 2.5V$		1.0	50	μA
I_IRSI	Output load current for RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mAV
I_ICTL	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselct		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS, R/$\overline{C}$ only	$V_{IN} = 0.5V$		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	$V_{IN} = 0.5V$		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	$I_{OL} = 20mA$		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	$I_{OL} = 10mA$		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	$V_{OH} = -1mA$	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	$I_{OH} = -100\mu A$	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	THREE-STATE output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	$T_A = 25°C$		8		pF
C_{IN}	Input capacitance all other inputs	$T_A = 25°C$		5		pF

**These are absolute voltage with respect to pins 13 or 38 on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 70°C$ See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	ACCESS PARAMETER	FIGURE	'S409-3 MIN	TYP	MAX	UNIT
t_{RHA}	Row address held from column select	Figure 4	10			ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay Mode 6)	Figure 11	40	54	80	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figures 7, 10		90	140	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figures 7, 10, 11		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	15	23	37	ns
t_{APDL}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	46	ns
t_{APDH}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	46	ns
t_{SPDL}	Address strobe to address output low	Figures 4, 5		40	70	ns
t_{SPDH}	Address strobe to address output high	Figures 4, 5		40	70	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ setup time to $\overline{RASIN}$ high (Mode 6)	Figure 11	35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (R/C low in Mode 4)	Figure 5	32	41	67	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 5	25	39	60	ns
t_{RCC}	Column select to column address valid	Figure 4		40	67	ns
t_{RCR}	Row select to row address valid	Figures 4, 5		40	67	ns
t_{RAH}	Row address hold time (Mode 5)	Figures 7, 10	30			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 7, 10, 11	20			ns
t_{ASC}	Column address setup time (Mode 5)	Figures 7, 10	8			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 7, 10, 11	6			ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	'S409-3 MIN	TYP	MAX	UNIT
t_{FRQL}	RFCK low to forced $\overline{RFRQ}$ low	$C_L = 50$ pF, Figure 6		20	30	ns
t_{FRQH}	RGCK low to force $\overline{RFRQ}$ high	$C_L = 50$pF, Figure 6		50	75	ns
t_{RGRL}	RGCK low to $\overline{RAS}$ low	Figure 6	50	65	95	ns
t_{RGRH}	RGCK low to $\overline{RAS}$ high	Figure 6	40	60	85	ns
t_{RFRH}	$\overline{RFSH}$ high to $\overline{RAS}$ high (encoding forced RFSH)	See Mode 1 description	55	80	125	ns
t_{CSCT}	$\overline{CS}$ high to $\overline{RFSH}$ counter valid	Figure 6		55	75	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 3			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	$\overline{CS}$ = X, Figures 3, 6, 8		47	70	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figures 3, 6		45	70	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figures 3, 8		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	$C_L = 50$pF, Figure 3			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	$C_L = 50$pF, Figure 3			80	ns
t_{RGEOB}	RGCK low to end-of-burst low	$C_L = 50$pF, Figure 8			95	ns
t_{MCEOB}	Mode change to end-of-burst high	$C_L = 50$pF, Figure 8			75	ns

Switching Characteristics: (Cont'd)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S409-3 MIN	TYP	MAX	UNIT
	THREE-STATE PARAMETER					
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 6, 13 R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 6, 13 R2 = 1k, S1 Open		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 6, 13 R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 6, 14 R1 = 1k, S2 Open		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0\text{-}3}$) high from Hi-Z high	Figures 6, 13 R2 = 750Ω, S1 open		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0\text{-}3}$) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0\text{-}3}$) low from Hi-Z high	Figure 13 S1, S2 Open		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0\text{-}3}$) Hi-Z high from low	C_L = 15pF, Figure 13, R2 = 750Ω, S1 open		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. C_L = 500pF; RAS0-RAS3, C_L = 150pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF/IO should not exceed 50 pF.

Applications

The 74S409 Dynamic RAM Controller provides all the address and control signals necessary to access and refresh dynamic RAMs. Since the 74S409 is not compatible with a specific bus or microprocessor, an interface is often necessary between the 74S409 and the system. A general application using PAL to implement the interface and two additional chips to provide refresh clock and chip select is shown in figure 15.

The 74S409 operating mode may vary from application to application. For efficient refresh it is recommended to use mode 1 and mode 5 to take advantage of the hidden (transparent) refresh with forced refresh back-up.

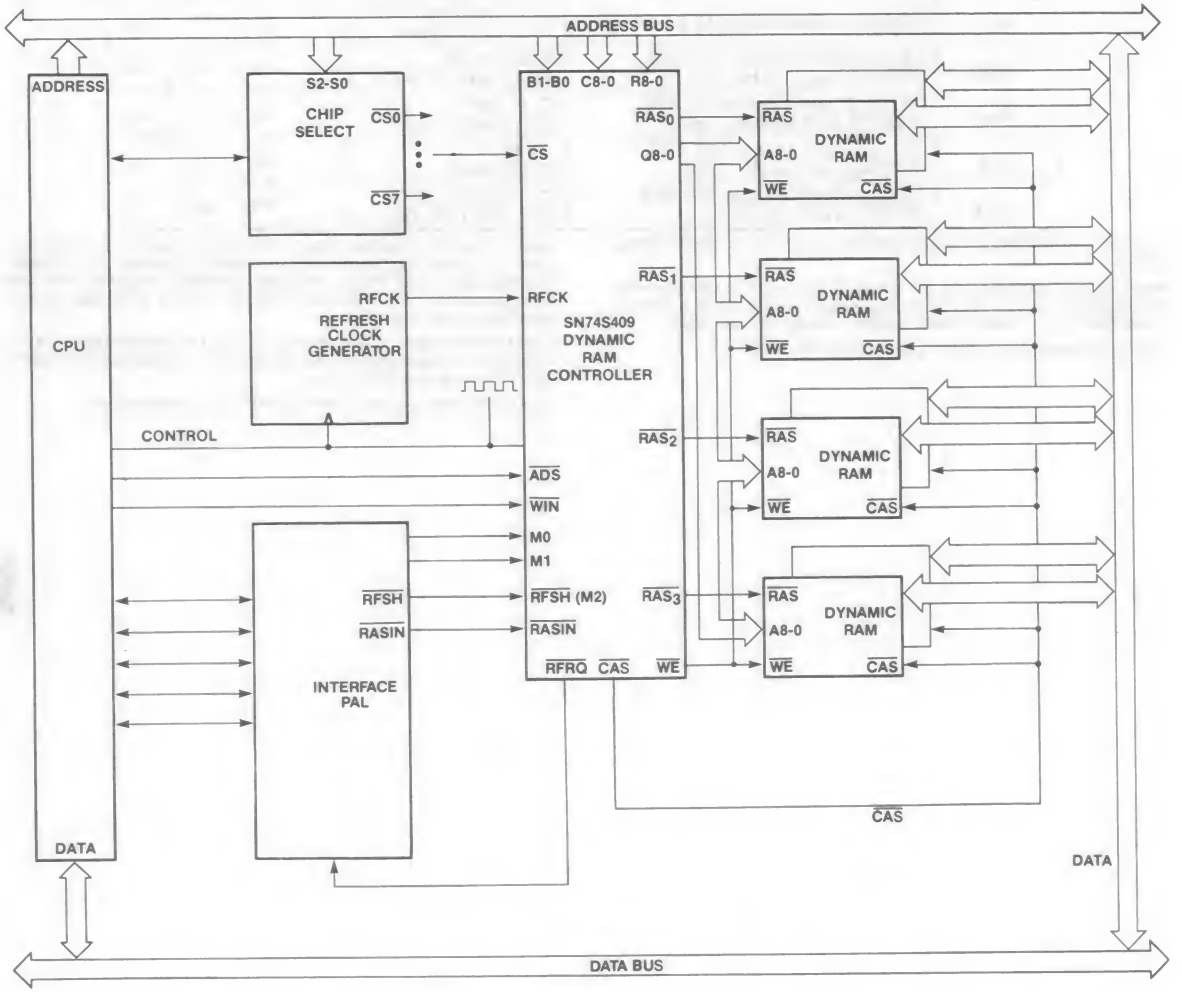


Figure 15. 74S409 in general application.

Octal Dynamic-RAM Driver with 3-state Outputs

SN54/74S700/-1 SN54/74S730/-1 SN54/74S731/-1 SN54/74S734/-1

Features/Benefits:

- Provides MOS voltage levels for 16 K and 64 K D-RAMs
- Undershoot of low-going output is less than -0.5 V
- Large capacitive drive capability
- Symmetric rise and fall times due to balanced output impedance
- Glitch-free outputs at power-up and power-down
- 20-pin SKINNYDIP® saves space
- 'S730/734 are exact replacement for the Am2965/66
- 'S700/730/731/734 are pin-compatible with 'S210/240/241/244, and can replace them in many applications
- 'S700-1/730-1/731-1/734-1 have a larger resistor in the output stage for better undershoot protection
- Commercial devices are specified at $V_{CC} \pm 10\%$.

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S700/-1	J,F,L	Mil	High-Low	Invert	S
SN74S700/-1	N,J	Com			
SN54S730/-1	J,F,L	Mil	Low		
SN74S730/-1	N,J	Com			
SN54S731/-1	J,F,L	Mil	High-Low	Non-Invert	
SN74S731/-1	N,J	Com			
SN54S734/-1	J,F,L	Mil	Low		
SN74S734/-1	N,J	Com			

Description:

The 'S700, 'S730, 'S731, and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S700 and 'S730 are inverting drivers and the 'S731 and 'S734 are non-inverting drivers. The 'S700/731 are pin-compatible with the 'S210/241 and have complementary enables. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular octal buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S700, 'S730, 'S731, and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC} - 1.15 volts, limit undershoot to 0.5V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

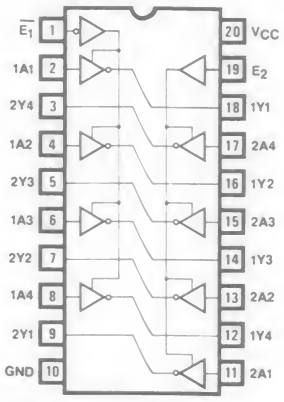
For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S700-1, 'S730-1, 'S731-1, 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S700-1 series.

A typical fully-loaded-board dynamic-RAM array consists of 4 banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50pf and 500pf load capacitances, and the commercial-range specifications are extended to $V_{CC} \pm 10\%$.

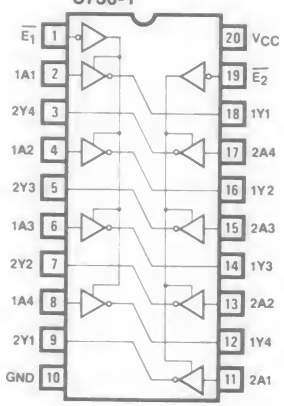
All of the octal devices are packaged in the popular 20-pin SKINNYDIP™

Logic Symbols

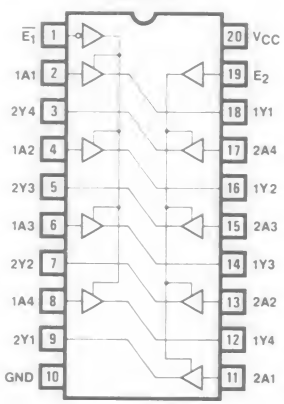
'S700/-1



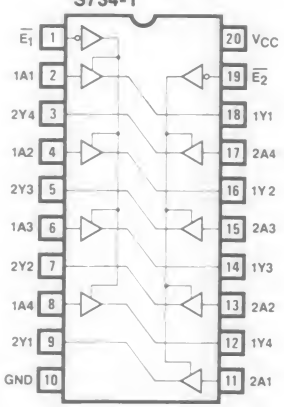
S730 (AM2965)
S730-1



'S731/-1



S734 (AM2966)
S734-1



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Monolithic Memories MMI

Function Tables

S700/-1

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

S730/-1

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

S731/-1

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

S734/-1

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −.5V to 7V
Input Voltage ..... −1.5V to 7.0V
Off-state Output Voltage ..... −.5V to + V_{CC} max
Storage Temperature ..... −65° to + 150°C
Output Current ..... 200 mA

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}*	Low-level input voltage						0.8			0.8	V
V_{IH}*	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	Any A	V_{CC} MAX	V_I = 0.4V			−0.2			−0.2	mA
		Any E					−0.4			−0.4	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 1mA			0.5			0.5	V
				I_{OL} = 12mA			0.8			0.8	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −1mA	V_{CC} −1.15	V_{CC} −.7		V_{CC} −1.15	V_{CC} −.7		V
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			−200			−200	μA
I_{OZH}				V_O = 2.7V			100			100	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		−60		−200	−60		−200	mA
I_{OL}	Output sink current		V_{OL} = 2.0V	'S 7XX	50			50			mA
				'S 7XX-1	40			40			
I_{OH}	Output source current		V_{OH} = 2.0V		−35			−35			mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	S700/-1 S730/-1		24	50		24	50	mA
				S731/-1 S734/-1		53	75		53	75	
		Outputs Low		S700/-1 S730/-1		86	125		86	125	
				S731/-1 S734/-1		92	130		92	130	
		Outputs Disabled		S700/-1 S730/-1		86	125		86	125	
				S731/-1 S734/-1		116	150		116	150	

†Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

*These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or test noise. Do not attempt to test these values without suitable equipment.

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Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S700, 'S730, 'S731, 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	30	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	16	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf	*	±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	−0.5	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S700, 'S730, 'S731, 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10%			COMMERCIAL V_{CC} = 5.0V ±10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		40	18		35	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			−0.5			−0.5	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

††T_C = -55 to + 125°C for flatpack versions.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S700-1, 'S730-1, 'S731-1, 'S734-1

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	40	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf	*	±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	−0.3	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S700-1, 'S730-1, 'S731-1, 'S734-1

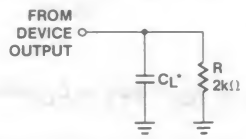
SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10%			COMMERCIAL V_{CC} = 5.0V ±10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		50	18		45	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			-0.3			-0.3	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

†† T_C = -55 to + 125°C for flatpack versions.

Switching Test Circuits



*t_{pd} specified at C_L = 50 and 500pF

Figure 1. Capacitive Load Switching

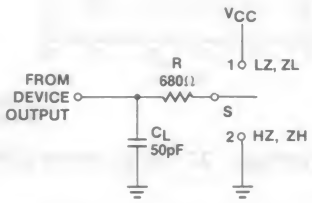


Figure 2. Three-State Enable/Disable

Typical Switching Characteristics

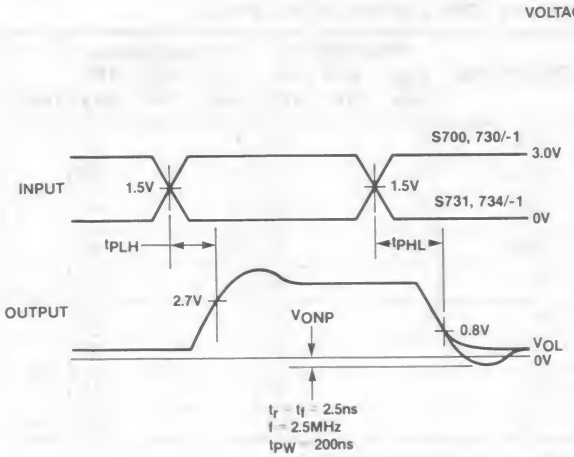


Figure 3. Output Voltage Levels

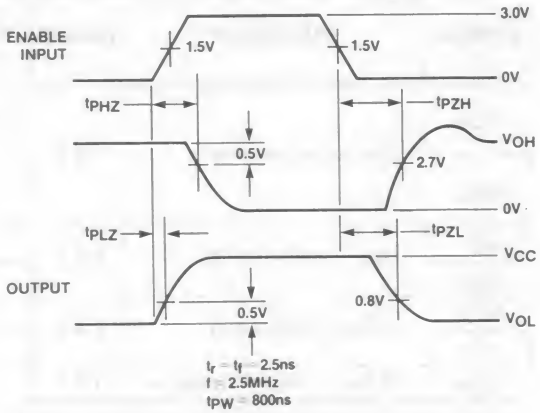
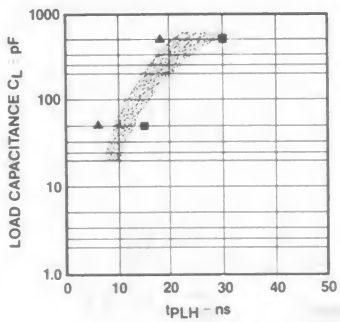


Figure 4. Three-State Control Levels

Typical Performance Characteristics:



▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5a. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S700 series

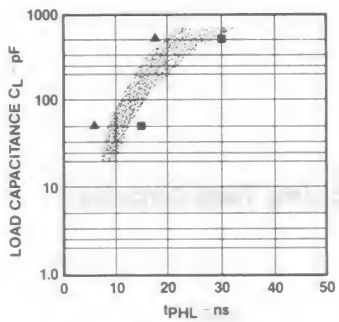
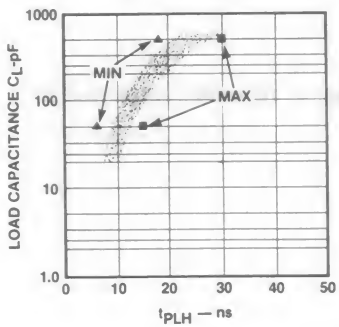


Figure 6a. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S700 series



▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5b. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S700-1 series

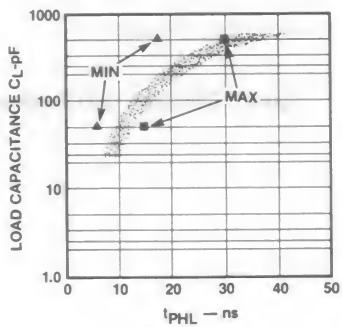


Figure 6b. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S700-1 series

Applications

The 'S700, 'S730, 'S731, and 'S734 are bipolar octal dynamic RAM drivers and are pin-compatible with the 'S210, 'S240, 'S241, and 'S244.

The actual circuit conditions that arise for driving dynamic RAM memories are as follows: Typically, in dynamic RAM arrays address lines and control lines, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ have a fair amount of "daisy chaining." The daisy chaining causes an inductive effect due to the traces in the printed circuit board; the dominant factor in the RAM loading is input capacitance, and these two conditions contribute to the actual driver conditions shown in Figure 7. The result is a transmission line with distributed inductance and capacitance connected to the driver outputs.

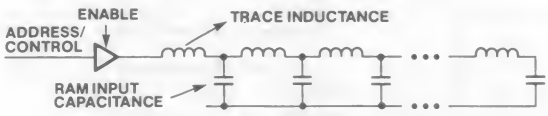


Figure 7. RAM Driver Output To Array

The transmission line effect can imply reflections, which in turn cause ringing, and it takes some time before the output settles from the low-to-high transition. On the high-to-low transition, along with ringing, a voltage undershoot can occur, and the circuit takes even longer to settle to an acceptable zero level. The main cause for the shorter high-to-low transition as compared to the low-to-high transition is the output impedance of typical Schottky drivers. Figure 8, shows a typical Schottky driver output stage and Figure 9 shows the output impedance for high and low output states.

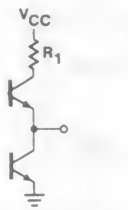


Figure 8. Typical Schottky Driver Output

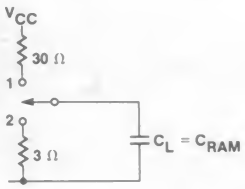


Figure 9. Driver Output Impedance

In Figure 9 when S=1, the output is high and the driver output impedance is approximately 30Ω. When S=2, the output is low and the driver output impedance is approximately 3Ω. There is a 10:1 ratio for the output impedances for the low and high states. The high-to-low transition causes a problem as the output transistor turns on fast due to the low impedance and undershoot results at the RAM inputs.

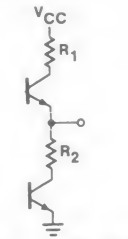


Figure 10. 'S700, 'S730, 'S731, and 'S734 Output Stage

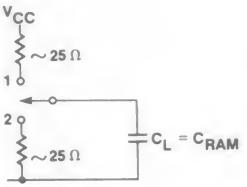


Figure 11. Driver Output Impedance For the 'S700, 'S730, 'S731, and 'S734

The 'S700, 'S730, 'S731, and 'S734 have a modification in their output stage, in that an internal resistor is added to the lower output stage as shown in Figure 10.

The 'S700-1, 'S730-1, 'S731-1 and the 'S734-1 have a larger resistor, R2, compared to the non-dash parts, which give better undershoot protection at a slightly slower switching performance.

The structure in Figure 10 provides a driver output impedance of approximately 25Ω in either high (S=1) or low (S=2) states as shown in Figure 11. In addition, this circuit limits undershoot to -0.5V, essentially eliminating that problem; provides a symmetrical rise and fall time; and guarantees output levels of V_{CC}-1.15 volts needed for MOS High levels. Also, when using the 'S700, 'S730, 'S731, and 'S734, no external resistors are needed. 'S240-series parts used with external resistors do provide drive capability, but the rise times and fall times are unsymmetrical due to higher impedance for low-to-high transitions.

Figure 12 shows the undershoot problem using a 'S240 without external resistors and the elimination of the problem by using the 'S730. Thus from a dynamic-RAM system-design viewpoint, the 'S700, 'S730, 'S731, and 'S734 are very effective RAM drivers.

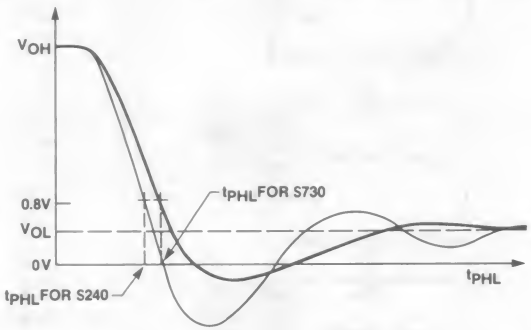


Figure 12. Comparison of Undershoots and t_{PHL}

An application using the octal drivers to interface address and control lines (and data lines) to a dynamic RAM array using 64K DRAMs is discussed. The signals needed for the controls are $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The address lines are A0–A7 and the data lines are shown as the high and low byte. The array is shown in Figure 13. It consists of four rows of DRAMs; each row has individual $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ lines. However, all four rows have common address lines A0–A7. The RAM capacitive loading for $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ is about 10 pf per input. The loading of the address lines is about 5 to 7 pf per input. The loading of the $\overline{RAS}_i$, $\overline{CAS}_i$ and $\overline{WE}_i$ inputs to each row of memories is 160 pf. Note that $\overline{RAS}_i$ and $\overline{CAS}_i$ come from the same driver, which reduces timings skews which might arise if they were output from separate drivers. The address lines are outputs from another driver, and the loading on each line is 320 pf (5 pf loading times 64 DRAMs). At this point it is worth noting that if a 320-pf loading affects performance unduly, then the address lines can be split between two drivers with each having a load of 160 pf, reducing overall signal delay.

If an error-detection-and-correction scheme is used, then typically a row size expands to 22 bits from the 16 bits shown in the example. The 'S700, 'S730, 'S731, and 'S734 drivers lend themselves to such expansion, as their propagation delays are specified at 50 and also at 500 pf.

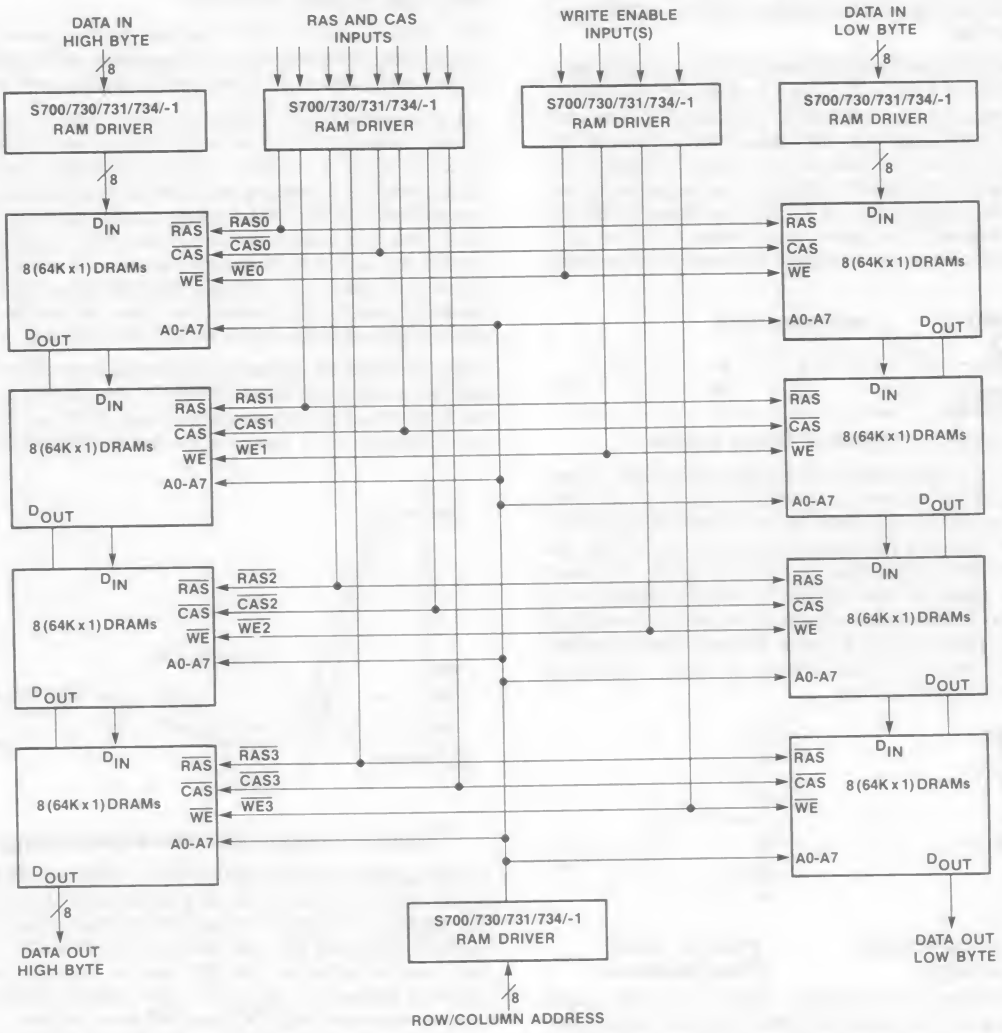
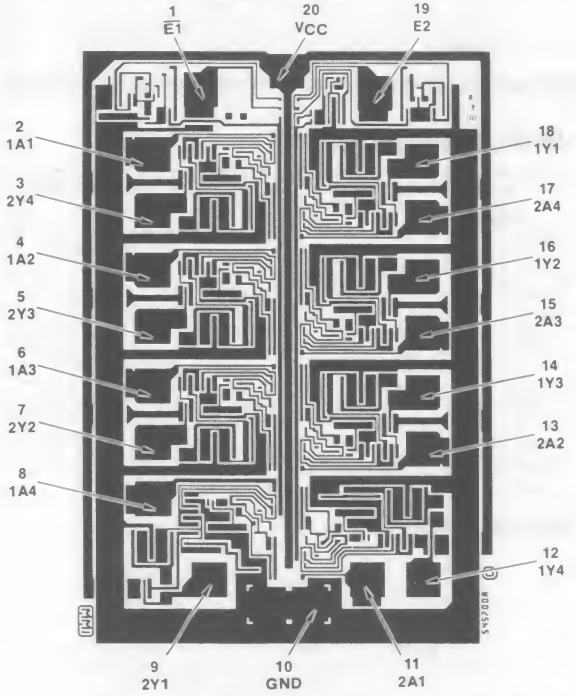


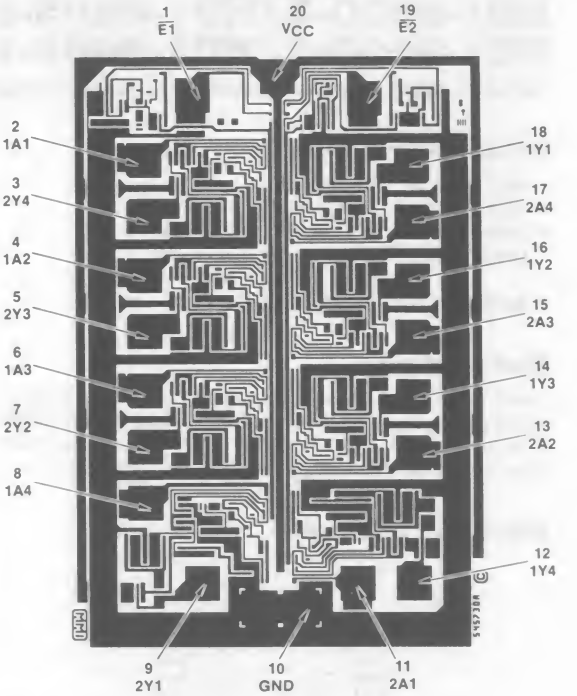
Figure 13. 256K X 16 Dynamic RAM Array with RAM Drivers

Die Configurations

SN54/74S700/-1

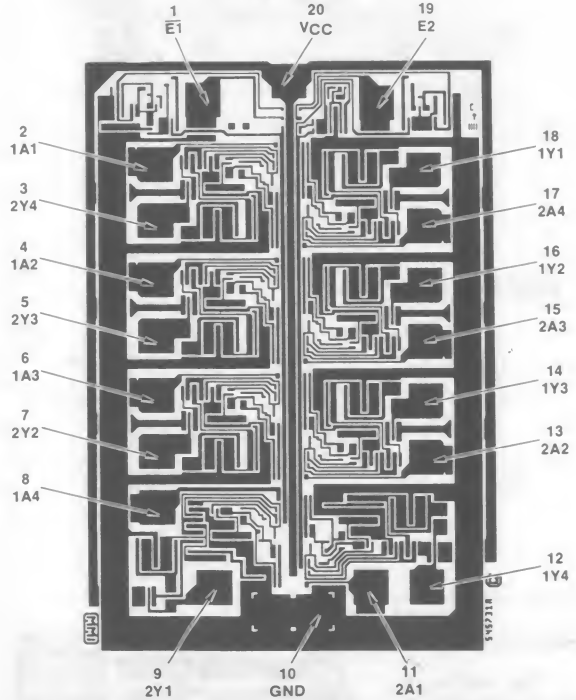


SN54/74S730/-1

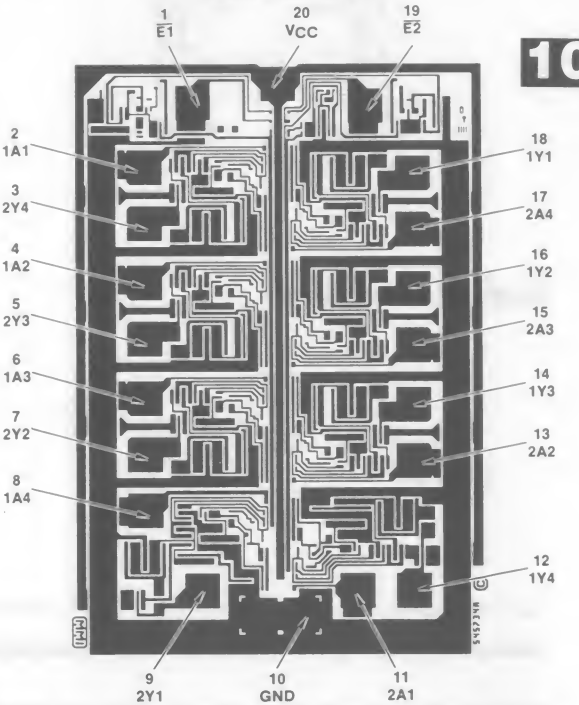


DIE SIZE: 62 x 87 mils

SN54/74S731/-1



SN54/74S734/-1



10

Quad Power/Logic Strobe

HD1-6600-8/HD1-6605-8
HD1-6600-5/HD1-6605-5
HD1-6600-2/HD1-6605-2

Features/Benefits

- High drive current—200 mA
- High speed—40 ns typical
- Low fan-in (250μA Max), TTL COMPATIBLE
- Low power: Standby 30 mW/circuit
  Active 120 mW/circuit
- Several different power-supply levels

Description

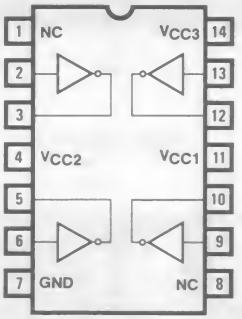
The HD1-6600 quad power strobe and the HD1-6605 quad logic strobe are four high-current drivers used for power-down mode of ROM/PROM and other logic devices. V_{CC} can be removed from nonactive devices and reduce total system power.

Ordering Information

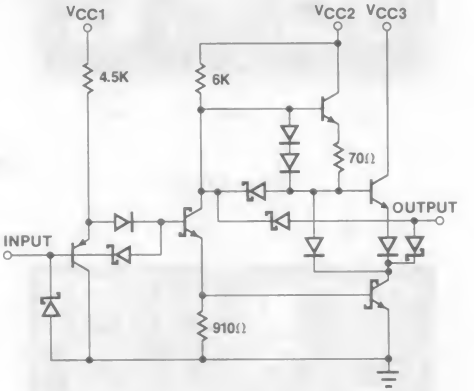
PART NUMBER	PACKAGE	TYPE	TEMPERATURE RANGE
HD1-6600-5	J14	Power	0°C to + 75°C
HD1-6605-5	J14	Logic	0°C to + 75°C
HD1-6600-2	J14	Power	-55°C to + 125°C
HD1-6605-2	J14	Logic	-55°C to + 125°C
HD1-6600-8*	J14	Power	-55°C to + 125°C
HD1-6605-8*	J14	Logic	-55°C to + 125°C

* LCC — contact the factory

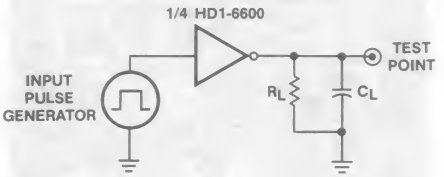
Pin Configuration



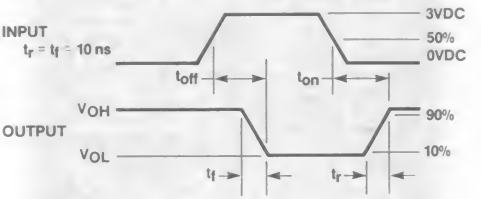
Block Diagram



Standard Test Load



Test Waveforms



*Note: Parts suffixed -8 are equivalent to parts suffixed -2 screened in accordance with MIL-STD 883 method 5004, Class B.

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Absolute Maximum Ratings

Supply voltage, V_{CC1} ..... +8V
V_{CC2} ..... + 18V (HD1-6600), + 14V (HD1-6605)
V_{CC3} ..... + 18V (HD1-6600), + 8V (HD1-6605)
Input voltage ..... −1.5V to +5.5V
Input current ..... −25 mA to +5 mA
Output current ..... −300 mA
Storage temperature range ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC1}	Supply voltage 1	4.5	5	5.5	4.5	5	5.5	V
V_{CC2}	Supply voltage 2	10	12	13.8	10	12	13.8	V
V_{CC3}	Supply voltage 3	4.5	5	5.5	4.75	5	5.5	V
I_{OH}	High-level output current		−150	−200		−150	−200	mA
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

Over Recommended Operating Free Air Temperature Range V_{CC2} = 12.0V V_{CC3} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IR} I_{IF}	Input current	V_{IN} = 2.4V V_{IN} = 0.4V	V_{CC1} = 5.5V		 −80	30 −250	μA
V_{IH} V_{IL}	Input threshold voltage	V_{CC1} = 4.5V		2.0		 0.8	V
V_{OH}	Output voltage (One strobe enabled)	V_{CC1} = 5.0V V_{IN} = 0.4V	I_L = −150mA	4.74	4.85		V
V_{OL}		V_{CC1} = 5.0V V_{IN} = 2.4V	I_L = 500μA		0.9	1.0	V
I_{CC1}	Supply current (All strobes enabled)	V_{CC1} = 5.5V	V_{IN} = 2.4V		4	6.0	mA
I_{CC1}		V_{CC1} = 5.5V	V_{IN} = 0.4V		4	6.4	mA
I_{CC2}		V_{CC1} = 5.5V V_{IN} = 0.4V	I_L = −150mA		50	60	mA
I_{CC2}		V_{CC1} = 5.5V V_{IN} = 2.4V	I_L = 0		10	12	mA

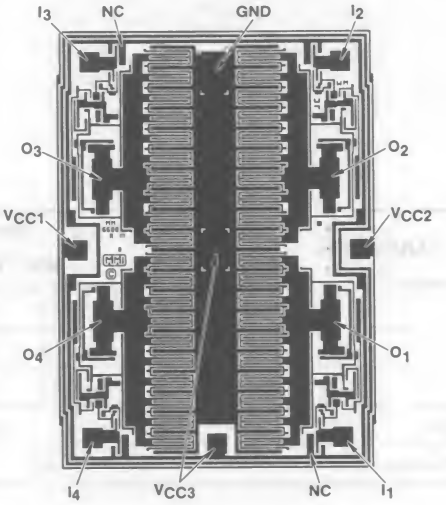
Switching Characteristics

V_{CC1} = 5.0V V_{CC2} = 12.0V V_{CC3} = 5.0V T_A = 25°C

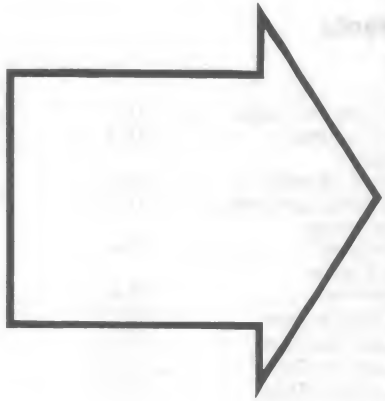
SYMBOL	PARAMETER	TEST CONDITIONS (SEE STANDARD TEST LOAD)	MIN	TYP	MAX	UNIT
t_{on}	Turn On delay	R_L = 31.6Ω C_L = 620pF		40	75	ns
t_{off}	Turn Off delay			40	75	ns
t_r	Rise time			35	65	ns
t_f	Fall time			35	65	ns

10

Die Configuration



Die Size: 90 x 67 mil



The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

Arithmetic and Logic Elements

DESCRIPTION	PART NUMBER	MAX ADD TIME	MAX CARRY (OR GENERATE) TIME	PINS
4-bit ALU	5/74S381	27 ns	20 ns	20
4 Group carry-look-ahead generator	5/74S182		7 ns	16

Encoder Priority

DESCRIPTION	PART NUMBER	OUTPUT	MAX LOGIC DELAYS	PINS
High-Speed Schottky Priority Encoders	SN54/74S148 SN54/74S348	Totem-Pole 3-State	$D_i \rightarrow A_i$ = 13nsec D_i — GS, EO = 15nsec	16

Look-Up Tables

DESCRIPTION	PART NUMBER	MAX ACCESS TIME	PINS
Sine (0°-90°) Look-Up Table	6086/7	100 ns	24
	5086/7	150 ns	24

Contents

Arithmetic Logic Unit/ Function Generator

SN54S381 SN74S381

Features/Benefits

- A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:

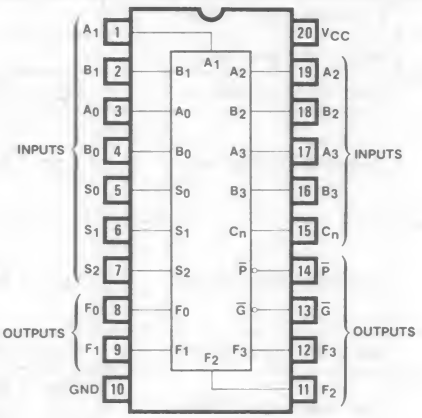
  A Minus B
  B Minus A
  A Plus B
  and Five Other Functions

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S381	J20,F20,20W,20L	Military
SN74S381	N20, J20	Commercial

Pin Configuration

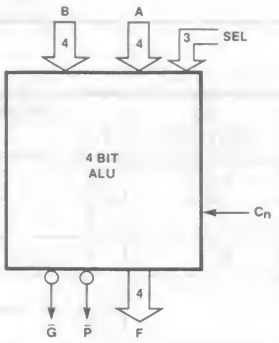
SN54S381, SN74S381



Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A fully carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package.

Logic Symbol



Function Table

SELECTION			ARITHMETIC/LOGIC OPERATION
S2	S1	S0	
L	L	L	Clear †
L	L	H	B minus A
L	H	L	A minus B
L	H	H	A plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset ††

† Force all F outputs to be Lows.
†† Force all F outputs to be Highs.

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over operating conditions

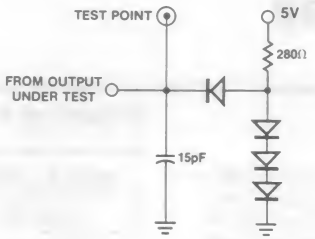
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA				−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	Any S input			−2	mA
			Cn			−8	
			All others			−6	
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.7V	Any S input			50	μA
			Cn			250	
			All others			200	
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = 20mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = −1mA	SN54S381	2.4	3.4		V
			SN74S381	2.7	3.4		
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			105	160	mA

* Not more than one output should be shorted at a time.

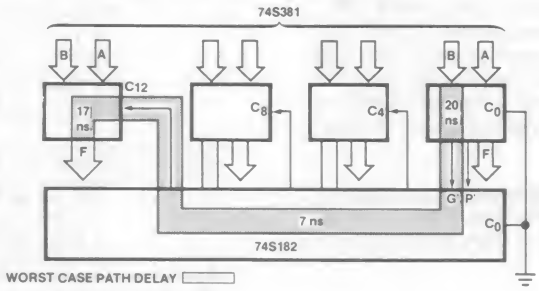
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	5/74S381 TYP	5/74S381 MAX	UNIT
t_P	Propagation delay time	C_n	Any F	10	17	ns
t_P	Propagation delay time	Any A or B	$\overline{G}$	12	20	ns
t_P	Propagation delay time	Any A or B	$\overline{P}$	11	18	ns
t_{PLH}	Propagation delay, low-to-high	Ai or Bi	Fi	18	27	ns
t_{PHL}	Propagation delay, high-to-low			16	25	ns
t_P	Propagation delay time	Any S	Fi, $\overline{G}$, $\overline{P}$	18	30	ns

Standard Test Load



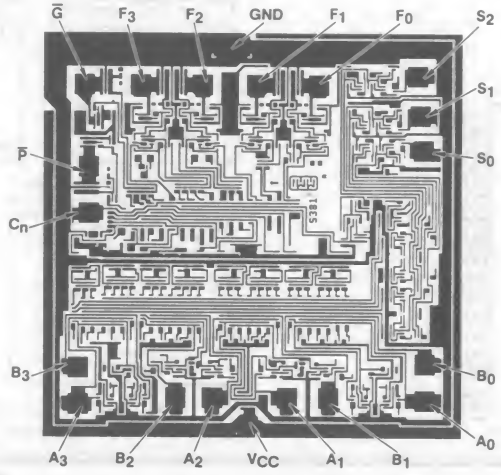
16-BIT ALU (USING 74S381)



MAXIMUM DELAY OF ADDITION/SUBTRACTION.

	74S381
1-4 bits	27ns
5-16 bits	44ns
17-64 bits	64ns

Die Configuration



Die Size: 83 x 86 mil

Look-Ahead Carry Generators

SN54S182 SN74S182

Description

The SN54S182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table below.

When used in conjunction with 74S381, 67S581, 74S181, 2901, 6701 arithmetic logic units (ALU), these generators provide high-speed carry lookahead capability for any word length. Each 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Logic equations for the 'S182 are:

$$C_{n+x} = G0 + P0\ Cn$$

$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ Cn$$

$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$

$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$

$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\ (X0 + Cn)}$$

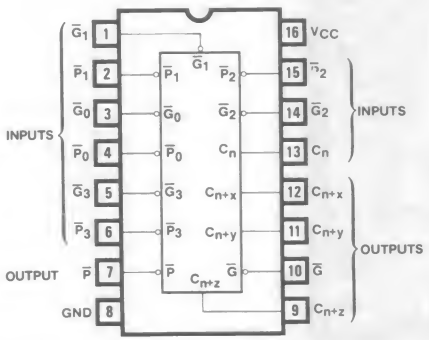
$$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + Cn)]}$$

$$\overline{C}_{n+z} = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + Cn)]\}}$$

$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$

$$X = X3 + X2 + X1 + X0$$

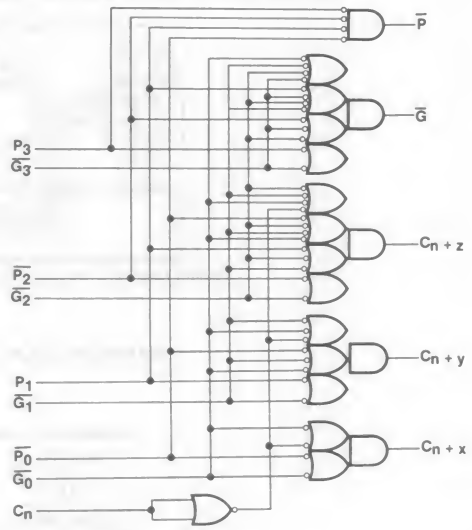
Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S182	J16,F16,16W,20L	Military
SN74S182	N16, J16	Commercial

Block Diagram/Schematic



Summarizing Tables

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS	OUTPUT
$\overline{G}1\ \overline{G}0\ \overline{P}1\ \overline{P}0\ Cn$	C_{n+y}
L X X X X	H
X L L X X	H
X X L L H	H
All other combinations	L

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS	OUTPUT
$\overline{P}3\ \overline{P}2\ \overline{P}1\ \overline{P}0$	$\overline{P}$
L L L L	L
All other combinations	H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS	OUTPUT
$\overline{G}0\ \overline{P}0\ Cn$	C_{n+x}
L X X	H
X L H	H
All other combinations	L

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS	OUTPUT
$\overline{G}3\ \overline{G}2\ \overline{G}1\ \overline{G}0\ \overline{P}3\ \overline{P}2\ \overline{P}1$	$\overline{G}$
L X X X X X X	L
X L X X L X X	L
X X L X L L X	L
X X X L L L L	L
All other combinations	H

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS	OUTPUT
$\overline{G}2\ \overline{G}1\ \overline{G}0\ \overline{P}2\ \overline{P}1\ \overline{P}0\ \overline{C}n$	C_{n+z}
L X X X X X X	H
X L X L X X X	H
X X L L L X X	H
X X X L L L H	H
All other combinations	L

H = High Level, L = Low Level, X = Irrelevant. Any inputs not shown in a given table are irrelevant with respect to that output.

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Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over operating conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA					−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	C_n input				−2	mA
			$\overline{P}_3$ input				−4	
			$\overline{P}_2$ input				−6	
			$\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ input				−8	
			$\overline{G}_0$ or $\overline{G}_2$				−14	
			$\overline{G}_1$ input				−16	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	C_n input				50	μA
			$\overline{P}_3$ input				100	
			$\overline{P}_2$ input				150	
			$\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ input				200	
			$\overline{G}_0$ or $\overline{G}_2$				350	
			$\overline{G}_1$ input				400	
I_I	Maximum input current	V_{CC} = MAX, V_I = 5.5V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA					0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1mA	SN74S182		2.7	3.4		V
			SN54S182		2.5	3.4		
I_{OS}	Output short-circuit current *	V_{CC} = MAX			−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 1	SN74S182			69	109	mA
			SN54S182			69	99	
I_{CCH}	Supply current, all outputs high	V_{CC} = 5V, See Note 2				35		mA

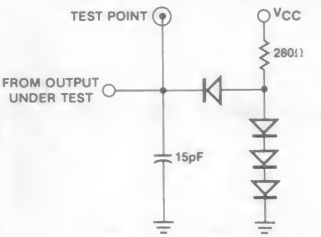
*Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTES: 1. ICCL is measured with all outputs open; inputs $\overline{G}0$, $\overline{G}1$, and $\overline{G}2$ at 4.5 V; and all other inputs grounded.
2. ICCH is measured with all outputs open, inputs $\overline{P}3$ and $\overline{G}3$ at 4.5 V, and all other inputs grounded.

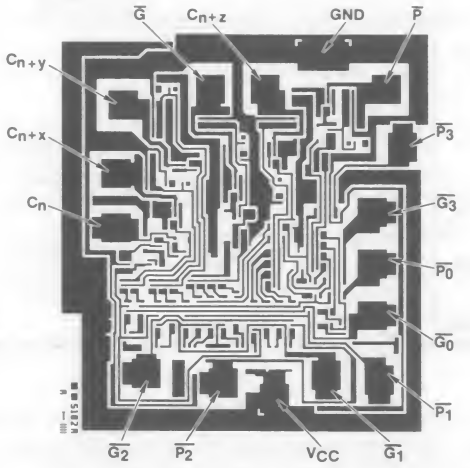
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$, $\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	C_{n+x}, C_{n+y}, or C_{n+z}	4.5	7	ns
t_{PHL}	Propagation delay, high-to-low			4.5	7	ns
t_{PLH}	Propagation delay, low-to-high	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	$\overline{G}$	5	7.5	ns
t_{PHL}	Propagation delay, high-to-low			7	10.5	ns
t_{PLH}	Propagation delay, low-to-high	$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	$\overline{P}$	4.5	6.5	ns
t_{PHL}	Propagation delay, high-to-low			6.5	10	ns
t_{PLH}	Propagation delay, low-to-high	C_n	C_{n+x}, C_{n+y}, or C_{n+z}	6.5	10	ns
t_{PHL}	Propagation delay, high-to-low			7	10.5	ns

Standard Test Load



Die Configuration



Die Size: 53 x 57 mil

High-Speed Schottky Priority Encoders

SN54/74S148 (93S18)
SN54/74S348

Features/Benefits

- Second-generation-Schottky designs feature VERY High Speed compared to other TTL priority encoders
- Totem-pole outputs on SN54/74S148
- Three-state outputs on SN54/74S348
- SN54/74S148 is speed upgrade for SN54/74148, SN54/74LS148, 9318, 93L18
- SN54/74S348 is speed upgrade for SN54/74LS348
- Encode 8 data lines to 3-bit binary (octal) code
- Cascadable in several different ways
- Glitch on $\overline{GS}$ line in other TTL priority encoders has been designed out
- Applications include:
  - Interrupt/status scanning
  - Resource allocation in processors/peripherals
  - Normalization in floating-point arithmetic units
  - Bus arbitration
- Maximum Logic Delays:
  - $\overline{D_i}$ → $\overline{A_i}$ 13ns
  - $\overline{D_i}$ → $\overline{GS}$ 15ns
  - $\overline{D_i}$ → $\overline{EO}$ 15ns

  } 'S148 and 'S348

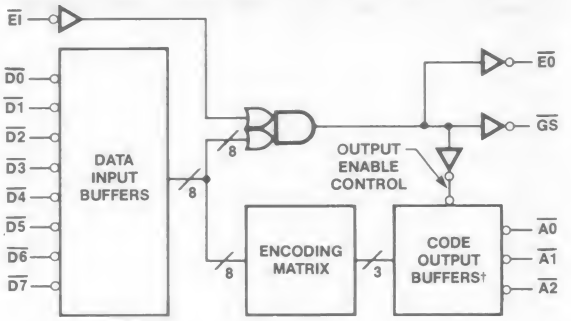
  - t_{ZX}(E_i to A_i) 18ns
  - t_{XZ}(E_i to A_i) 15ns

  } 'S348 Only

Ordering Information

PART NUMBER	PKG	TEMP	OUTPUTS	POWER
SN54S148	J,F,20,L	Mil	Totem-pole	S
SN74S148	N,J	Com		
SN54S348	J,F,20,L	Mil	Three-state	
SN74S348	N,J	Com		

Block Diagram



† Disabled outputs are High for 54/74S148 and Hi-Z for 54/74S348.

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Description

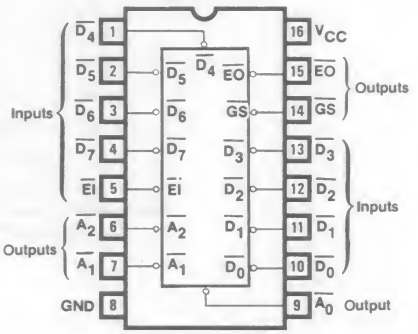
The SN54/74S148 and SN54/74S348 high-speed Schottky TTL priority encoders scan 8 data-input lines, and output a 3-bit binary (that is, "octal") code which is the line number of the highest-priority data input being asserted. To allow expansion by cascading, in some cases without external logic, both devices provide three control signals: $\overline{EI}$ (Enable Input), $\overline{EO}$ (Enable Output), and $\overline{GS}$ (Group Select).

When $\overline{EI}$ is not being asserted, the code outputs are forced High in the 'S148 and into Hi-Z state in the 'S348. When $\overline{EI}$ is being asserted, these outputs are forced to the line-number code; see "Function Table." Also, when $\overline{EI}$ is being asserted, $\overline{EO}$ and $\overline{GS}$ are complementary; $\overline{EO}$ indicates that no data-input line is being asserted, whereas $\overline{GS}$ indicates that at least one of them is being asserted.

$\overline{EI}$ and $\overline{EO}$ may be used to link encoders together in a "daisy-chained" configuration. Also, in a two-level cascaded configuration, the GS signals from the first-level encoders are the data inputs for the second-level encoder(s); see "Applications."

Pin Configuration

SN54/74S148
SN54/74S348
(Top View)

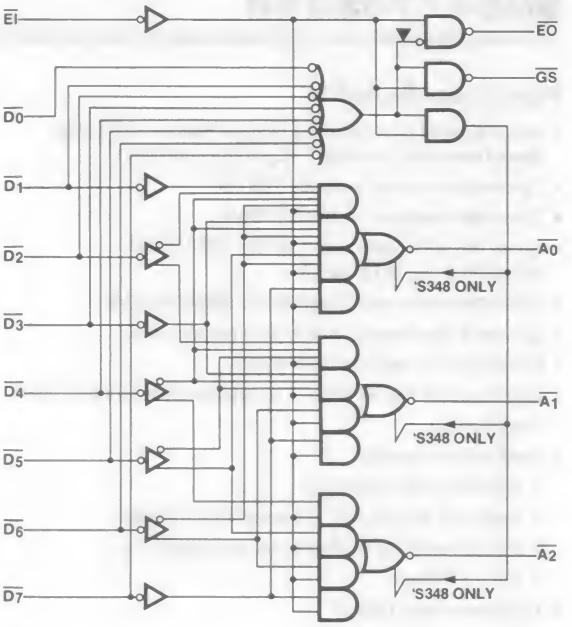


The line-number-code outputs ($\overline{A_2}$, $\overline{A_1}$, $\overline{A_0}$) are totem-pole in the 'S148 and are three-state in the 'S348. All inputs and outputs of both devices are TTL-compatible. Data inputs present **two** standard 54S/74S normalized loads; $\overline{EI}$, however, presents only a half of one such load.

The "Function Table" has been stated in terms of High (H) and Low (L) signal levels rather than in terms of "ones" and "zeroes." The most natural interpretation of the operation of these parts is that **all** signals, outputs as well as inputs, are **assertive-low** — that is, L is identified with "one" and H with "zero." Consequently, the highest-priority data input is named "D_7" and the output code it produces when asserted is LLL. In like manner, asserting the input D_4 produces the output code LHH if none of the higher-priority data-input lines D_7, D_6, or D_5 is being asserted; and so forth.

It is consistent with this interpretation that an 'S148 outputs a code of HHH either when it is disabled, or when it is enabled but none of its data inputs are being asserted. Under the same circumstances, the code outputs of an 'S348 go into Hi-Z state.

Logic Symbol



Function Table

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{D0}$	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{D4}$	$\overline{D5}$	$\overline{D6}$	$\overline{D7}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	$\overline{GS}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H/Z*	H/Z*	H/Z*	H	H
L	H	H	H	H	H	H	H	H	H/Z*	H/Z*	H/Z*	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

* NOTE: "H" for 'S148, "Z" for 'S348

Absolute Maximum Ratings

	Operating
Supply voltage V_{CC}	−0.5V to 7V
Input voltage	−1.5V to 7V
Off-state output voltage	−0.5V to 5.5V
Storage temperature range	−65°C to + 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High level output current			−1			−1	mA
I_{OL}	Low level output current			20			20	mA
T_A	Operating free air temperature	−55		+125	0		+75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	$\overline{EI}$ Input	V_{CC} = MAX	V_I = 0.5V			−0.8			−0.8	mA
		Any Input Except $\overline{EI}$					−3.2			−3.2	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Input current		V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V	I_{OL} = 20mA			.5			.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V	I_{OH} = −1.0mA	2.5	3.4		2.7	3.4		V
I_{OZL}	Off-state output current, Low-level voltage applied	('S348 Only)	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V			−50			−50	μA
I_{OZH}	Off-state output current, High-level voltage applied	('S348 Only)	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.7V			50			50	μA
I_{OS}	Short-circuit output current †		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current, See note 1	'S148	V_{CC} = MAX				115			110	mA
		'S348					125			120	

NOTE 1: I_{CC} is measured with inputs $\overline{D_7}$ and $\overline{EI}$ Low, other inputs High, and outputs open.

† Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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Switching Characteristics

V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	Low to High	$\overline{D_1}$ thru $\overline{D_7}$	$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	C_L = 15pf, R_L = 280Ω		9	13	ns
t_{PHL}		High to Low					9	13	ns
t_{PLH}		Low to High	$\overline{D_0}$ thru $\overline{D_7}$	$\overline{GS}$			11	15	ns
t_{PHL}		High to Low					11	15	ns
t_{PLH}		Low to High		$\overline{EO}$			12	15	ns
t_{PHL}		High to Low					12	15	ns
t_{PLH}		Low to High	$\overline{EI}$	$\overline{GS}$			6	9	ns
t_{PHL}		High to Low					6	9	ns
SN54/74S148 ONLY									
t_{PLH}	Propagation delay	Low to High	$\overline{EI}$	$\overline{EO}$	C_L = 15pf, R_L = 280Ω		8	12	ns
t_{PHL}		High to Low					8	12	ns
t_{PLH}		Low to High		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$			10	13	ns
t_{PHL}		High to Low					10	13	ns
SN54/74S348 ONLY									
t_{PLH}	Propagation delay	Low to High	$\overline{EI}$	$\overline{EO}$	C_L = 15pf, R_L = 280Ω		11	14	ns
t_{PHL}		High to Low					11	14	ns
t_{PZH}		Three-state to High		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	C_L = 50pf, R_L = 280Ω		12	18	ns
t_{PZL}		Three-state to Low					12	18	ns
t_{PHZ}		High to Three-state		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	C_L = 5pf, R_L = 280Ω		8	15	ns
t_{PLZ}		Low to Three-state					8	15	ns
t_{PZH}		Three-state to High	$\overline{D_0}$ thru $\overline{D_7}$*	$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$	N/A†		13		ns
t_{PZL}		Three-state to Low					13		ns
t_{PHZ}		High to Three-state		$\overline{A_0}$, $\overline{A_1}$, or $\overline{A_2}$			20		ns
t_{PLZ}		Low to Three-state					26		ns

* NOTE: Refer to second line of "Function Table".

† NOTE: These values are furnished for the purpose of estimating the logic delays of a combination such as shown in Fig. 1 and 2. They are design guidelines only and are not tested and therefore not guaranteed.

Applications

The basic logic function performed by these priority encoders is to scan a parallel word of any length for the most-significant Low signal in a field of Highs. Although a single part has only 8 data inputs and hence can only scan a one-byte field, the architecture of these parts supports several different cascading schemes.

The Enable Input ($\overline{EI}$), when **not** being asserted, forces the code outputs ($\overline{A_2}$, $\overline{A_1}$, $\overline{A_0}$) High in an 'S148 or into Hi-Z (high-impedance) state in an 'S348. Since all input signals and all output signals for these parts are conventionally considered as assertive-low, the effect is to disable the code outputs in the manner appropriate for a totem-pole part ('S148) or a three-state part ('S348). When $\overline{EI}$ is asserted, the code outputs are forced to the code of the highest-priority data inputs being asserted; if no data input is being asserted, the code outputs remain as if the part were not enabled.

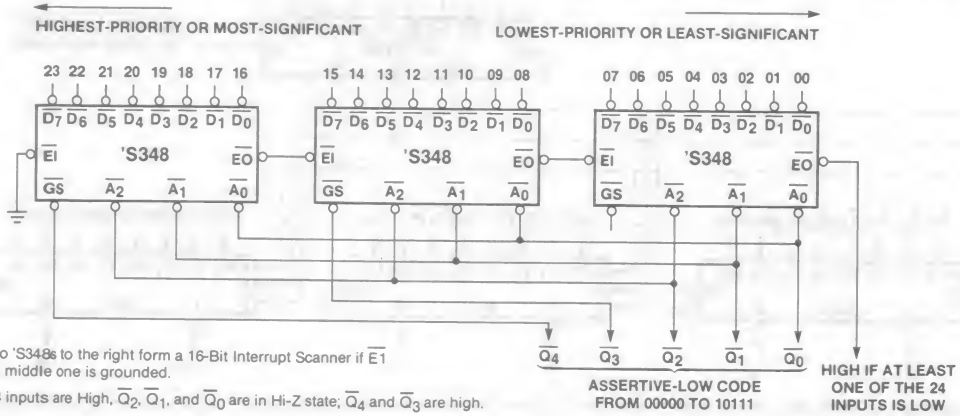
Also, when $\overline{EI}$ is being asserted, the $\overline{EO}$ and $\overline{GS}$ signals operate as complementary "presence" signals. When the encoder asserts $\overline{EO}$, this condition means that none of the data inputs for that encoder are being asserted, and that a lower-priority encoder should therefore be enabled to examine its data inputs. Thus, several encoders may be daisy-chained as in Figures 1 and 2, with $\overline{EO}$ from the highest-priority encoder controlling $\overline{EI}$ for the next-highest-priority encoder, and so forth. The highest-priority-encoder is always enabled. In such daisy-chain arrangements, code outputs may simply be bussed together if three-state encoders are being used, or combined using external assertive-low "OR" logic. Figure 1 illustrates a three-encoder daisy chain to scan 24 lines; a two-encoder daisy-chain may likewise be used to scan 16 lines. In each of these cases, no other components besides encoders are needed.

A slightly different approach is needed to scan more than 24 lines. Figure 2 shows a 64-line scanner which uses 9 'S348s and no other components. These encoders are on two "levels"; the $\overline{GS}$ outputs from the first-level encoders are the inputs for the second-level encoder, and indicate when asserted that the corresponding first-level encoders do indeed have inputs being asserted. The bussed first-level-encoder outputs form the least-significant octal digit of the 6-bit line-number code for the highest-priority data-input line being asserted; the outputs of the second-level encoder form the most-significant octal digit of this result. Figure 3 shows the highest-speed "totally-parallel" approach, which eliminates the potential delay due to daisy-chaining the enable signal through the first-level parts. The $\overline{EI}$ signals for all of the encoders are grounded, and an 8-way 3-bit multiplexer comprised of three 'S151s or three 'S251s is used to select the code outputs of the highest-priority first-level encoder which has any data-input lines being asserted. The address lines of these multiplexers are controlled by the code outputs of the second-level encoder.

Yet another cascading scheme, not shown, uses a single decoder such as an 'S138 instead of three multiplexers. The decoder's address-input lines are controlled by the second-level-encoder outputs as in Figure 3. Its outputs go to the $\overline{E1}$ inputs of the first-level encoders, so that **only** the highest-priority first-level encoder which has any data-input lines being asserted gets enabled. The first-level-encoder code outputs are bussed together as in Figure 2. This scheme is not quite as fast as that of Figure 3, but is faster than that of Figure 2 since the daisy-chaining delay is still eliminated.

The scheme of Figure 3 can be implemented with either totem-pole or three-state parts; the others require three-state parts. Additional schemes are possible. If more than 64 lines must be scanned, more than two levels of encoders can be used. Obviously, also, if only 48 or 56 lines must be scanned, a partially-populated version of one of the 64-bit schemes can do the job.

Although the original system purpose of priority encoders was to scan interrupt lines, they are also ideally suited for high-speed normalization scanning of the result of a floating-point adder/subtracter, in order to determine how many leading zeroes the result contains in order that the normalization shift may be performed in one operation by a "barrel shifter" or "matrix shifter." This result must be in "Negative Absolute Value" form because of the assertive-low behavior of the encoder. (See Monolithic Memories Application note AN-111, "Big, Fast, and Simple — Algorithms, Architecture, and Components for High-End-Superminis," by Ehud Gordon and Chuck Hastings, pages 7-8.) Another important application is "resource control" in computer systems having several semi-autonomous active units; for instance, a single encoder followed by a decoder can arbitrate requests on 8 bus-request lines and return a single bus-grant signal on one of 8 bus-grant lines.



NOTES: 1. The two 'S348s to the right form a 16-Bit Interrupt Scanner if $\overline{E1}$ for the middle one is grounded.

2. If all 24 inputs are High, $\overline{Q_2}$, $\overline{Q_1}$, and $\overline{Q_0}$ are in Hi-Z state; $\overline{Q_4}$ and $\overline{Q_3}$ are high.

Figure 1. 24-Bit Leading-Zeroes Detector or Interrupt Scanner Using 'S348s and No External Components

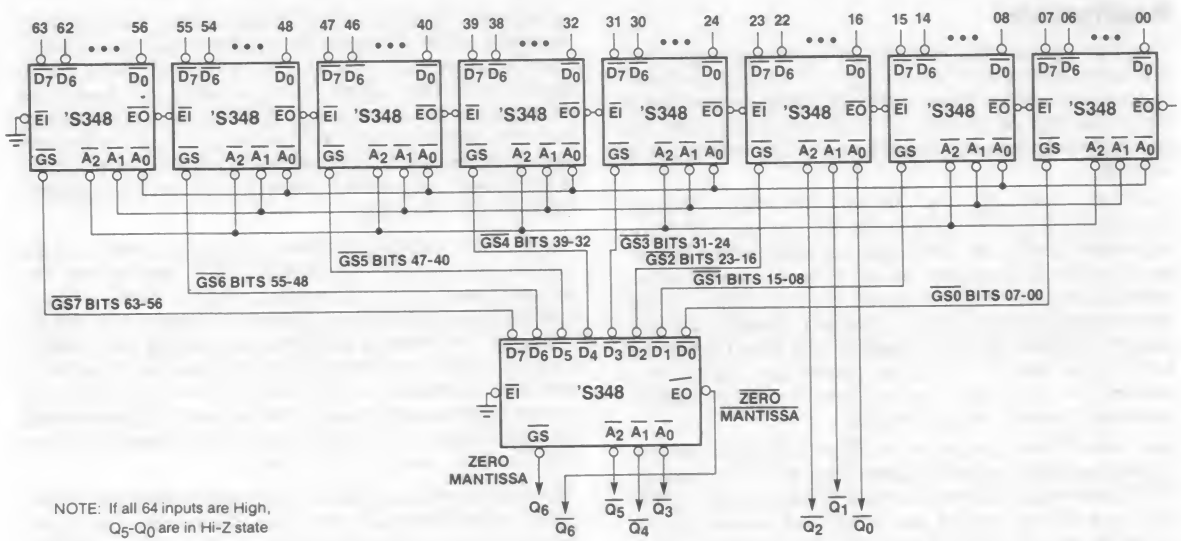
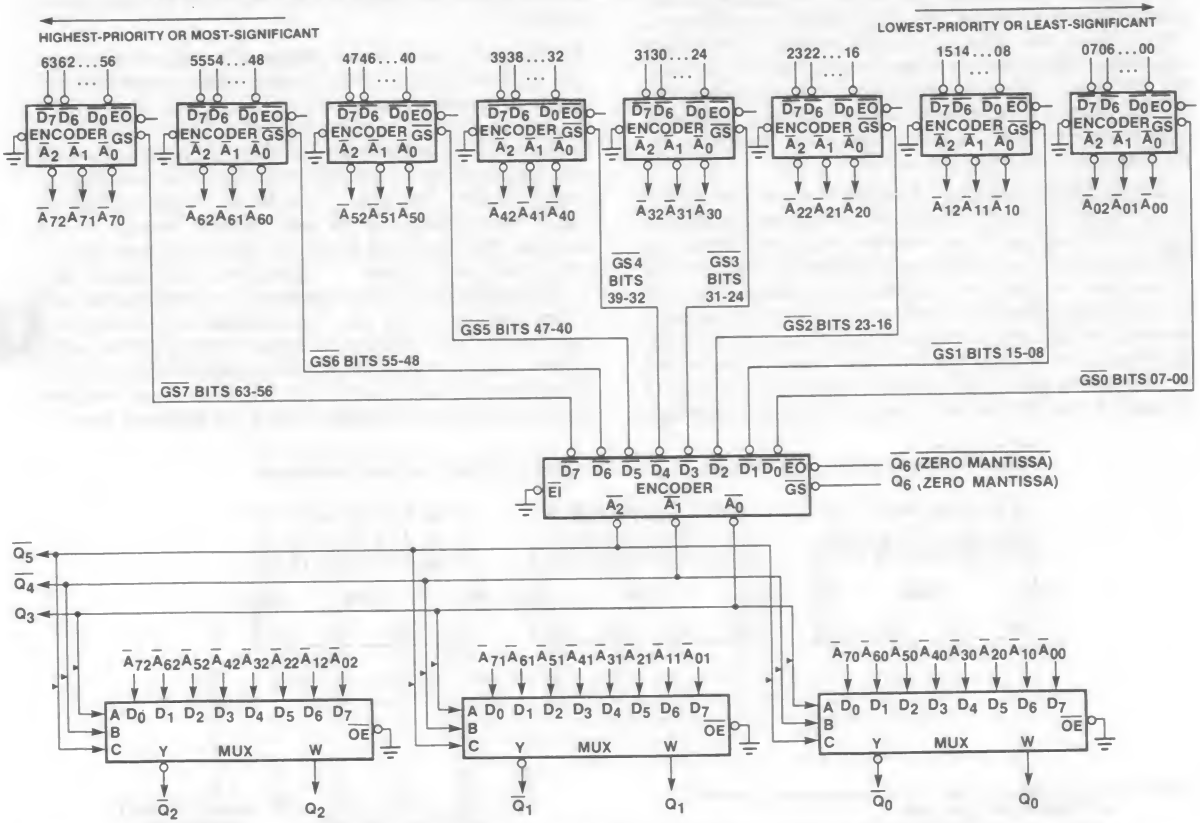


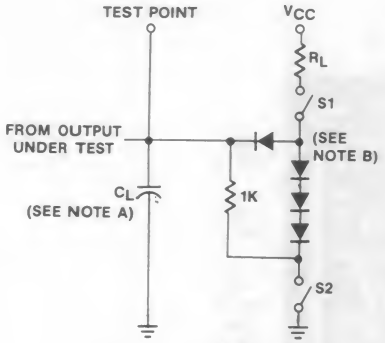
Figure 2. 64-Bit Leading-Zeroes Detector or Interrupt Scanner Using 'S348s and No External Components



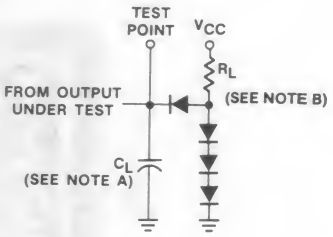
NOTE: Encoders here may be 'S148s or 'S348s; muxes may be 'S151s or 'S251s. If all 64 inputs are High, Q_5-Q_3 are in Hi-Z state, and Q_2-Q_0 are not meaningful.

Figure 3. Totally-Parallel 64-Bit Leading-Zeroes Detector or Interrupt Scanner

Standard Test Loads

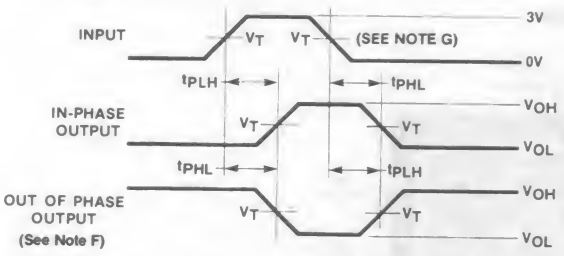


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

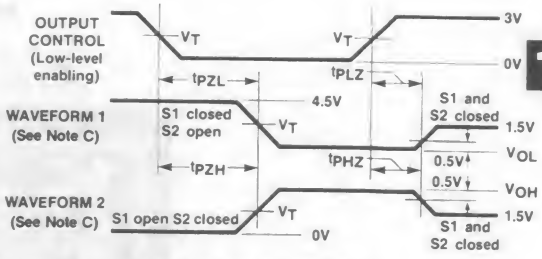


LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

Test Waveforms



PROPAGATION DELAY



ENABLE AND DISABLE

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

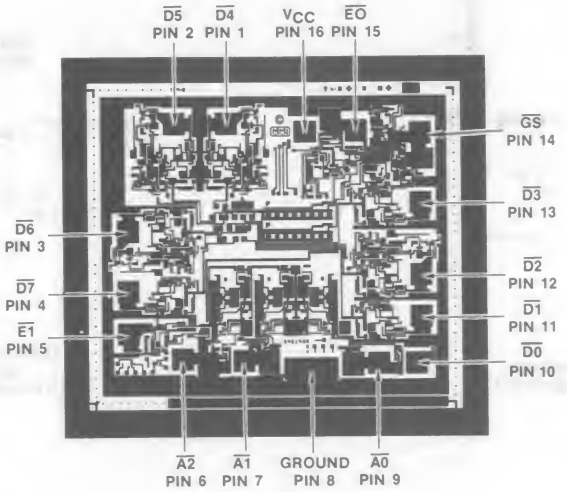
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and:

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

G. V_T = 1.5V

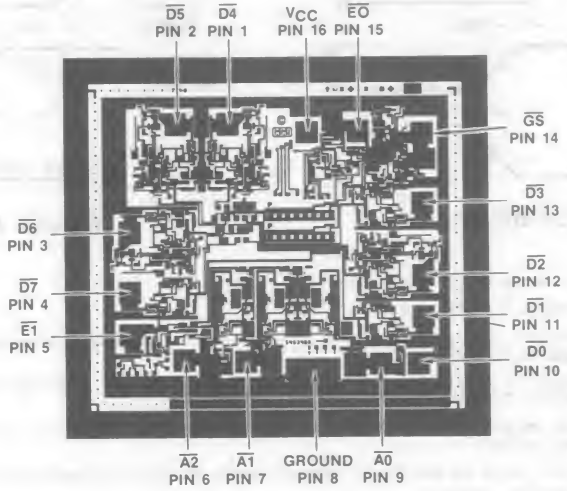
Die Configurations

SN54/74S148



DIE SIZE 0.081" x 0.070"

SN54/74S348



DIE SIZE 0.081" x 0.070"

Sine (0° to 90°) Look Up Table Using a 1024 X 10 ROM (5/6255 5/6256) 5/6086 5/6087

Features/Benefits

- **Input angle increments of 90°/1024 = .0879°**
- **10 bit binary outputs**
- **Low power dissipation. Typically 500 mw**
- **Fast access time 100 ns max.**
- **TTL compatible**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
5086/87	J24	Military
6086/87	J24	Commercial

Description

The 5255/6255, 1024 words by 10 bits Read Only Memory has been customized to make a sine θ look up table (5086/6086) for $0° \leq \theta < 90°$. The address inputs are used to divide the first 90° quadrant into angles increments of 90°/1024 words or .0879°/word. The memory outputs should be interpreted as binary weighted fractions where output 1 has a weight of 1/2 or .500, output 2 has a weight of 1/4 or .250, and so on until output 10 which has a weight of 1/1024 or .000976. The 10 bit output code has not been rounded off so that output error will always be positive and less than 1/1024 or .0009765. Round off error, in approximating the ROM input word, must be added or subtracted to the output error. For electrical characteristics and pin out refer to 6255 specifications (in ROM section).

Example 1:

Find the sine 45°

Let X = the ROM word where sine 45° is stored

$$\frac{X}{1024 \text{ words}} = \frac{45°}{90°}$$

X = word 512

Word 511 has the following stored data and interpretation:

Output #	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8	0_9	0_{10}
Stored Data	H	L	H	H	L	H	L	H	L	L
Binary Weight	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024

(H = TTL HIGH)

Adding the fractions wherever an "H" appears given.

$$\frac{1}{2} + \frac{1}{8} + \frac{1}{16} + \frac{1}{64} + \frac{1}{256} = .50000 + .12500 + .06250 + .01562 + .00391 = .70507$$

Handbook Value = .70711

Our Error = .70711 − .70703 = .00008

Example 2:

Find the sine 210°

This value is in quadrant three, therefore, $\theta' = 210° - 180°$ or 30°

Let X = the ROM word where sine 30° is stored $\frac{X}{1024 \text{ words}} = \frac{30°}{90°}$

X = word 341.33 (round off to word 341)

Word 341 has the following stored data and interpretation:

Output #	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8	0_9	0_{10}
Stored Data	L	H	H	H	H	H	H	H	H	H
Binary Weight	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024

Adding the fractions wherever an "H" appears gives 0.49902

The sine 210°, therefore, = −.49902 with the sign generated by external logic. Note that the address 341 to which we rounded off is actually the sine 29.97°.

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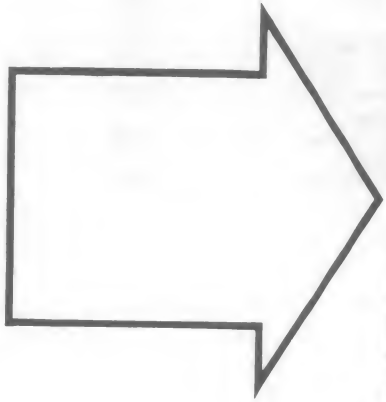


Multiplier/Divider Selection Guide

The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

Co-Processor Multiplier/Divider with Accumulator

DESCRIPTION	PART NUMBER	MAX MULTIPLICATION TIME/ MAX DIVISIONN TIME	PINS
8 Bits	SN74S508 SN54S508	.8 μs/2.2 μs	24
16 Bits	SN74S516 SN54S516	1.5 μs/3.5 μs	24

Cray Multipliers

DESCRIPTION	PART NUMBER	MAX DELAY	PINS
8x8 Multiplier (latched)	SN74S557	60 ns (X_i, Y_i to S_{15})	40
8x8 Multiplier (latched)	SN54S557	60 ns	40
8x8 Multiplier (latched)	SN74S558	60 ns	40
8x8 Multiplier (latched)	SN54S558	60 ns	40

Contents

Four New Ways to go Forth and Multiply

Chuck Hastings

Our Multiplier Population Explosion

Recently it has seemed as if every time you turned around Monolithic Memories was announcing *another* new multiplier. Want to catch your breath, and find out where each of these fits into the overall scheme of things? Read on.

Actually, there have been *four* new multipliers in all within the last two years plus two which had already been available for several years. In time order of introduction, these are:

Parts #	Description A
57/67558	150-nsec 8x8 Flow-Through Cray Multiplier B
57/67558-1	125-nsec 8x8 Flow-Through Cray Multiplier B
54/74S508	8-Bit Bus-Oriented Sequential Multiplier/ Divider
54/74S558	60-nsec 8x8 Flow-Through Cray Multiplier
54/74S557	60-nsec 8x8 Flow-Through Cray Multiplier with Transparent Output Latches
54/74S516	16-Bits Bus-Oriented Sequential Multiplier/ Divider

Notes: A. Times are worst-case times for commercial-temperature-range parts.
B. Obsolete. 54/74S558 replaces these in both new and existing designs.

You will notice that the above parts fall into two categories: 8x8 flow-through Cray multipliers, and bus-oriented sequential multiplier/dividers. Although all of these parts get referred to rather casually as "multipliers," there are major differences between the two general types; see Table 1 below.

The Cray Multipliers

The essential idea of a Cray multiplier, as originally put together by Seymour Cray in the late 1950s with discrete logic at Control Data Corporation, is to wire up an array of full adders in the form of a binary-arithmetic-multiplication pencil-and-paper example.[3] That is, everywhere that there is a "1" or a "0" in a longhand binary-multiplication example, the Cray type of multiplication uses a full adder. One may visualize a Cray multiplier functionally as a "diamond," as follows:

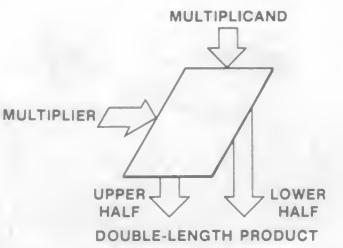


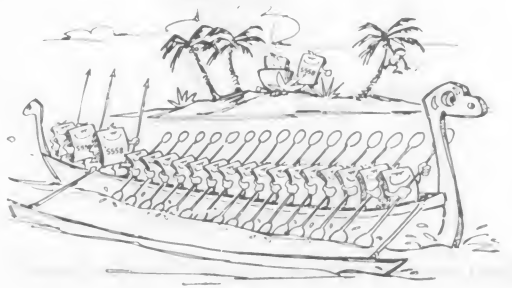
Figure 1. Pencil-and-Paper Analogy to Cray-Multiplier Operation

	8x8 Flow-Through Cray Multiplier	Bus-Oriented Sequential Multiplier/Divider
Role in System	*Building-block role* — as many as 34 parts used in one super-minicomputer (NORD-500 from Norsk Data[1]).	*Co-processor role* — one, or occasionally two, parts used in one microcomputer[2].
Internal Operation	Static arithmetic-logic network; multiplies without being clocked[3] using eight bits of the multiplier at a time.	State machine; requires clocking to operate; contains edge-triggered registers; sequenced by a state counter; multiplies using two bits of the multiplier at a time[4].
External Control	Controlled by several mode-control input signals.	Controlled by sequences of micro-opcodes which come from a microprocessor, a registered PAL, or some other sequential-control device.
Package	40-pin DIP.	24-pin DIP.
Operations Performed	Can only perform multiplication.	Can perform multiplication, division, and multiplication-with-accumulation.
Storage Capabilities	Either no storage capabilities (558 types) or optional storage for the double-length product only (557 types).	Four full-length registers; capable of storing both input operands and the double-length product.
Second Sources	Multiple-sourced (AMD, Fairchild, Monolithic Memories).	Sole-sourced; only bipolar *dividers* on the market.
Where Used	Initial usage has been in high-end minicomputers, array processors, and signal processors.	Initial usage has been in industrial-control microcomputers, digital moderns, military avionics, CRT graphic systems, video games, and cartographic analysis systems.
Future Prospects	Potential large market today since these parts are now low-cost and multiple-sourced, and should be used in *all* new minicomputer designs!	Potential huge world-wide market for enhancement of microprocessor, bit-slice processor, and microcomputer capabilities, and for small-scale signal processing!

Table 1. A comparison of the two types of Monolithic Memories Multipliers

Our 57/67558, introduced about half a decade ago, was the original *single-chip* Cray multiplier. To achieve what was for that time very high performance for a Schottky-TTL-technology part, the internal design of the 57/67558 also exploited other speed-freak multiplication techniques such as Booth multiplication[4] and Wallace-Tree addition[5]. All of these techniques achieve increased speed through extensive parallelism, and can be used at the system level as well as within LSI components. Subsequently, process improvements made it possible to offer a faster final-test option, the 57/67558-1, which attained a sales-volume level essentially equal to that of the original part.

About four years ago, AMD paid us the sincere compliment of second-sourcing these parts with the 75-nsec 25S558. Two years ago, we returned the compliment with the 60-nsec 54/74S558. All of these '558 parts, and the 70-nsec 54/74F558 announced by Fairchild, are fully compatible drop-in equivalents except for the variations in logic delay.



" ALL OF THESE TECHNIQUES ACHIEVE INCREASED SPEED THROUGH EXTENSIVE PARELLELISM."

When AMD introduced the 25S558, they introduced along with it the 80-nsec 25S557, a "metal option" of the same basic design with "transparent" output latches to hold the double-length product. "Transparent" means that the latches go away when you don't want them there; a latch-control line like that of the 54/74S373 controls whether these output latches store information, or simply behave as output buffers. Anyway, when we introduced our 54/74S558, we followed it within a few weeks with the 60-nsec 54/74S557, which is a much faster drop-in replacement for AMD's part. And subsequently, Fairchild has announced a 70-nsec 54/74F557.

Because AMD's 'S557 has the output latches implemented in TTL technology *after* the ECL-to-TTL converters, whereas our 'S557 has them implemented in ECL technology *before* the conversion, the latches operate much faster in ours. Our 'S557 is typically only about a nanosecond slower than our 'S558, whereas the logic-delay difference between AMD's two parts is considerably greater. Consequently, our margin of superiority over AMD for the 'S557 is even greater than for the 'S558.

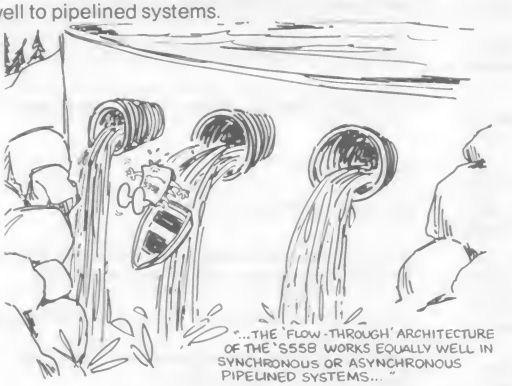
'S557/8 Cray multipliers come in a 40-pin dual-inline package, either ceramic or plastic. The data-bus outputs can sink up to 8 mA I_{OL}. Worst-case power-supply current is 280 mA.

Reference 5 discusses technical approaches to using Cray multipliers in high-performance minicomputers. The 'S558, together with PROMs organized in a "Wallace-tree" configuration, can sail right along at the rate of four 56x56 multiplications every microsecond, on the basis of fixed-point arithmetic with no renormalization. (See table 7 on page 16 of reference 5; the multiplication time is 238 nsec for a "division step," which is a fixed-point multiplication, and 319 nsec for a floating-point multiplication where extra time is required for renormalization and correction of the exponent of the product.) 34 'S558s or 'S557s are required to perform this multiplication if the computer system architecture does not call for the computation of the least-significant half of the double-length product; 49 are required if it does.

" ... THE 'S558, TOGETHER WITH PROMS ORGANIZED IN A "WALLACE-TREE" CONFIGURATION, CAN SAIL RIGHT ALONG AT THE RATE OF FOUR 56 x 56 MULTIPLICATIONS EVERY MICROSECOND. "

The "local" architecture of the multiplier section of a digital system can take two rather different forms. A minicomputer[5] which executes an unpredictable mixture of arithmetic and logical instructions one after the other, typically needs to be able to get the complete multiplication over and done with before going on to the next program step—which is probably not another multiplication. An array processor or digital correlator, however, tends to do very regular iterative computations; and the performance of such a system can often be greatly increased by a technique called "pipelining," in which the arithmetic unit consists of stages with registers or latches in between each stage, and partial computational results move from one stage to the next on each clock.

The "flow-through" architecture of the 'S558 works equally well in synchronous or asynchronous pipelined systems, but registers or latches must be provided externally. The 'S557, however, is actually a *superset* of the 'S558, and the added internal-output-latch feature adapts it particularly well to pipelined systems.



"...THE 'FLOW-THROUGH' ARCHITECTURE OF THE 'S558 WORKS EQUALLY WELL IN SYNCHRONOUS OR ASYNCHRONOUS PIPELINED SYSTEMS..."

Even a smaller-scale system can make effective use of these parts. To return to the case of 56x56 multiplication, which corresponds to the word-length needed for multiplying mantissas in several popular floating-point-number formats, an iterative clocked scheme using just seven multipliers, some adders, and an accumulator register can form the entire 112-bit double-length product in just seven multiply/add cycles. A number of mid-range minicomputers today multiply in this manner. The multipliers are configured as suggested by the following block diagram:

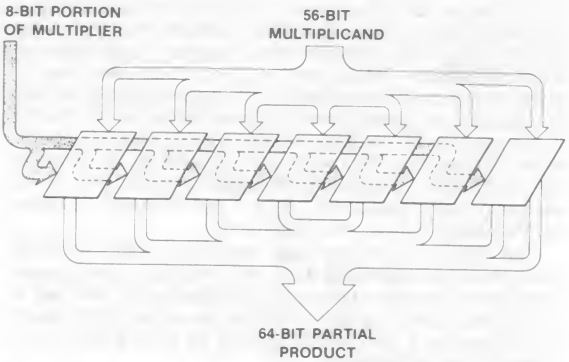


Figure 2. 8x56 Cray Multiplier In Diamond Representation

There is even an occasional 8-bit or 16-bit microprocessor-based system with a need for *very* fast multiplication, where 'S557/8s may get used as microprocessor peripherals[5] Digital-video systems, in particular electronic games, with "vector graphic" capabilities are one example.

The world of 'S557/8 applications has turned out to include *all* sizes of minicomputers, digital video systems, and signal processors—FFT (Fast Fourier Transform) processors, voice recognition equipment, radar systems, digital correlators and filters, electronic seismographs, brain and body scanners, and so forth. And there are many unexpected off-beat applications, such as real-time data-rescaling circuits in instruments, altogether too numerous to list here. After all, an 'S557/8 can multiply two 8-bit numbers together and output their entire 16-bit product in 60 nsec *worst-case*... less time than it would take a speeding bullet to move the distance equal to the thickness of this piece of paper. How's that for Supermultiplier?

The Multiplier/Dividers

The Monolithic Memories 'S516 and 'S508 are state-of-the-art TTL-compatible intelligent peripherals for microprocessors, somewhere between arithmetic sequential circuits and specialized bipolar microprocessors. The 'S516 and 'S508 each can perform any of 28 different multiply and multiply-and-accumulate instructions, plus any of 13 different divide instructions, at bipolar speeds under the control of an internal state counter. (See Figure 2 of the 'S516 data sheet.) The state counter's sequence is in turn guided by 3-bit instruction codes which are external inputs to the 'S516/508. The 'S516 computes with 16-bit binary numbers, and the 'S508 computes with 8-bit binary numbers, as the part numbers none-too-subtly imply.

A 16-bit bi-directional data bus connects the 'S516 with the outside world for bringing in multipliers, multiplicands, dividends, and divisors; and returning products, quotients and remainders. It also has clock (CK) and run/wait ($\overline{GO}$) inputs, and an overflow indication (OVR) output.

The 'S508 has all of the above inputs and outputs also, except that it has only an 8-bit bidirectional data bus. Since it comes in the same 24-pin package as the 'S516, it obviously has eight more pins available for other purposes. Four of these are used to bring out the internal-state-counter value; one each is used for a completion ($\overline{DONE}$) status output, an output-enable control (OE) input, and a master-reset ($\overline{MR}$) control input; and one is not used at all.

A simple, general interfacing scheme can be used to team a 'S516 with any of the currently popular 16-bit microprocessors,or an 'S508 with any 8-bit microprocessor. (See Figure 7 of the'S516 data sheet.) With a couple extra interface circuits, an'S516 can also be interfaced to an 8-bit microprocessor.Particularly if the system software is written in a highly-structured language such as PASCAL or FORTH, an'S516/508 can be retrofitted into an existing system with a large gain in performance and very little impact on either hardware or software — calls to the previous software-implemented one-step-at-a-time multiply and divide subroutines are simply rerouted to substitute a command from the microprocessor to the 'S516/508 to accept an operand and start its operation sequence.

The 'S516 and 'S508 are in fact two different "metal options" of one basic design; the 'S516 has twice as many data bits in each internal register. The 'S516 and 'S508 both have a worst-case clock rate of 6 MHz (commercial) or 5 MHz (military); the typical rate is 8 MHz. The simplest complete twos-complement 16x16 multiplication instruction can be performed in nine clock cycles by an 'S516, or in five by an 'S508, since 2-bits-at-a-time Booth multiplication is used;[4] thus, the worst-case time required by the 'S516 to multiply in this mode is 1.5 μsec for a commercial part, and for an 'S508 it is 833 nsec. On the same basis, 32/16 division can be done in 21 clock cycles, or 3.5 μsec worst-case, by an 'S516; and 16/8 division can be done in 13 clock cycles, or 2.2 μsec worst-case, by an 'S508.

An 'S516/508 can perform either positive or negative multiplication or multiply-accumulation, and many of the instructions provide for "chaining" of successive computations to eliminate extra operand transfers on the bus; these features further enhance the computational speed of the 'S516/508 in particular applications. Arithmetic can be either integer or fractional with respect to positioning of the results.

An 'S516 can powerfully enhance the capabilities of *any* present-day 16-bit or 8-bit microprocessor in a compute-bound application. In fact, it can be used in any digital system where there is a need to multiply and divide on a bus. An 'S508 can likewise enhance the capabilities of any 8-bit microprocessor.

The 'S516 comes in an industry-standard 600-mil 24-pin dual-inline package, modified to include an integral aluminum heatsink which does not add appreciably to the package height. It requires only +5V and ground power connections, and draws a worst-case power-supply current of 450mA (commercial) or 500mA (military). Power consumption is greatest at cold temperatures, and decreases substantially as operating temperature increases. The 16 databus inputs require at most 0.25mA input current; the other inputs require at most 1mA. The 16 databus outputs can sink up to 8mA I_{OL}. The 'S508 also fits the above description, except that its worst-case power-supply current is 380mA (commercial) or 400mA (military), and it has only 8 databus inputs and outputs.

In describing applications of these parts, it is difficult to know where to start — they can be used in almost any design where a microprocessor can be used, and you know how many places that is today. So, perhaps a good starting point is to see what uses customers have thought up all by themselves. One customer even used *two* 'S516s in "pingpong" mode on a single 16-bit bus! So, rather than merely speculating as to what these parts *might* be good for, here's a list of what Monolithic Memories's customers have already *proven* they are good for:

- Real-time control of heavy machinery[7]
- Low-cost, high-performance digital modems
- CRT graphics, including video games
- Military avionics
- Cartographic analysis

As it happens, the above are 'S516 applications, except that digital modem designs have been done with both the 'S516 and the 'S508. One of the 'S516 designs is already in production. In each of these applications, the microprocessor could have coped all right with the computational complexity, albeit at its own less-than-tremendous speed, but a 'S516 used together with the microprocessor can provide extra muscle for handling formidable problems.

Competition? Well, since there are no second sources for the 'S516, and no competitor at present has a similar fast part capable of performing division as well as multiplication, right now the 'S516 has no *direct* competition. Indirectly, there are some competing parts which perform *only* multiplication, and would have to perform division by Newton-Raphson iteration to be usable for any application where division is required. However, the 'S516 is (as far as we know) by far the lowest-priced *bipolar* 16-bit multiplier, and the other microprocessor peripheral chips which can perform division as well as multiplication are relatively-slow MOS devices. In one case, an 8-bit cascadable CMOS part requires a 50% reduction in clock rate to do 16-bit arithmetic. And considerable numerical-analysis and programming sophistication are required to implement Newton-Raphson division with *fixed-point* operands. (It's easier with floating-point operands.) In contrast, the 'S516/508 can be easily interfaced to almost any microprocessor using one or two PALs,* and can perform *either* multiplication or division on command[2]

The 'S516 is so much faster than the competing MOS chips that it can even take them on for *floating-point* computations (which some of them are designed to do) and *win*. A conference paper[8] describes the design of an 'S516-based S-100-bus card capable of beating an Intel 8087 2:1 on floating-point arithmetic.

Some competing parts, in particular the AMI 2811 and Nippon Electric μPD7720, include an on-board ROM which must be mask-programmed at the factory, which makes life difficult for small companies (or even larger ones) which are trying to get a microprocessor-based product to market quickly. Also, some competing parts require sequencing by external TTL jellybeans.

And, as for using AMD/TRW 64-pin 16x16 Cray multiplier chips as microprocessor peripherals, these cost much more than the 'S516, occupy about three times the circuit-board space, multiply faster, don't divide at all except by Newton-Raphson iteration, and also require one or two "overhead" microprocessor instructions to interface for a given arithmetic operation. From a *system* viewpoint, when this overhead time is reckoned with, these chips provide little actual gain in multiply performance over the 'S516 at lots of extra cost, and an actual loss in divide performance: the 'S516 is *much more cost-effective overall.*

'S516s potentially fit into many, many places in commercial, industrial, and military electronics, particularly into small-scale real-time systems. The part is fast enough to enhance the performance of the 16-bit Motorola 68000, Zilog Z8000, and Intel 8086, as well as that of *any* 8-bit microprocessor. It is also fast enough to considerably improve the multiplication and division performance of 16-bit 2901-based "bit-slice" bipolar microcomputers, which are often used as processors in desktop graphics CRT terminals.

It is worth bringing the 'S516 to the attention of *any* designer who is developing:

- A personal computer or small business computer.
- A word processor, or a more grandiose "office automation system."
- A cruise missile, or any other "smart weapon."
- A digital modem.
- A small-scale speech-processing system. (These are *very* multiplication-intensive. We have one magazine article on the 'S516 in such an application[9])
- A smart instrument, which does data conversion.
- An industrial control system, particularly one which must do many coordinate transformations.
- An all-digital studio-quality high-fidelity system.
- A cost-reduced computerized medical scanning system.
- A multimicroprocessor system for scientific computations.[10]

If an 'S516/508 is introduced into a system configured around an older microprocessor as a "co-processor" or

helpmate for the microprocessor, and the application is arithmetic-intensive, the end effect can be a major upgrading of performance at the system level.[2-7] Consequently, a major reason for designing these parts in is *microprocessor life-cycle enhancement*. In particular, many MOS microprocessors have single-length and double-length add and subtract instructions: but either they have no multiply or divide instructions at all, or else they perform their multiply and divide instructions so slowly as to jeopardize the ability of the entire system to handle its computing load in real time.

So picture, if you will, the entrepreneur or chief engineer of a firm making a successful microprocessor-based widget which has been on the market for a few months, which uses an older 8-bit microprocessor such as a 6800 or 8085 or Z80. Just when his/her sales are really taking off, here comes a new start-up competitor with a similar system, using a Motorola 68000, with added features and faster performance made possible by the 68000's 16-bit word length and multiply/divide capabilities. The 'S516 can, in this instance, serve as a "great equalizer"—it can be retrofitted into the older system as previously described, and provides even higher-speed multiplication and division than the 68000. (Enough so, actually, that there are designers using the 'S516 *with* the 68000.) Thus, the 'S516 can dramatically extend the life cycle of existing microcomputer systems based on microprocessors which either don't have multiplication and division instructions, or perform these operations relatively slowly.

"... THE 'S516 CAN DRAMATICALLY EXTEND THE LIFE CYCLE OF EXISTING MICROCOMPUTER SYSTEMS BASED ON MICROPROCESSORS WHICH EITHER DON'T HAVE MULTIPLICATION AND DIVISION INSTRUCTIONS, OR PERFORM THESE OPERATIONS RELATIVELY SLOWLY..."

'S508s are somewhat easier to control from a logic-design viewpoint than 'S516s, purely because they have more control inputs and outputs. However, the shorter 'S508 word length makes the part naturally fit into smaller-scale systems than those which might use an 'S516. Essentially, the 'S508 is optimized for small-scale systems.

Now that you know what these parts are, can't you think of at least half a dozen prime uses for them right in your own back yard?

References (all available from Monolithic Memories)

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2. "SN54/74S516 Co-Processor Supercharges 68000 arithmetic," Richard Wm. Blasco, Vincent Coli, Chuck Hastings and Suneel Rajpal, Monolithic Memories Application Note AN-114.
3. "How to Design Superspeed Cray Multipliers with 558s," Chuck Hastings, included within the SN54/74S557/8 data sheet.
4. "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-102.
5. "Big, Fast, and Simple — Algorithms, Architecture, and Components for High-End Superminis," Ehud Gordon and Chuck Hastings, Monolithic Memories Application Note AN-111.
6. "An 8x8 Multiplier and 8-bit μp Perform 16x16 Bit Multiplication,"Shai Mor, *EDN* November 5, 1979. Monolithic Memories Article Reprint AR-109.
7. "The Design and Application of a High-Speed Multiply/Divide Board for the STD Bus," Michael Linse, Gary Oliver, Kirk Bailey, and Michael Alan Baxter, Monolithic Memories Application Note AN-115.
8. "Minimum Chip-Count Number Cruncher Uses Bipolar Co-Processor," C. Hastings, E. Gordon, and R. Blasco. Monolithic Memories Conference Proceedings reprint CP-109.
9. "Medium-speed Multipliers Trim Cost, Shrink Band-width in Speed Transmission," Shlomo Waser and Allen Peterson, *Electronic Design,* February 1, 1979; pages 58-65. Monolithic Memories Article Reprint AR-107.
10. "A Synchronous Multi-Microprocessor System for Implementing Digital Signal Processing Algorithms," T.P. Barnwell, III and C.J.M. Hodges, *Southcon/82 Professional Program Session Record,* Session 21 reprint, paper 21/4.

8x8 Multiplier/Divider
SN54/74S508

Features/Benefits

- **Co-processor for enhancing the arithmetic speed of all present 8-bit microprocessors**
- **Bus-oriented organization**
- **24-pin package**
- **8/8 or 16/8 division in less than 2.2 μsec**
- **8x8 multiplication in less than .8 μsec**
- **28 different multiplication instructions such as "fractional multiply and accumulate"**
- **13 different divide instructions**
- **Self-contained and microprogrammable**

Description

The SN54/74S508 ('S508) is a bus-organized 8x8 Multiplier/Divider. The device provides both multiplication and division of 2s-complement 8-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S508 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 8-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

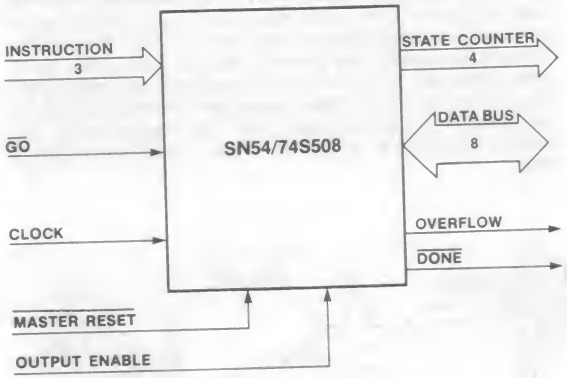
The 'S508 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands and reading of the double-length result, the device takes five clock periods — one for initialization, and four for the actual multiplication. A typical clock period is 125 ns, which gives a multiplication time of 500 ns typical for 8x8 multiplication, plus 125 ns additionally for initialization, or 625 ns in all. More complex multiplications will take additional clock periods for loading the additional oper-; ands. A simple division operation requires 8 + 4 = 12 clock periods for a typical time of 1.5 μs (16 bits/8 bits), also plus 125 ns for initialization, or 1.625 μs in all.

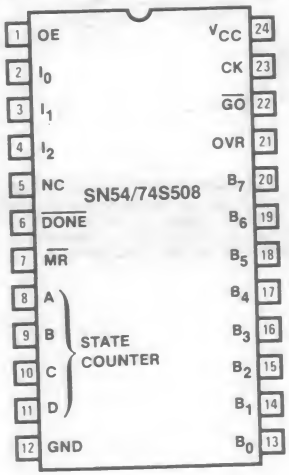
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S508	D24	Military
SN74S508	D24	Commercial

Logic Symbol



Pin Configuration



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Monolithic Memories MMI

INSTRUCTION SEQUENCE				OPERATION	CLOCK CYCLES
ARITHMETIC OPERATIONS					
			0	$X1 \cdot Y$	5
			1	$-X1 \cdot Y$	5
			2	$X1 \cdot Y + K_Z, K_W$	5
			3	$-X1 \cdot Y + K_Z, K_W$	5
			4	$K_Z, K_W/X1$	13
		5/6	0	$X \cdot Y$	6
		5/6	1	$-X \cdot Y$	6
		5/6	2	$X \cdot Y + K_Z, K_W$	6
		5/6	3	$-X \cdot Y + K_Z, K_W$	6
		5/6	4	K_W/X	14
		5/6	5	K_Z/X	14
	5/6	6	0	$X \cdot Y + Z$	7
	5/6	6	1	$-X \cdot Y + Z$	7
	5/6	6	2	$X \cdot Y + K_Z \cdot 2^{-8}$	7
	5/6	6	3	$-X \cdot Y + K_Z \cdot 2^{-8}$	7
	5/6	6	4	Z, W/X	15
	5/6	6	5	Z/X	15
5/6	6	6	0	$X \cdot Y + Z$, W	8
5/6	6	6	1	$-X \cdot Y + Z$, W	8
5/6	6	6	2	$X \cdot Y + W_{sign}$	8
5/6	6	6	3	$-X \cdot Y + W_{sign}$	8
5/6	6	6	4	W/X	16
5/6	6	6	5	W_{sign}/X	16
5/6	6	6	6	(See Note 9 below)	—
5/6	5/6	6	7	Load X, Load Z, Load W, Clear Z	3
READING OPERATIONS					
			7	Read Z	1
		7	7	Read Z, W	2
	7	7	7	Read Z, W, Z	3
7	7	7	7	Read Z, W, Z, W	4
		5	7	Round, then Read Z	2
	5	7	7	Round, then Read Z, W	3

NOTES:
1. X,Y are input multiplier and multiplicand.
2. X1 is the previous contents of the first rank of the X register, (either the old X or a new X).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. Z, W is a double-precision number. Z is the most significant half. Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
5. K_Z, K_W represents previous accumulator contents. K_Z is the most-significant half.
6. W_{sign} is a single-length signed number, with sign extension.
7. Maximum clock cycle = 167 ns for a 6-MHz clock.
8. If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+4 for multiplication and n+12 for division.
9. The code "5/6 6 6 6" represents an incomplete operation since it leaves the 'S508 in state 1 rather than in state 0, 8, or 10

Figure 1 'S508 Instruction Set (Partial List)

SUMMARY OF SIGNALS/PINS	
B_7-B_0	Bidirectional data bus inputs/outputs
I_2-I_0	Instruction (sequential control) input
A, B, C, D	Internal-state-counter outputs
CK	Clock pulse input
$\overline{GO}$	Chip activation input
OE	Output enable input
$\overline{MR}$	Master reset input
OVR	Arithmetic overflow output
$\overline{DONE}$	Arithmetic-operation completion output

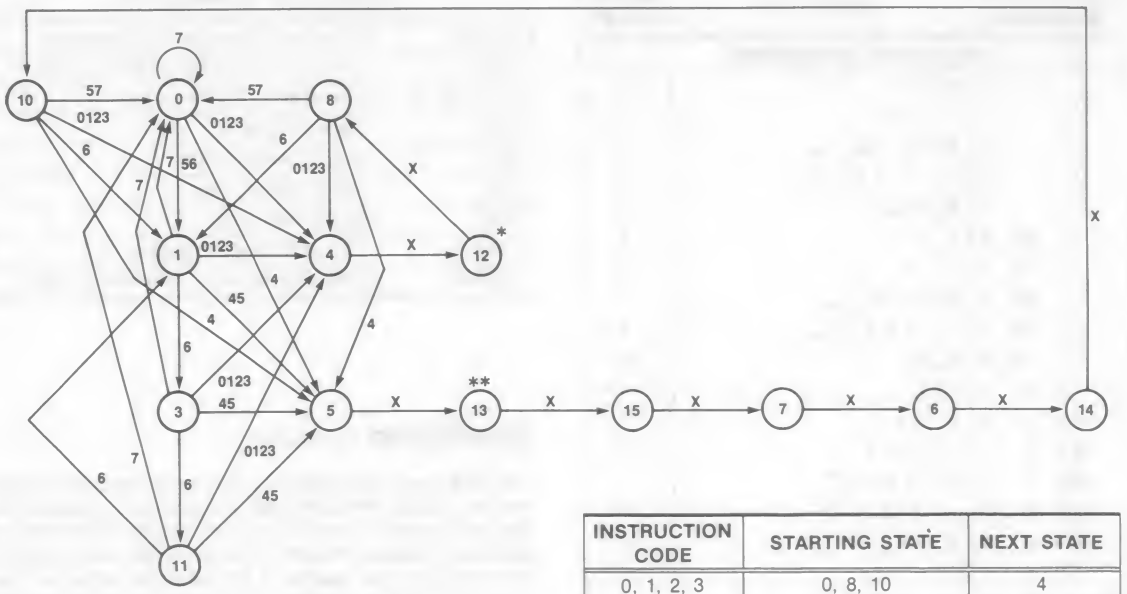
Description (continued)

The 'S508 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S508 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

Device Operation

The 'S508 contains four 8-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{GO}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{GO}$ is continually held HIGH, the 'S508 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S508 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{GO}$ goes LOW. Also, $\overline{GO}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S508 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 5 clock periods for a simple multiply or 13 clock periods for a simple divide, for example, the device is ready to place the result on the bus in time sequence.



* Loop 3 times for multiplication.
** Loop 6 times for fractional division, or 7 times for integer division.

INSTRUCTION CODE	STARTING STATE	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
5, 7	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

KEY:

The numbers inside the circles indicate the *state* of the 'S508 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. These four bits are available externally on the 'S508.

The next state of the 'S508 is a function of the present state and the instruction lines. For example if the 'S508 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S508 from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S508 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2 Transition Diagram for the 'S508 Multiplier/Divider

Three instruction inputs I_2, I_1, I_0, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13).

(continued next page)

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-complement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S508 8x8 Multiplier/Divider.

(continued page after next)

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8
X1 · Y	INS CODE	0	MULTIPLY						
	BUS	Y							
-X1 · Y	INS CODE	1	MULTIPLY						
	BUS	Y							
X1 · Y + K_Z, K_W	INS CODE	2	MULTIPLY						
	BUS	Y							
-X1 · Y + K_Z, K_W	INS CODE	3	MULTIPLY						
	BUS	Y							
X · Y	INS CODE	5/6	0	MULTIPLY					
	BUS	X	Y						
-X · Y	INS CODE	5/6	1	MULTIPLY					
	BUS	X	Y						
X · Y + K_Z, K_W	INS CODE	5/6	2	MULTIPLY					
	BUS	X	Y						
-X · Y + K_Z, K_W	INS CODE	5/6	3	MULTIPLY					
	BUS	X	Y						
X · Y + Z	INS CODE	5/6	6	0	MULTIPLY				
	BUS	X	Z	Y					
-X · Y + Z	INS CODE	5/6	6	1	MULTIPLY				
	BUS	X	Z	Y					
X · Y + $K_z \cdot 2^{-8}$	INS CODE	5/6	6	2	MULTIPLY				
	BUS	X	—	Y					
-X · Y + $K_z \cdot 2^{-8}$	INS CODE	5/6	6	3	MULTIPLY				
	BUS	X	—	Y					
X · Y + Z, W	INS CODE	5/6	6	6	0	MULTIPLY			
	BUS	X	Z	W	Y				
-X · Y + Z, W	INS CODE	5/6	6	6	1	MULTIPLY			
	BUS	X	Z	W	Y				
X · Y + W_{sign}	INS CODE	5/6	6	6	2	MULTIPLY			
	BUS	X	—	W	Y				
-X · Y + W_{sign}	INS CODE	5/6	6	6	3	MULTIPLY			
	BUS	X	—	W	Y				

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) $K_Z \cdot 2^{-8}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Fractional or integer arithmetic is specified by having the next-to-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

Figure 3 Multiplication Codes and Times for 8x8 Multiplication in the 'S508

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
K_Z, K_W/X_1	INS CODE	4	DIVIDE											1			
	BUS	—															
K_W/X	INS CODE	5/6	4	DIVIDE											1		
	BUS	X	—														
K_Z/X	INS CODE	5/6	5	DIVIDE											1		
	BUS	X	—														
Z, W/X	INS CODE	5/6	6	4	DIVIDE											1	
	BUS	X	Z	W													
Z/X	INS CODE	5/6	6	5	DIVIDE											1	
	BUS	X	Z	—													
W/X	INS CODE	5/6	6	6	4	DIVIDE											1
	BUS	X	—	W	—												
W_{sign}/X	INS CODE	5/6	6	6	5	DIVIDE											1
	BUS	X	O	W	—												

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) Fractional division divides a 16-bit 2s-complement number in 1 clock period less than integer division.
3) W_{sign} is a single-length signed number, with sign-extension as needed.
4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.
5) Fractional or integer arithmetic is specified by having the operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4 Division Codes and Time for 16/8 Division in 'S508

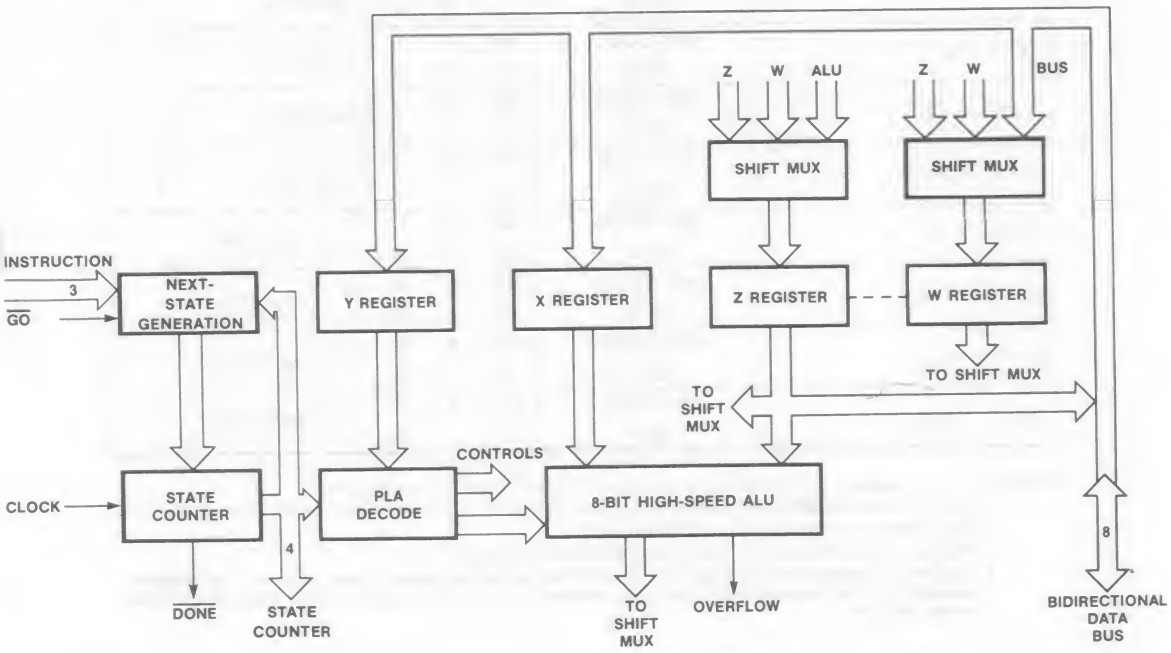


Figure 5 Internal Architecture of the 'S508

Multiplication

The 'S508 provides 2s-complement 8-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S508 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C,(A + B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 8-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{GO}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S508 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Continual read operations at state 0 just swap the contents of register Z and W.

The 'S508 has a direct master reset input $\overline{MR}$. Alternatively, initialization of the 'S508 can also easily be performed by continually presenting instruction code 7, which after a maximum of 13 clock periods forces the machine back to state 0.

Integer and Fractional Arithmetic

The 'S508 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end and the least-significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{15} to $+2^{15}-1$; the operands X and Y, and single-length results, are in the range -2^7 to $+2^7-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 *(negative)*. The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1}. The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-15}$ and the operands X and Y and single-length results are in the range -1 to $+1-2^7$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the 'S508 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S508 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The 'S508 looks at the most-significant bit of the least-significant half of the product W_7, and adds 1 to the most-significant half of the product at the least-significant end if W_7 is a 1. After the operation, the 'S508 is in state 0, so that the rounded product can be read, and the W register is clear.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S508 goes to state 0, so that a read operation can be performed, and the W register is clear.

Overflow

The 'S508 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: $(-1)x(-1)=+1$, which cannot be held in the 'S508's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-15}$, then the overflow flipflop will be set.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-7}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^7.

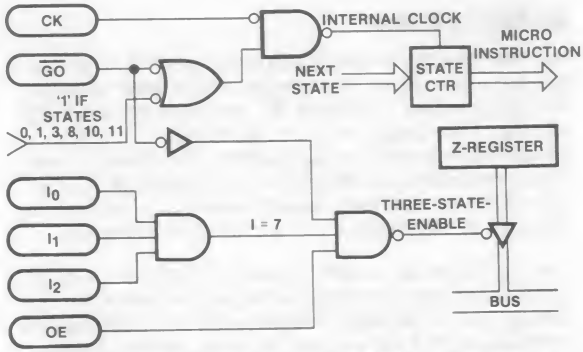


Figure 6 'S508 Internal Circuitry of "$\overline{GO}$" Line and Three-State-Enable.

During the states 0, 1, 2, 3, 8, 10, 11, the "GO" line ($\overline{GO}$) is logic HIGH then the machine will be in a wait state until $\overline{GO}$ goes to logic LOW.

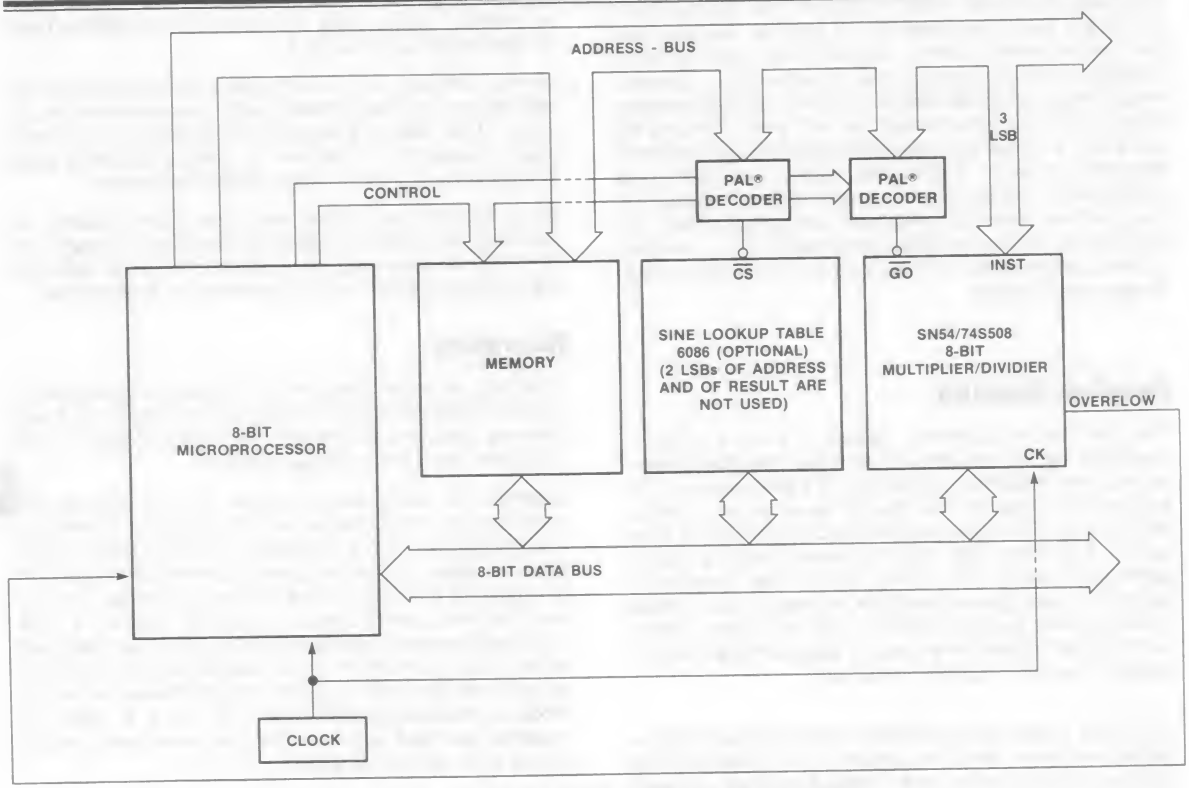


Figure 7 Interfacing the 'S508 to an 8-bit Microprocessor

Figure 7 shows the block diagram of a minimum 8-bit microprocessor system with its arithmetic capabilities enhanced by the use of a 'S508 8x8 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S508 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S508 is assigned address 100; then any address in the range of 100-107 will enable the 'S508 (i.e., the $\overline{GO}$ line is LOW). Thus, if the address is 100 the 'S508 instruction is 0; if the address is 106 the 'S508 instruction is 6; and so forth.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		125†	0		75	°C
f_{MAX}	Clock frequency	8	5			6			MHz
t_{CWP}	Positive clock pulse width	8	90			70			ns
t_{CWN}	Negative clock pulse width	8	60			50			ns
t_{BS}	Bus setup time for inputting data *	8	60			50			ns
t_{BH}	Bus hold time for inputting data *	8	45			35			ns
t_{INSS}	Instruction, $\overline{GO}$ setup time	8	10			10			ns
t_{INSH}	Instruction, $\overline{GO}$ hold time	8	20			20			ns

* During operations when the bus is being used to input data.
† Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	B_7-B_0			–250	µA
			All other inputs			–1	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				250	µA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN I_{OL} = 8mA			0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN I_{OH} = –2mA		2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX V_O = 0V		–10		–90	mA
I_{CC}	Supply current	V_{CC} = MAX	SN54S508		300	400	mA
			SN74S508		300	380	

* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

12

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{BO}	Bus output delay for outputting data*		8		70	120		70	95	ns
t_{PXZ}	Output disable delay	From I_2-I_0 to bus			40	70		40	65	ns
		From OE, $\overline{GO}$ to bus			20	50		20	40	
t_{PZX}	Output enable delay	From I_2-I_0 to bus			45	90		45	80	ns
		From OE, $\overline{GO}$ to bus			25	55		25	45	
t_{OVR}	Overflow output delay from CK		8		70	120		70	95	ns
t_{DN}	$\overline{Done}$ output delay		8		30	90		30	70	ns

* During operations when the bus is being used to output data.

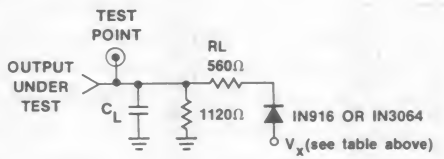
AC Test Conditions

Inputs $0V_{LOW}$, $3V_{HIGH}$. Rise and fall time 1–3ns from 1V to 2V. Measurements made from $1.5V_{IN}$ to $1.5V_{OUT}$, except T_{PXZ} measured by a delta in the outputs of 0.5V from V_{OL} or V_{OH} respectively.

Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.

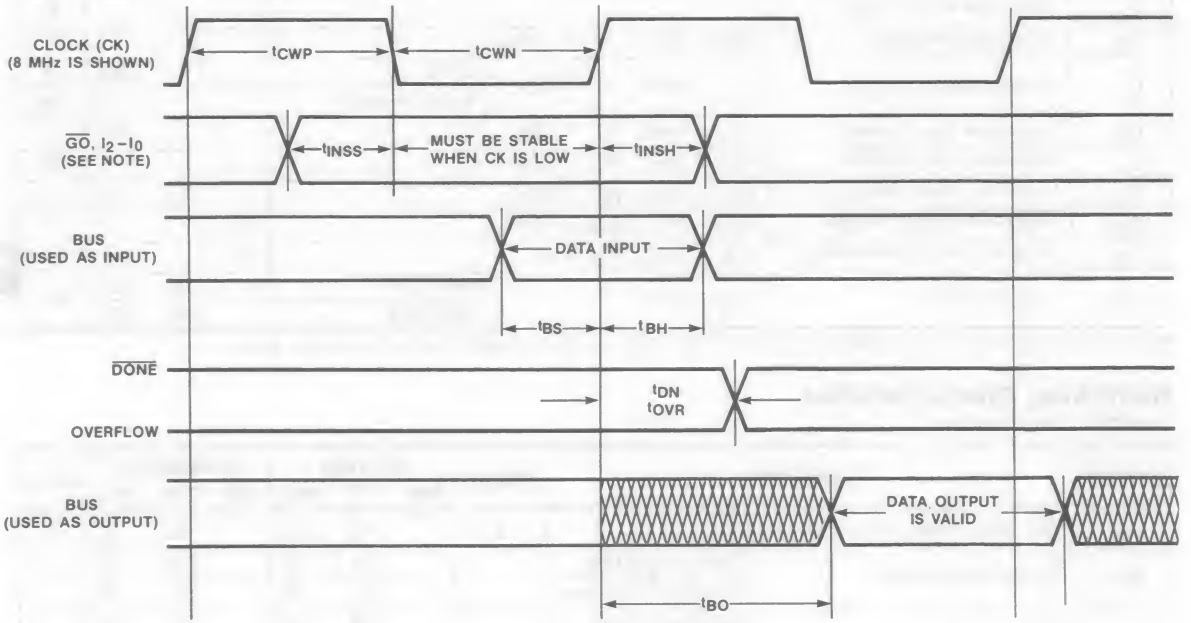
Load Test Circuit



Test Waveforms

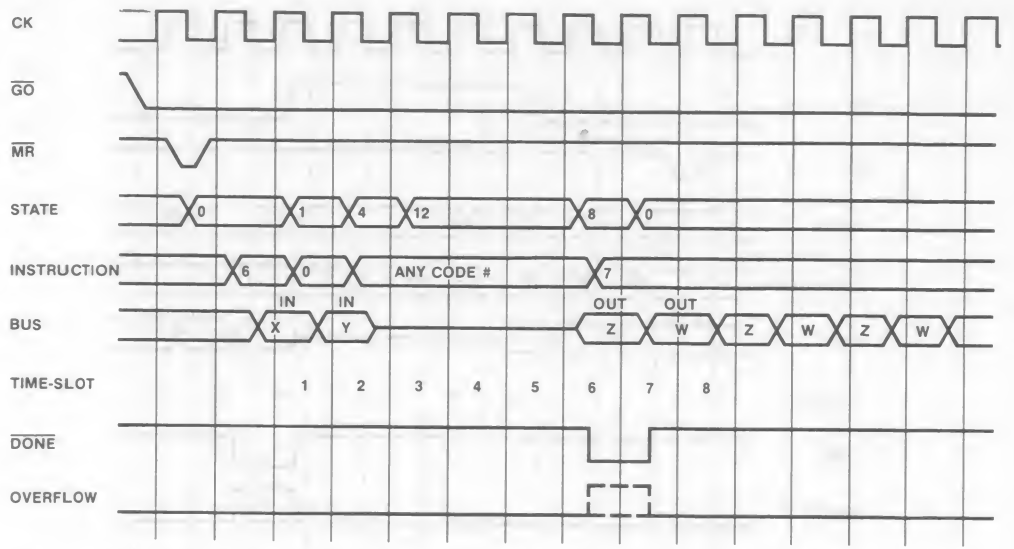
TEST	V_X*		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	t_{PLZ}	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	t_{PZH}	t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

*At diode; see "Test Circuit" figure below.



NOTE: $\overline{GO}$ and I_2-I_0 can change only when CK is high.

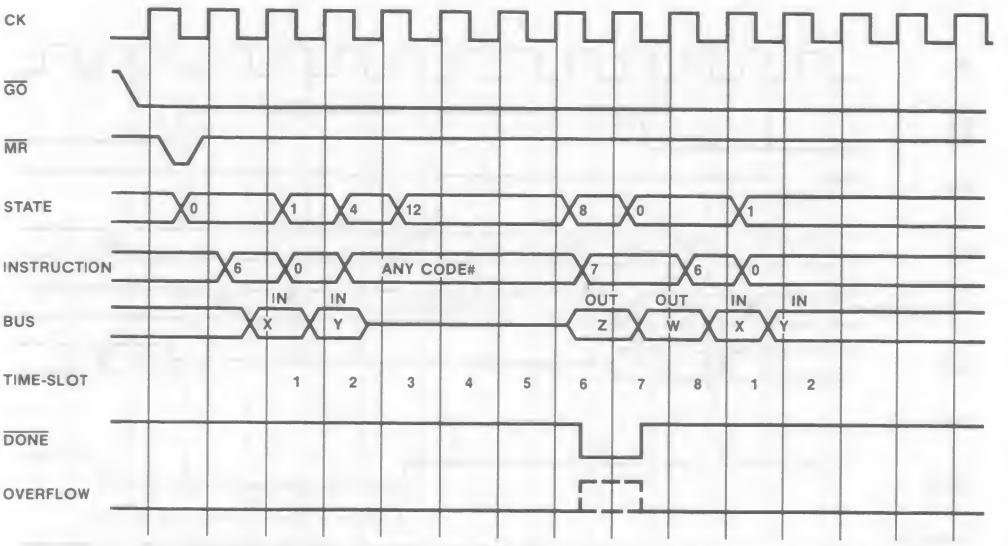
Figure 8 Timing diagram of the 'S508



NOTES: Register Z is read at the same time that the "done" signal is set. If the instruction remains at code 7 after time-slot 7, the contents of registers Z and W are swapped each cycle.

"Any code" means code 0 through 7. However code 6 will load a new value of X, and code 7 will cause the 'S508 to attempt to drive the data bus.

Figure 9 Instruction Timing Example #1: Load X, Load Y, Multiply, Read W. by presenting code 7 on the instruction lines during the last multiply cycle (state 8), the results may be read during time slots 6 and 7.

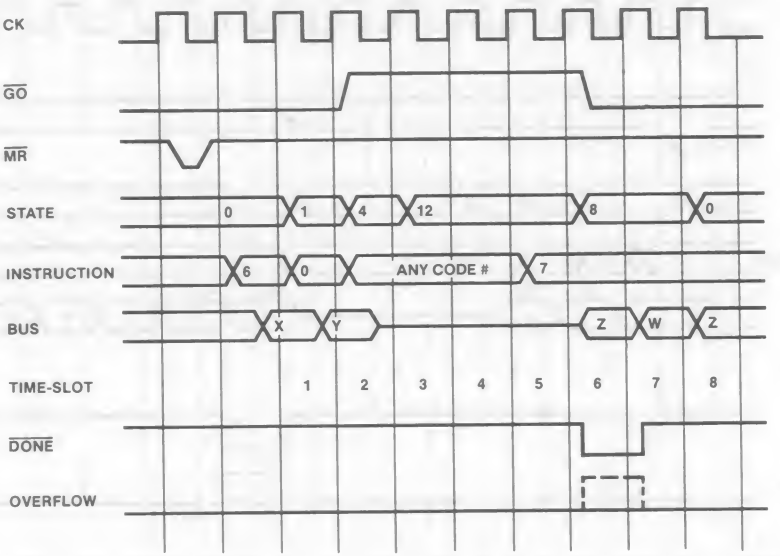


NOTES: The instruction lines may be changed only when CK is high.

#"Any code" means code 0 through code 7.

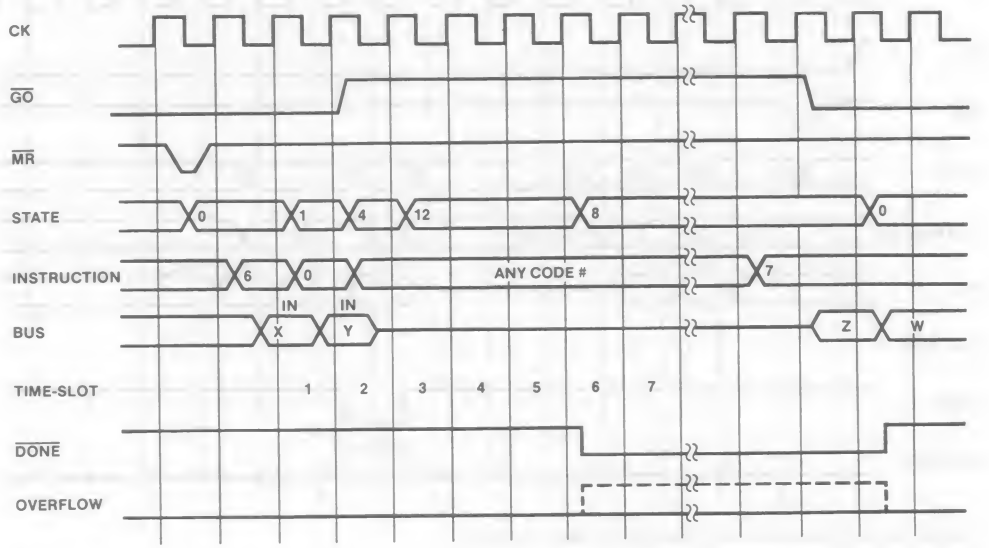
Code 6 may be used here since a new X enplicitly gets loaded for the next multiply operation. However, code 7 will cause the 'S508 to attempt to drive the data bus.

Figure 10 Instruction Timing Example #2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W".



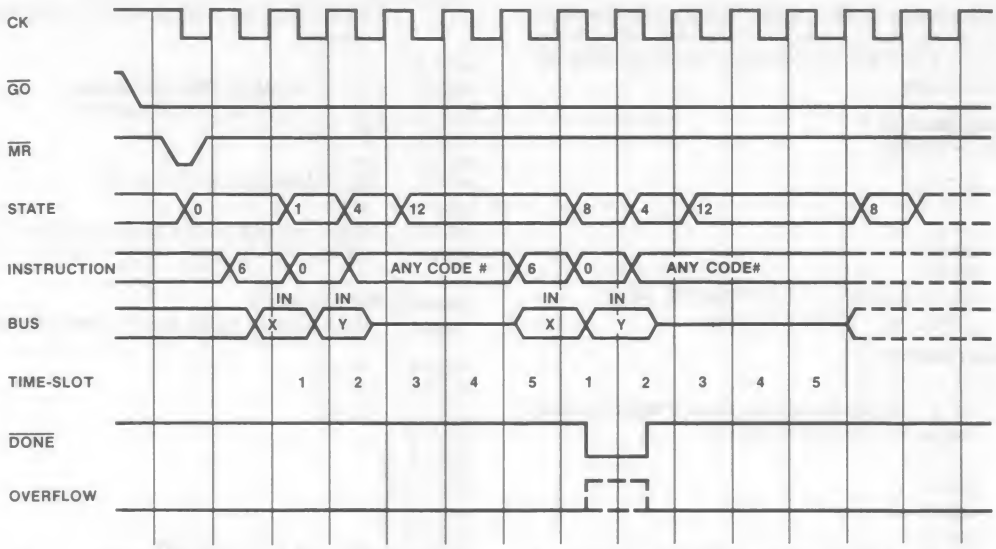
NOTE: If code 7 is given (instead of code 0 through 6), the first data that is read from the bus after the DONE signal is set (time-slot 7) is W and not Z. However, Z is read at time-slot 8.
#"Any code" means code 0 through code 7.

Figure 11 Instruction Timing Example #3: Load X, Load Y, Multiply, Read Z, Read W. This timing diagram corresponds to Table 1. Only after the "Done" signal is set (after four clock pulses of the operation cycles), the result is read — Z during time-slot 7, and W during time-slot 8.



NOTE:
"Any code" means code 0 through code 7. Code 6 or code 7 may be used here. Since GO is HIGH, no new X can be loaded and the 'S508 can not attempt to drive the bus.

Figure 12 Instruction Timing Example #4: Load X, Load Y, Multiply, Wait, Read Z, Read W.



NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example #3 for $\sum_{i=1}^{N} X_i \cdot Y_i$

#"Any code" means code 0 through code 7.
†Code 6 allows loading of a new X value in state 12 and it takes the 'S508 to state 8. In state 8, Y is loaded via instruction 2 and the multiply-accumulate operation is initiated.

Figure 13 Instruction Timing Example #5: Sum of Products

Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X·Y (A·B)

INST 6	X ← A	
INST 0	Y ← B	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST 7	MULT and READ	Z = 8 MSB OF (A·B)
INST 7	READ	W = 8 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A · C)

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

INST 0	Y ← C	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST 7	MULT and READ	Z = 8 MSB OF (A·C)
INST 7	READ	W = 8 LSB OF (A·C)

Programming Example 3

Calculating $\sum_{i=1}^{N} X_i \cdot Y_i$ (A·B + C·D + E·F + ...)

In this case we read only after N multiplications. A new X_{i+1} is loaded during the multiplication process for X_iY_i.

Assume N = 3.

The sequence of instructions and operations for calculating

$\sum_{i=1}^{3} X_i \cdot Y_i$ is: (A·B + C·D + E·F)

N = 1	INST 6	X ← A	
	INST 0	Y ← B	
	INST X	MULT	Perform A·B
	INST X	MULT	
	INST X	MULT	
N = 2	INST 6	MULT and LOAD X ← C Z ← 8 MSB of (A·B) W ← 8 LSB of (A·B)	
	INST 2	Y ← D	
	INST X	MULT	Perform C·D + (K_Z, K_W)
	INST X	MULT	
	INST X	MULT	
N = 3	INST 6	MULT and LOAD X ← E Z ← 8 MSB of (C·D + A·B) W ← 8 LSB of (C·D + A·B)	
	INST 2	Y ← F	
	INST X	MULT	Perform E·F + (K_Z, K_W)
	INST X	MULT	
	INST X	MULT	
READ Z	INST 7	MULT and READ Z = 8 MSB of (E·F + C·D + A·B)	
READ W	INST 7	READ W = 8 LSB of (E·F + C·D + A·B)	

Programming Example 4

Multiplication plus a constant (A·B + Constant (16 bits))

Assume that the constant is a 16-bit 2s-complement number.

INST 6	X ← A	
INST 6	Z ← C	LOAD 8 MSB of constant
INST 6	W ← D	LOAD 8 LSB of constant
INST 0	Y ← B	
INST X	MULT	Perform A·B + (Z, W)
INST X	MULT	
INST X	MULT	
INST 7	MULT and READ	Z = 8 MSB of (A·B + (C, D))
INST 7	READ	W = 8 LSB of (A·B + C, D)

Programming Example 5

Dividing a 16-bit number by an 8-bit number ((B, C)/A)

INST 6	X ← A
INST 6	Z ← B
INST 4	W ← C
INST X (×11)	Perform Division $\frac{(Z, W)}{X}$
INST 7	DIVIDE and READ the quotient Z = $\frac{(B, C)}{A}$
INST 7	READ the remainder W of $\frac{(B, C)}{A}$

16x16 Multiplier/Divider
SN54/74S516

Features/Benefits

- **Co-processor for enhancing the arithmetic speed of all present 16-bit and 8-bit microprocessors**
- **Bus-oriented organization**
- **24-pin package**
- **16/16 or 32/16 division in less than 3.5 μsec**
- **16x16 multiplication in less than 1.5 μsec**
- **28 different multiplication instructions such as "fractional multiply and accumulate"**
- **13 different divide instructions**
- **Self-contained and microprogrammable**

Description

The SN54/74S516 ('S516) is a bus-organized 16x16 Multiplier/Divider. The device provides both multiplication and division of 2s-complement 16-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S516 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 16-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

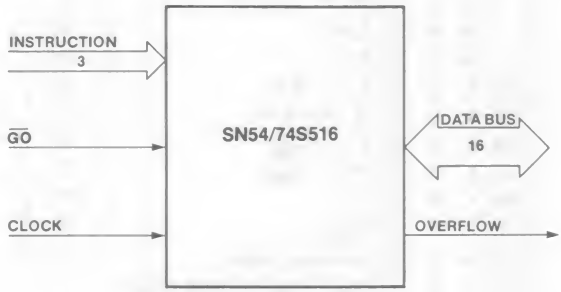
The 'S516 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands the device takes nine clock periods — one for initialization, and eight for the actual multiplication. A realistic clock period is 167 ns, which gives a multiplication time of 1333 ns typical for 16x16 multiplication, plus 167 ns additionally for initialization, or 1500 ns in all. More complex multiplications will take additional clock periods for loading the additional operands. A simple division operation requires 16 + 4 = 20 clock periods for a typical time of 3.333 ns (32 bits/16 bits), also plus 167 ns for initialization, or 3500 ns in all.

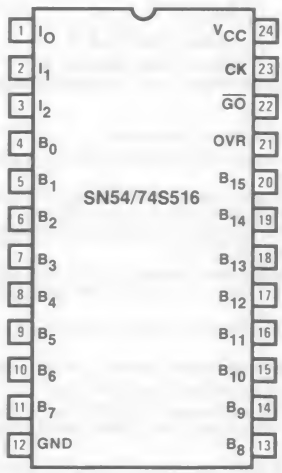
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S516	T24	Military
SN74S516	T24	Commercial

Logic Symbol



Pin Configuration



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2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

INSTRUCTION SEQUENCE				OPERATION	CLOCK CYCLES
ARITHMETIC OPERATIONS					
			0	$X1 \cdot Y$	9
			1	$-X1 \cdot Y$	9
			2	$X1 \cdot Y + K_Z, K_W$	9
			3	$-X1 \cdot Y + K_Z, K_W$	9
			4	$K_Z, K_W/X1$	21
		5/6	0	$X \cdot Y$	10
		5/6	1	$-X \cdot Y$	10
		5/6	2	$X \cdot Y + K_Z, K_W$	10
		5/6	3	$-X \cdot Y + K_Z, K_W$	10
		5/6	4	K_W/X	22
		5/6	5	K_Z/X	22
	5/6	6	0	$X \cdot Y + Z$	11
	5/6	6	1	$-X \cdot Y + Z$	11
	5/6	6	2	$X \cdot Y + K_Z \cdot 2^{-16}$	11
	5/6	6	3	$-X \cdot Y + K_Z \cdot 2^{-16}$	11
	5/6	6	4	Z, W/X	23
	5/6	6	5	Z/X	23
5/6	6	6	0	$X \cdot Y + Z$, W	12
5/6	6	6	1	$-X \cdot Y + Z$, W	12
5/6	6	6	2	$X \cdot Y + W_{sign}$	12
5/6	6	6	3	$-X \cdot Y + W_{sign}$	12
5/6	6	6	4	W/X	24
5/6	6	6	5	W_{sign}/X	24
5/6	6	6	6	(See Note 9 below.)	—
5/6	6	6	7	Load X, Load Z, Load W, Clear Z	4
	5/6	6	7	Load X, Load Z, Read Z	3
READING OPERATIONS					
			7	Read Z	1
		7	7	Read Z, W	2
	7	7	7	Read Z, W, Z	3
7	7	7	7	Read Z, W, Z, W	4
		5	7	Round, then Read Z	2
	5	7	7	Round, then Read Z, W	3

NOTES:
1. X,Y are input multiplier and multiplicand.
2. X1 is the previous contents of the first rank of the X register (either the old X or a new X).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. Z, W is a double-precision number. Z is the most significant half. Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
5. K_Z, K_W represents previous accumulator contents. K_Z is the most-significant half.
6. W_{sign} is a single-length signed number, with sign extension.
7. Maximum clock cycle = 167 ns for an 6-MHz clock.
8. If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+8 for multiplication and n+20 for division.
9. The code "5/6 6 6 6" represents an incomplete operation since it leaves the 'S516 in state 1 rather than in state 0, 8, or 10.

Figure 1 'S516 Instruction Set (Partial List)

SUMMARY OF SIGNALS/PINS	
B_{15}-B_0	Bidirectional data bus inputs/outputs
I_2-I_0	Instruction (sequential control) input
CK	Clock pulse input
$\overline{GO}$	Chip activation input
OVR	Arithmetic overflow output

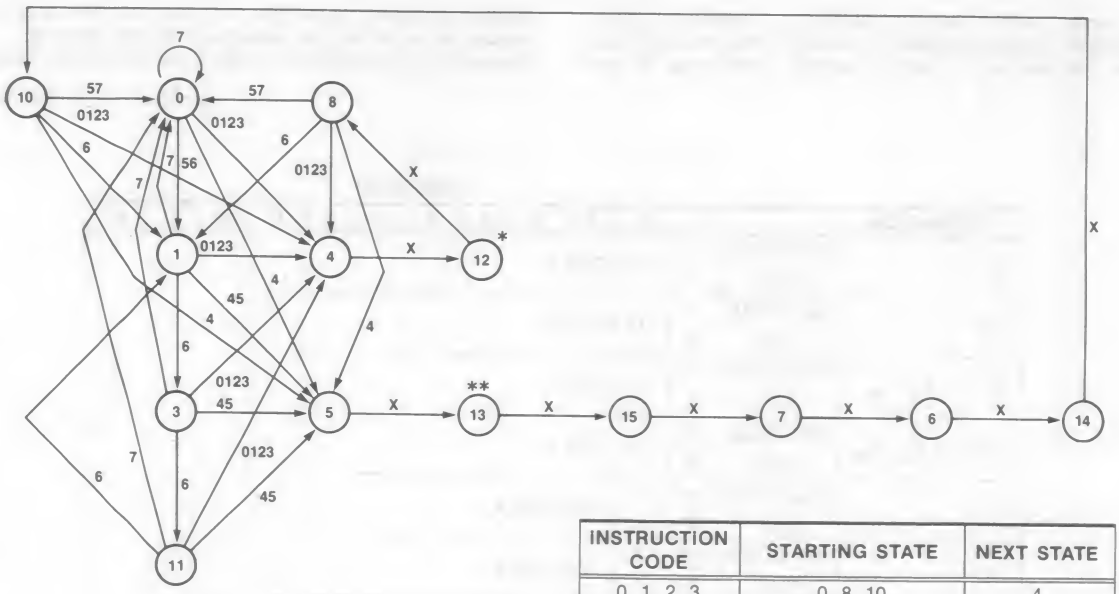
Description (continued)

The 'S516 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S516 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

Device Operation

The 'S516 contains four 16-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{GO}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{GO}$ is continually held HIGH, the 'S516 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S516 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{GO}$ goes LOW. Also, $\overline{GO}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S516 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 9 clock periods for a simple multiply or 21 clock periods for a simple divide, for example, the result is placed on the bus in time sequence.



INSTRUCTION CODE	STARTING STATE	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
5, 7	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

*Loop 7 times for multiplication.
**Loop 14 times for fractional division, or 15 times for integer division.

KEY:

The numbers inside the circles indicate the *state* of the 'S516 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. (These four bits are not available externally on the 'S516.)

The next state of the 'S516 is a function of the present state and the instruction lines. For example if the 'S516 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S516 from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S516 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2 Transition Diagram for the 'S516 Multiplier/Divider

Three instruction inputs I_2, I_1, I_0, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13).

(continued next page)

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-complement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S516 16x16 Multiplier/Divider.

(continued page after next)

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12
$X1 \cdot Y$	INS CODE	0	MULTIPLY										
	BUS	Y											
$-X1 \cdot Y$	INS CODE	1	MULTIPLY										
	BUS	Y											
$X1 \cdot Y + K_Z, K_W$	INS CODE	2	MULTIPLY										
	BUS	Y											
$-X1 \cdot Y + K_Z, K_W$	INS CODE	3	MULTIPLY										
	BUS	Y											
$X \cdot Y$	INS CODE	5/6	0	MULTIPLY									
	BUS	X	Y										
$-X \cdot Y$	INS CODE	5/6	1	MULTIPLY									
	BUS	X	Y										
$X \cdot Y + K_Z, K_W$	INS CODE	5/6	2	MULTIPLY									
	BUS	X	Y										
$-X \cdot Y + K_Z, K_W$	INS CODE	5/6	3	MULTIPLY									
	BUS	X	Y										
$X \cdot Y + Z$	INS CODE	5/6	6	0	MULTIPLY								
	BUS	X	Z	Y									
$-X \cdot Y + Z$	INS CODE	5/6	6	1	MULTIPLY								
	BUS	X	Z	Y									
$X \cdot Y + K_Z \cdot 2^{-16}$	INS CODE	5/6	6	2	MULTIPLY								
	BUS	X	—	Y									
$-X \cdot Y + K_Z \cdot 2^{-16}$	INS CODE	5/6	6	3	MULTIPLY								
	BUS	X	—	Y									
$X \cdot Y + Z, W$	INS CODE	5/6	6	6	0	MULTIPLY							
	BUS	X	Z	W	Y								
$-X \cdot Y + Z, W$	INS CODE	5/6	6	6	1	MULTIPLY							
	BUS	X	Z	W	Y								
$X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	2	MULTIPLY							
	BUS	X	—	W	Y								
$-X \cdot Y + W_{sign}$	INS CODE	5/6	6	6	3	MULTIPLY							
	BUS	X	—	W	Y								

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).

2) $K_Z \cdot 2^{-16}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.

3) W_{sign} is a single-length signed number, with sign-extension as needed.

4) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

Figure 3 Multiplication Codes and Times for 16x16 Multiplication in the 'S516

OPERATION		TIME-SLOT 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
$K_Z, K_W/X_1$	INS CODE	4	DIVIDE																			1			
	BUS	—																							
K_W/X	INS CODE	5/6	4	DIVIDE																			1		
	BUS	X	—																						
K_Z/X	INS CODE	5/6	5	DIVIDE																			1		
	BUS	X	—																						
Z, W/X	INS CODE	5/6	6	4	DIVIDE																			1	
	BUS	X	Z	W																					
Z/X	INS CODE	5/6	6	5	DIVIDE																			1	
	BUS	X	Z	—																					
W/X	INS CODE	5/6	6	6	4	DIVIDE																			1
	BUS	X	—	W	—																				
W_{sign}/X	INS CODE	5/6	6	6	5	DIVIDE																			1
	BUS	X	0	W	—																				

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).
2) Fractional division divides a 32-bit 2s-complement number in 1 clock period less than integer division.
3) W_{sign} is s single-length signed number, with sign-extension as needed.
4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.
5) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent *two* instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4 Division Codes and Time for 32/16 Division in 'S516

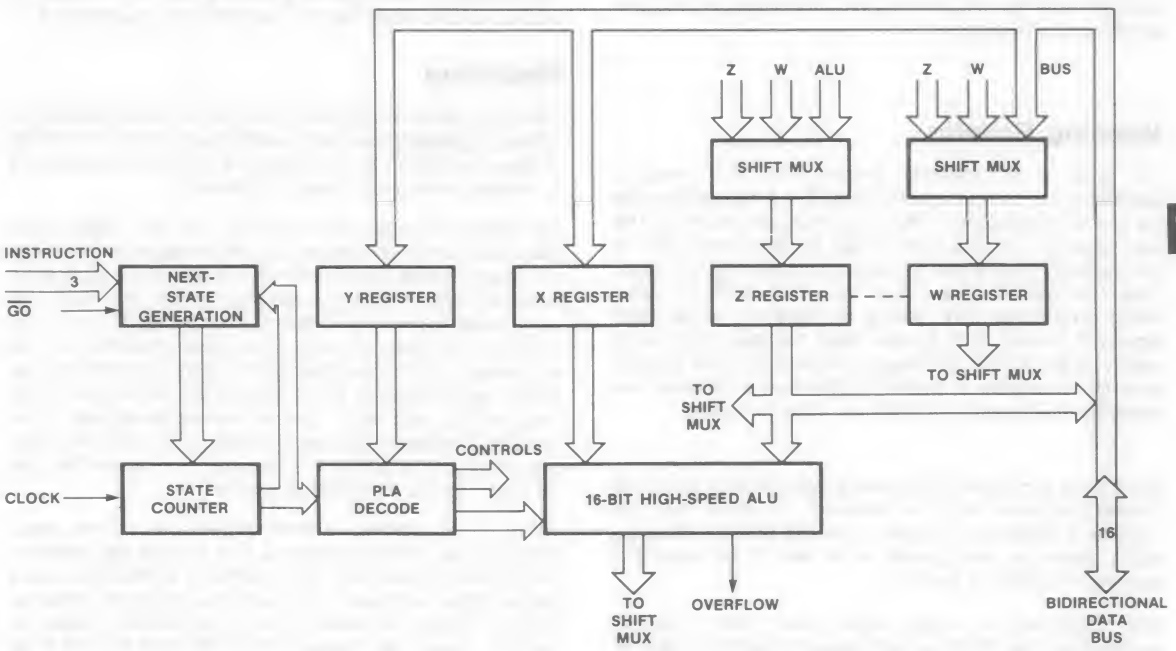


Figure 5 Internal Architecture of the 'S516

Multiplication

The 'S516 provides 2s-complement 16-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S516 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C, (A+ B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 16-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{GO}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S516 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Continual read operations at state 0 just swap the contents of register Z and W.

The 'S516 has no direct master reset input. However, initialization of the 'S516 can easily be performed by continually presenting instruction code 7, which after a maximum of 21 clock periods forces the machine back to state 0.

Integer and Fractional Arithmetic

The 'S516 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end and the least-significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{31} to $+2^{31}-1$; the operands X and Y, and single-length results, are in the range -2^{15} to $+2^{15}-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 *(negative)*. The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1}. The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-31}$ and the operands X and Y and single-length results are in the range -1 to $+1-2^{15}$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the 'S516 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S516 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The 'S516 looks at the most-significant bit of the least-significant half of the product W_{15}, and adds 1 to the most-significant half of the product at the least-significant end if W_{15} is a 1. After the operation, the 'S516 is in state 0, so that the rounded product can be read, and the W register is cleared.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S516 goes to state 0, so that a read operation can be performed, and the W register is cleared.

Overflow

The 'S516 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: $(-1)x(-1)=+1$, which cannot be held in the 'S516's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-31}$, then the overflow flipflop will be set.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-15}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^{15}.

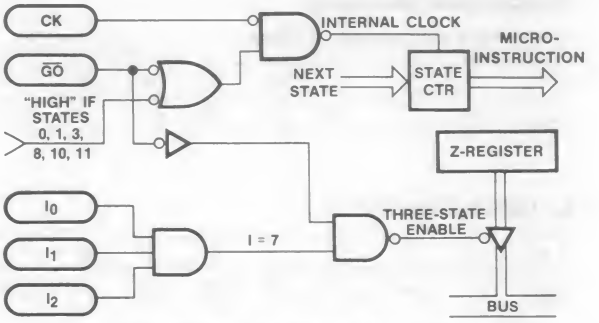


Figure 6 'S516 Internal Circuitry of "$\overline{GO}$" Line and Three-State-Enable.

During the states 0, 1, 3, 8, 10, 11, the "GO" line ($\overline{GO}$) is logic HIGH then the machine will be in a wait state until $\overline{GO}$ goes to logic LOW.

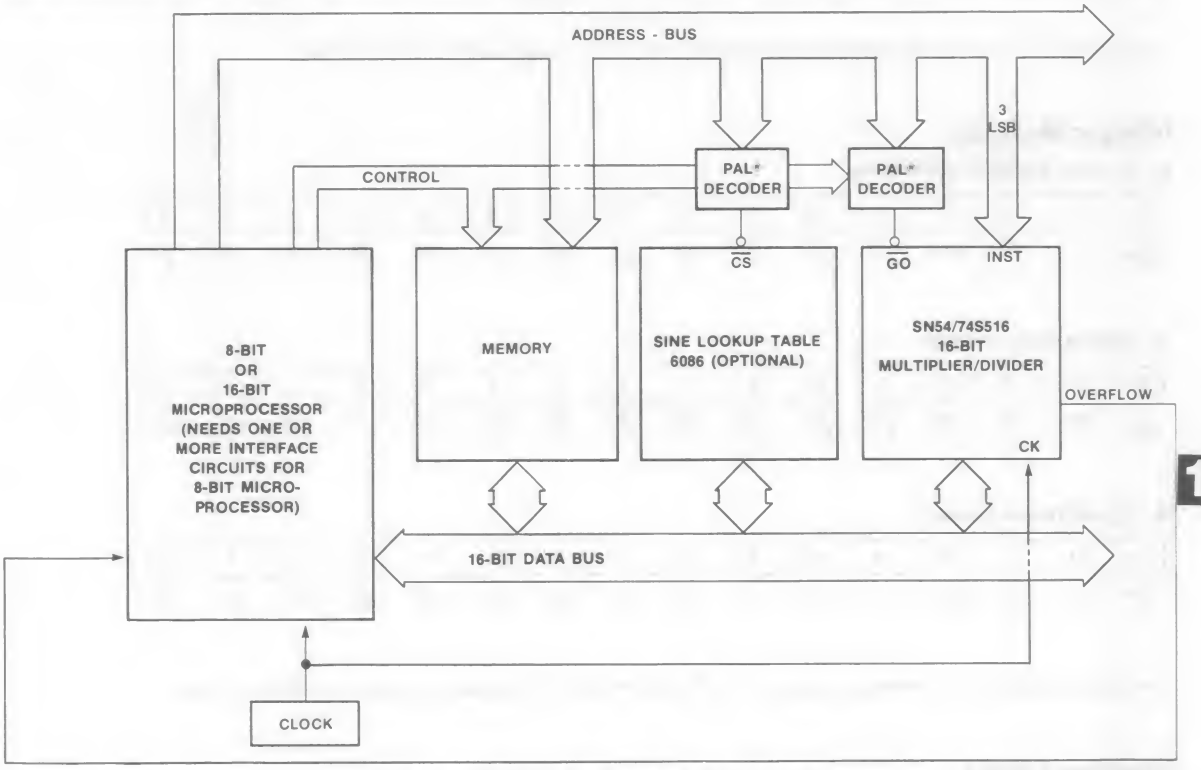


Figure 7 Interfacing the 'S516 to a Microprocessor

Figure 7 shows the block diagram of a microprocessor system with its arithmetic capabilities enhanced by the use of a 'S516 16x16 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S516 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S516 is assigned address 100; then any address in the range of 100-107 will enable the 'S516 (i.e., the $\overline{GO}$ line is LOW). Thus, if the address is 100 the 'S516 instruction is 0; if the address is 106 the 'S516 instruction is 6; and so forth.

Fractional Multiply

X_i, Y_1 - Input, Multiplicand, Multipler

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Z_i - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

W_i - LS Half Output Product*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	"0"

* The least significant bit of W_i is always a binary 0 due to normalization. Note that -1 x -1 yields an overflow in fractional multiply.

Integer Multiply

X_i, Y_1 - Input, Multiplicand, Multiplier

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Z_i - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

W_i - LS Half Output Product**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

** The least significant bit of W_i is a valid data bit. Note that $2^{-15} \times 2^{-15}$ yields $+2^{30}$ which can be represented in the output bits without overflowing.

Fraction Divide

Z_i - Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Z_i - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

W - Output Partial Remainder †

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

† Note that the partial remainder $R = 2^{-15}$ (W)

Integer Divide Example (Z, W)/X

Z_i - MSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

W_i - LSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Z_i - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

W_i - Output Partial Remainder

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125†	0		75	°C
f_{MAX}	Clock frequency	8	5			6			MHz
t_{CWP}	Positive clock pulse width	8	90			70			ns
t_{CWN}	Negative clock pulse width	8	60			50			ns
t_{BS}	Bus setup time for inputting data *	8	60			50			ns
t_{BH}	Bus hold time for inputting data *	8	45			35			ns
t_{INSS}	Instruction, $\overline{GO}$ setup time	8	10			10			ns
t_{INSH}	Instruction, $\overline{GO}$ hold time	8	30			30			ns

* During operations when the bus is being used to input data. † Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	$\overline{B_{15}}$-$\overline{B_0}$			−250	µA
			All other inputs			−1	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				250	µA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN I_{OL} = 8mA			0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN I_{OH} = −2mA		2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX V_O = 0V		−10		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	SN54S516		370	500†	mA
			SN74S516		370	450†	

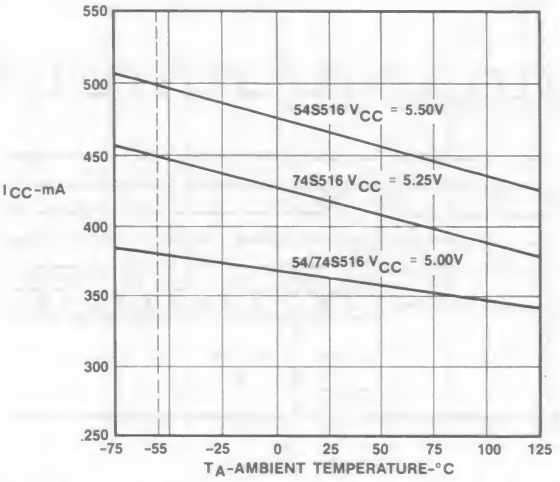
* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
†At code temperatures see the "I_{CC} vs Temperature" curves on the next page for more complete information. The typical values shown here are at 5.0V.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{BO}	Bus output delay from CK for outputting data; C_L = 30pF		8		70	120		70	95	ns
t_{PXZ}	Output disable delay	From I_2-I_0 to bus			30	70		30	65*	ns
		From $\overline{GO}$ to bus			20	50		20	40	
t_{PZX}	Output enable delay; C_L = 30pF	From I_2-I_0 to bus			55	90		55	80	ns
		From $\overline{GO}$ to bus			25	55		25	45	
t_{OVR}	Overflow output delay from CK; C_L = 30pF		8		60	120		60	95	ns

* During operations when the bus is being used to output data.

I_{CC} vs. Temperature

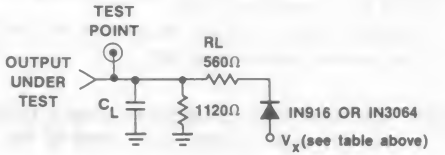


Test Waveforms

TEST	V_X*		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	t_{PHZ}	t_{PLZ}	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	t_{PZH}	t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

*At diode; see "Test Circuit" figure below.

Load Test Circuit

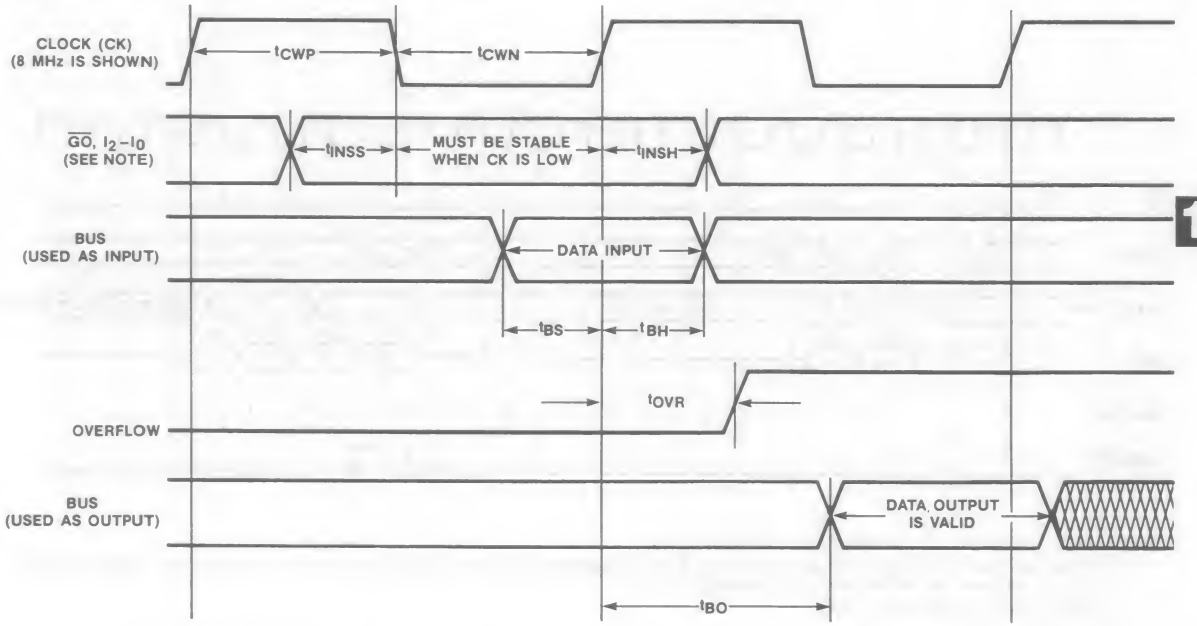


AC Test Conditions

Inputs 0V_{LOW}, 3V_{HIGH}. Rise and fall time 1-3ns from 1V to 2V. Measurements made from 1.5V_{IN} to 1.5V_{OUT}, except T_{PXZ} measured by a delta in the outputs of 0.5V from V_{OL} or V_{OH} respectively.

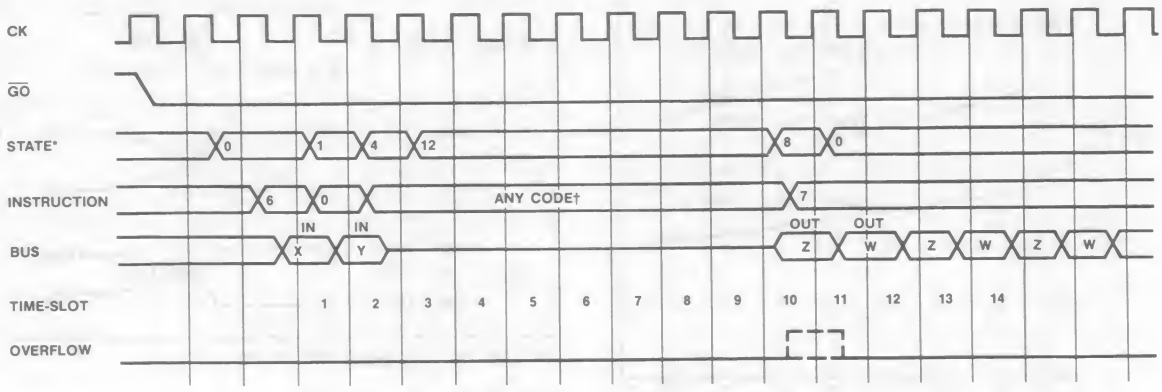
Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.



NOTE: $\overline{GO}$ and I_2-I_0 can change only when CK is high.

Figure 8 Timing Diagram of the 'S516

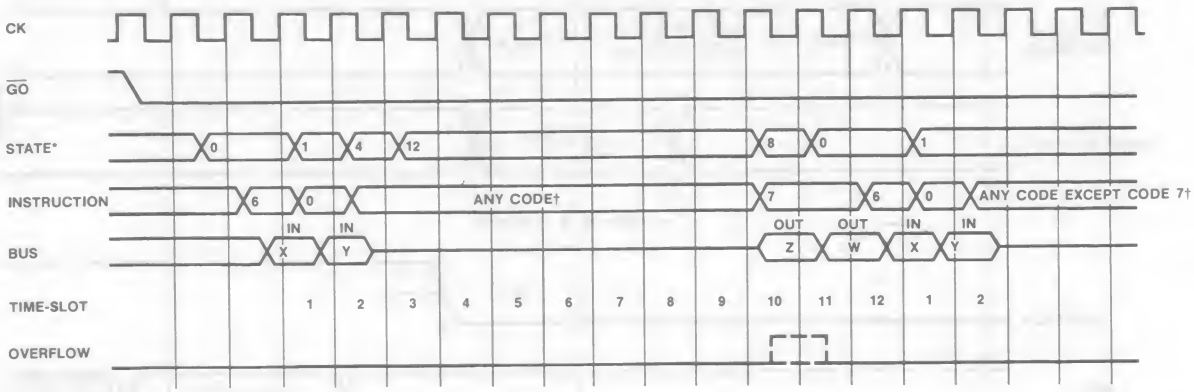


NOTES: Register Z is read at the same time that the overflow signal (if present) is set. If the instruction remains at code 7 after time-slot 11, the contents of registers Z and W are swapped each cycle.

†"Any code" means any of code 0 through code 7. However, code 6 will load a new value of X, and code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

Figure 9 Instruction Timing Example #1: Load X, Load Y, Multiply, Read Z, Read W. By presenting code 7 on the instruction lines during the last multiply cycle (state 8), the results may be read during time-slots 10 and 11.

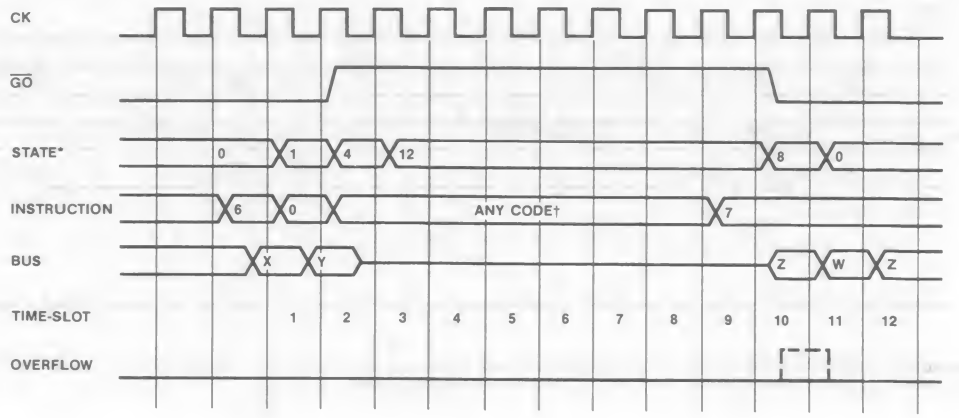


NOTES: The instruction lines may be changed only when CK is high.

†"Any code" means any of code 0 through code 7. Code 6 may be used here since a new X explicitly gets loaded for the next multiply operation. However, code 7 will cause the 'S516 to attempt to drive the data bus.

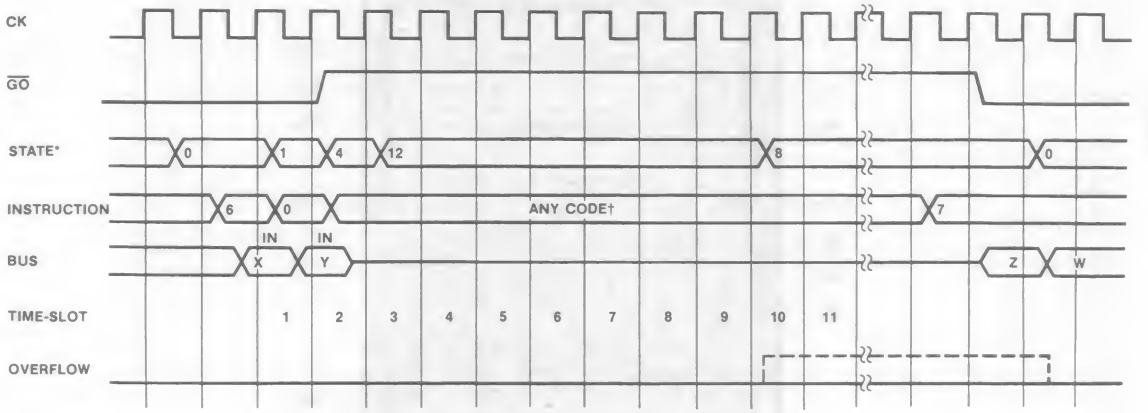
*Not available externally on the 'S516.

Figure 10 Instruction Timing Example #2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W".



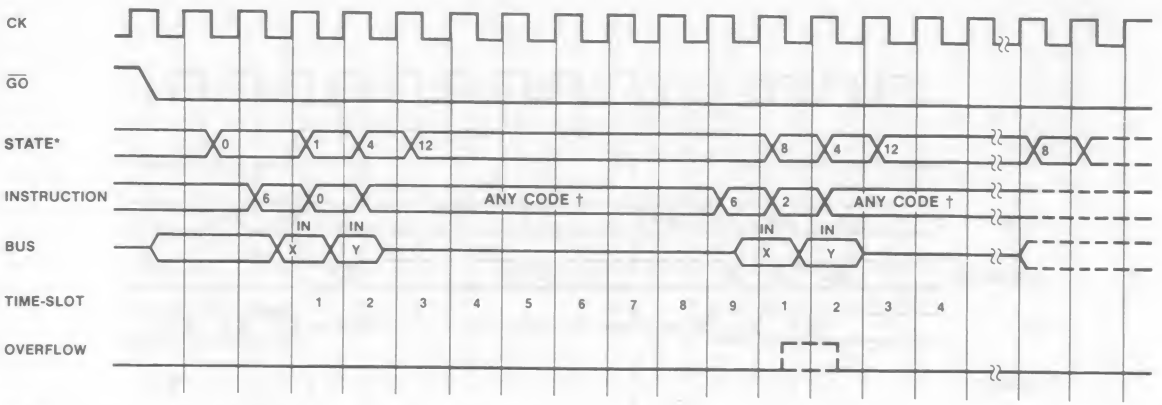
NOTES: Code 7 is given in time-slot 9, but has no effect until time-slot 10 since $\overline{GO}$ is HIGH. After $\overline{GO}$ goes LOW in time-slot 10, Z may be read.
†"Any code" means any of code 0 through code 7.
*Not available externally on the 'S516.

Figure 11 Instruction Timing Example #3: Load X, Load Y, Multiply, Read Z, Read W. This timing diagram corresponds to Table 1. Only after eight clock pulses of the operation cycle, the result is read — Z during time-slot 10 and W during time-slot 11.



NOTES: †"Any code" means any of code 0 through code 7. Code 6 or code 7 may be used here; since $\overline{GO}$ is HIGH, no new X can be loaded, and the 'S516 cannot attempt to drive the data bus.
*Not available externally on the 'S516.

Figure 12 Instruction Timing Example #4: Load X, Load Y, Multiply, Wait, Read Z, Read W.



NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example #3 for $\sum_{i=1}^{N} X_i \cdot Y_i$

†"Any code" means any of code 0 through code 7. However, code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

††Code 6 allows loading of a new X in State 12 and it takes the 'S516 State Counter to State 8. In State 8, Y is loaded via instruction 2 and the next multiply-accumulate cycle is initiated.

Figure 13 Instruction Timing Example #5: Sum of Products

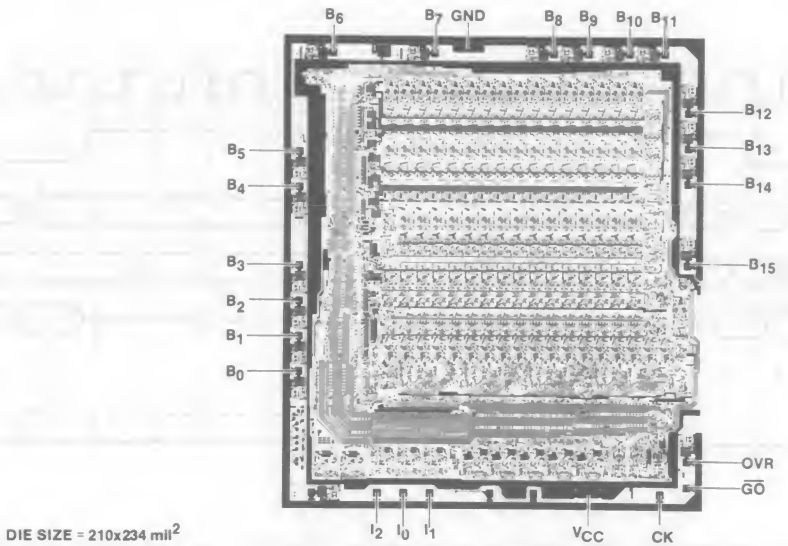


Figure 14 Metal Mask Layout of the SN54/74S516

Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X · Y (A·B)

INST 6	X ← A
INST 0	Y ← B
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST 7	MULT AND READ Z = 16 MSB OF (A·B)
INST 7	READ W = 16 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A·$\bar{C}$)

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

INST 0	Y ← C
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST X	MULT
INST 7	MULT and READ Z = 16 MSB OF (A·C)
INST 7	READ W = 16 LSB OF (A·C)

Programming Example 3

Calculating $\sum_{i=1}^{N} X_i \cdot Y_i$ (A·B + C·D + E·F + . . .)

In this case we read only after N multiplications. A new X_{i+1} is loaded during the multiplication process for X_iY_i.
Assume N = 3.
The sequence of instructions and operations for calculating $\sum_{i=1}^{3} X_i \cdot Y_i$ is: (A·B + C·D + E·F)

N = 1	INST 6	X ← A
	INST 0	Y ← B
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT } Perform A·B
	INST X	MULT
	INST X	MULT
	INST X	MULT
N = 2	INST 6	MULT and LOAD X ← C Z ← 16 MSB of (A·B) W ← 16 LSB of (A·B)
	INST 2	Y ← D
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT } Perform C·D + (K_Z, K_W)
	INST X	MULT
	INST X	MULT
	INST X	MULT
N = 3	INST 6	MULT and LOAD X ← E Z ← 16 MSB of (C·D + A·B) W ← 16 LSB of (C·D + A·B)
	INST 2	Y ← F
	INST X	MULT
	INST X	MULT
	INST X	MULT
	INST X	MULT } Perform E·F + (K_Z, K_W)
	INST X	MULT
	INST X	MULT
	INST X	MULT
READ Z	INST 7	MULT and READ Z = 16 MSB of (E·F + C·D + A·B)
READ W	INST 7	READ W = 16 LSB of (E·F + C·D + A·B)

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Programming Example 4

Multiplication plus a constant (A·B + Constant)
Assume that the constant is a 32-bit 2s-complement number.

INST 6	X ← A	
INST 6	Z ← C	LOAD 16 MSB of constant
INST 6	W ← D	LOAD 16 LSB of constant
INST 0	Y ← B	
INST X	MULT	} Perform A·B + (Z, W)
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST X	MULT	
INST 7	MULT and READ Z = 16 MSB of (A·B + (C, D))	
INST 7	READ W = 16 LSB of (A·B + (C, D))	

Programming Example 5

Dividing a 32-bit number by a 16-bit number ((B, C)/A)

INST 6	X ← A	
INST 6	Z ← B	
INST 4	W ← C	
INST X		} Perform Division $\frac{(Z, W)}{X}$
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST X		
INST 7	DIVIDE and READ the quotient $Z = \frac{(B, C)}{A}$	
INST 7	READ the remainder W of $\frac{(B, C)}{A}$	

8x8 High Speed Schottky Multipliers
SN54/74S557 SN54/74S558

Features/Benefits

- **Industry-standard 8x8 multiplier**
- **Multiplies two 8-bit numbers; gives 16-bit result**
- **Cascadable; 56x56 fully-parallel multiplication uses only 34 multipliers for the most-significant half of the product**
- **Full 8x8 multiply in 60ns worst case**
- **Three-state outputs for bus operation**
- **Transparent 16-bit latch in 'S557**
- **Plug-in compatible with original Monolithic Memories' 67558**

Description

The 'S557/'S558 is a high-speed 8x8 combinatorial multiplier which can multiply two eight-bit unsigned or signed twos-complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level the operand is treated as an unsigned eight-bit number, while if the Mode control is at a High logic level the operand is treated as an eight-bit signed twos-complement number. Additional inputs, R_S and R_U, (R, S557) allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers.

The 'S557 internally develops proper rounding for either signed or unsigned numbers by combining the rounding input R with X_M, Y_M, $\overline{X_M}$, and $\overline{Y_M}$ as follows:

$R_U = \overline{X_M} \cdot \overline{Y_M} \cdot R$ = Unsigned rounding input to 2^7 adder.

$R_S = (X_M + Y_M)\ R$ = Signed rounding input to 2^6 adder.

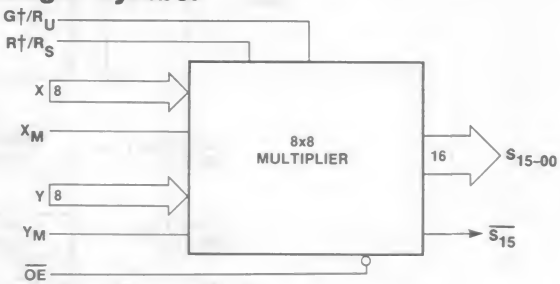
Since the 'S558 does not require the use of pin 11 for the latch enable input G, R_S and R_U are brought out separately.

The most-significant product bit is available in both true and complemented form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an assertive-low Output Enable which allows several multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

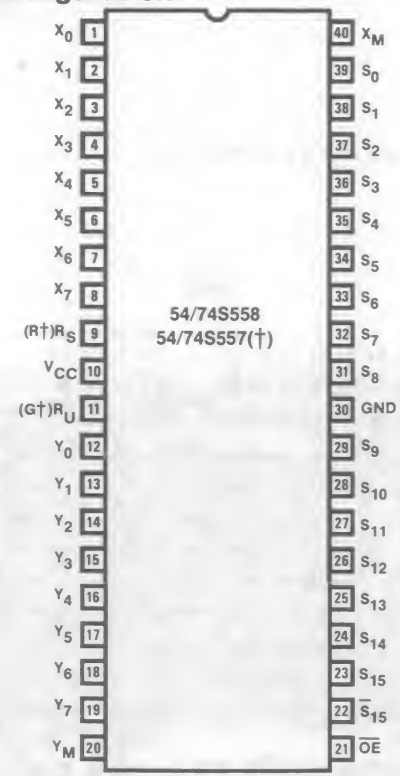
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
54S557, 54S558	J40, F42	Military
74S557, 74S558	N40, J40	Commercial

Logic Symbol



Pin Configuration



†For 54/74S557 Pin 9 is R and Pin 11 is G.

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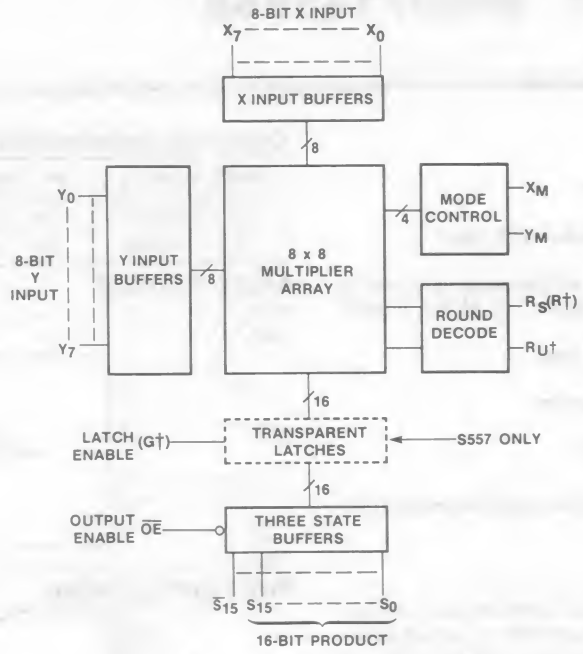
2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

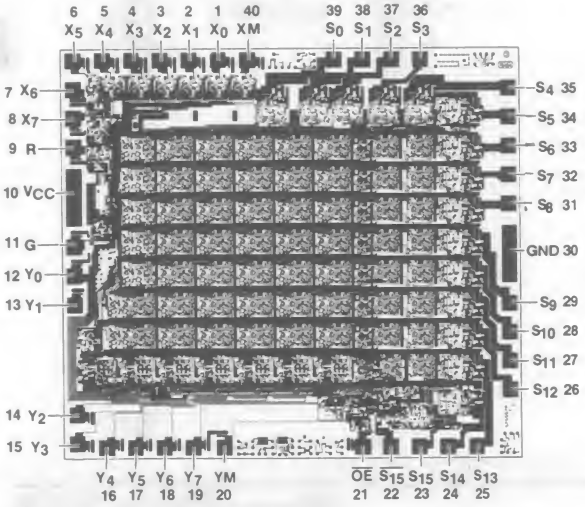
Monolithic Memories

Logic Diagram



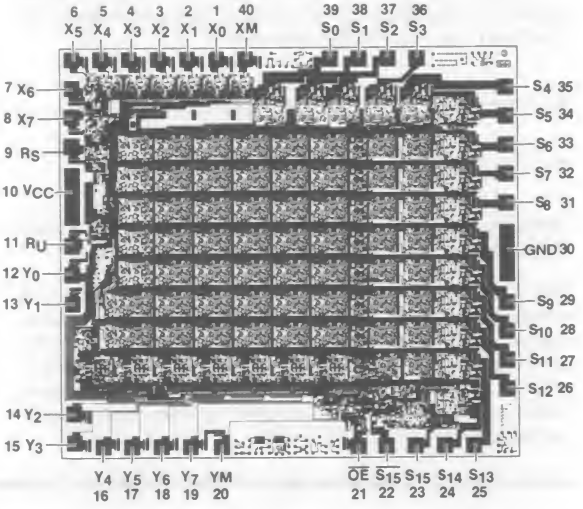
†For 54/74S557 Pin 9 is R and Pin 11 is G.

'S557



DIE SIZE: 144x130 mil

'S558



DIE SIZE: 144x130 mil

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	DEVICE	MILITARY			COMMERCIAL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	all	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	all	–55		125*	0		75	°C
t_{su}	X_i, Y_i to G set	'S557	50			40			ns
t_h	X_i, Y_i to G hold time	'S557	0			0			ns
t_w	Latch enable pulse width	'S557	20			15			ns

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			–1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			100	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = –2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			–100	μA
I_{OZH}			V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX			200	280	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	DEVICE	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PD1}	X_i, Y_i to S_{7-0}	All	C_L = 30pF R_L = 560Ω see test figures		40	60		40	50	ns
t_{PD2}	X_i, Y_i to S_{15-8}	All			45	70		45	60	ns
t_{PD3}	X_i, Y_i to $\overline{S}_{15}$	All			50	75		50	65	ns
t_{PD4}	G to S_i	'S557			20	40		20	35	ns
t_{PXZ}	$\overline{OE}$ to S_i	All			20	40		20	30	ns
t_{PZX}	$\overline{OE}$ to S_i	All			15	40		15	30	ns

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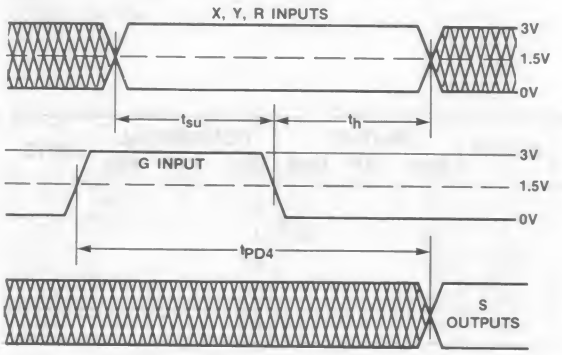
Timing Waveforms

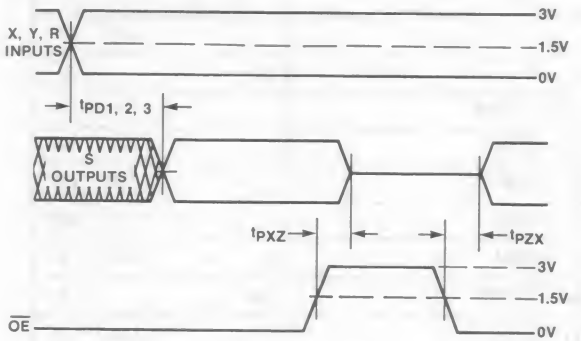
Setup and Hold Times ('S557)



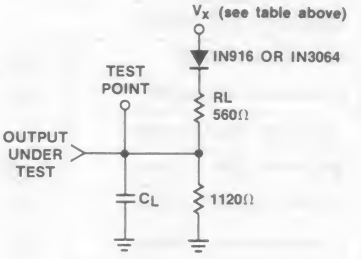
Test Waveforms

TEST	V_X		OUTPUT WAVEFORM — MEAS. LEVEL
All t_{PD}	5.0V		V_{OH}, V_{OL}, 1.5V
t_{PXZ}	for t_{PHZ}	for t_{PLZ}	V_{OH}, 0.5V, 0.5V, V_{OL}, 2.8V, 0.0V
	0.0V	5.0V	
t_{PZX}	for t_{PZH}	for t_{PZL}	2.8V, 0.0V, 1.5V, V_{OH}, V_{OL}
	0.0V	5.0V	

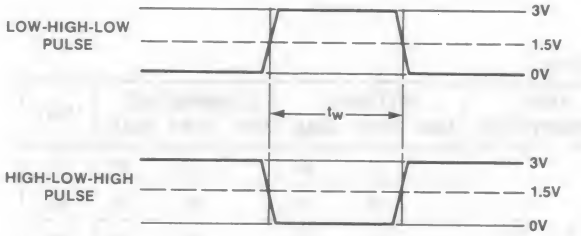
Propagation Delay



Load Test Circuit



Latch Enable Pulse Width ('S557)



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

SUMMARY OF SIGNALS/PINS	
X_7-X_0	Multiplicand 8-bit data inputs
Y_7-Y_0	Multiplier 8-bit data inputs
X_M, Y_M	Mode control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{15}-S_0	Product 16-bit output
$\overline{S}_{15}$	Inverted MSB for expansion
R_S, R_U	Rounding inputs for signed and unsigned data, respectively ('S558 only)
G	Transparent latch enable ('S557 only)
$\overline{OE}$	Three-state enable for S_{15}-S_0 and $\overline{S}_{15}$ outputs
R	Rounding input for signed or unsigned data; combined internally with X_M, Y_M ('S557 only)

ROUNDING INPUTS
'S557

INPUTS			ADDS	
X_M	Y_M	R	2^7	2^6
L	L	H	YES	NO
L	H	H	NO	YES
H	L	H	NO	YES
H	H	H	NO	YES
X	X	L	NO	NO

'S558

INPUTS		ADDS		USUALLY USED WITH	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	NO	NO	X	X
L	H	NO	YES	H†	H†
H	L	YES	NO	L	L
H	H	YES	YES	*	*

†In mixed mode, one of these could be Low but not both.
*Usually a nonsense operation. See applications section of data sheet.

74S557 FUNCTION TABLE

INPUTS		PRODUCT RESULT FROM ARRAY	LATCH CONTENTS (INTERNAL TO PART)	OUTPUTS	FUNCTION
$\overline{OE}$	G	T_i	Q_i	S_i	
L	L	X	L	L	Latched
L	L	X	H	H	
L	H	L	(L)*	L	Transparent
L	H	H	(H)*	H	
H	L	X	(L)	Z	Hi-Z; Latched Data not Changed
H	L	X	(H)	Z	
H	H	X	(X)*	Z	Hi-Z

*Identical with product result passing through latch.

MODE CONTROL INPUTS

OPERATING MODE	INPUT DATA		MODE CONTROL INPUTS	
	X_7-X_0	Y_7-Y_0	X_M	Y_M
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

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Functional Description

The 'S557 and 'S558 multipliers are 8x8 combinatorial logic arrays capable of multiplying numbers in unsigned, signed twos-complement, or mixed notation. Each eight-bit input operand X and Y has associated with it a mode control which determines whether the array treats this number as signed or unsigned. If the mode control is at a High logic level, then the operand is treated as a twos-complement number with the most-significant bit having a negative weight; while, if the mode control is at a Low logic level, then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most-significant product bit is available in both true and complemented form. This allows an adder to be used as a subtractor in many applications and eliminates the need for certain SSI circuits.

Two additional inputs to the array, R_S and R_U, allow the addition of a bit at the appropriate bit position so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers. In the 'S557, these two inputs are generated internally from the mode controls and a single R input.

The product outputs of the multiplier are controlled by an assertive-low $\overline{\text{Output Enable}}$ control. When this control is at a Low logic level the multiplier outputs are active, while if the control is at a High logic level then the outputs are placed in a high-impedance state. This three-state capability allows several multipliers to drive a common bus, and also allows pipelining of multiplication for higher-speed systems.

Rounding

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in an n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

$$\left.\begin{array}{l} 39.2 \rightarrow 39 \\ 39.6 \rightarrow 39 \end{array}\right\} \text{ Truncating}$$

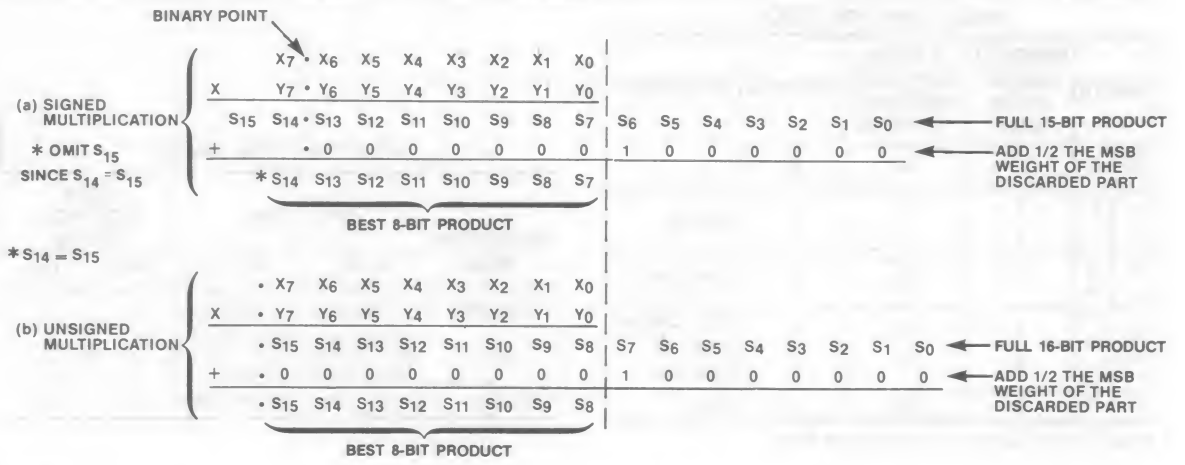
$$\left.\begin{array}{l} 39.2 + 0.5 = 39.7 \rightarrow 39 \\ 39.6 + 0.5 = 40.1 \rightarrow 40 \end{array}\right\} \text{ Rounding}$$

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

$$39.28 + 0.05 = 39.33 \rightarrow 39.3$$

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are -1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the S_7 weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 'S558 multiplier has two rounding inputs, R_S and R_U. Thus, to get a rounded single-length result, the appropriate R input is tied to V_{CC} (logic High) and the other R input is grounded. If a double-length result is desired, both R inputs are grounded for the 'S558, and the single R input is grounded for the 'S557.

†In general: multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.



NOTES:

(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S_{14} through S_7, and rounding is performed by adding "1" to bit position S_6.

(b) In unsigned notation the best 8-bit product is the most significant half of the product and is corrected by adding "1" to bit position S_7.

Figure 1. Rounding the Result of Binary Fractional Multiplication.

Signed Expansion

The most-significant product bit has both true and complement outputs available. When building larger signed multipliers, the partial products (except at the lower stages) are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complemented form of the most-significant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the carry from the previous adder stage plus the addition of the two negative most-significant partial-product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$S = A \oplus B \oplus C$

$C_{OUT} = AB + BC + CA$

where C is the carry-in and A and B are the sign bits of the two partial products.

Now an adder produces the equations:

$S = A \oplus B \oplus C$

$C_{OUT} = AB + BC + CA$

Examining these equations, it can be seen that, if the inversions of A and B are used, then the most significant sum bit of the adder is the sign extension bit.

Sign ext = $AB + B\overline{C} + \overline{C}A = \overline{\overline{A}\overline{B} + \overline{B}C + C\overline{A}}$,

and the sum remains the same.

16x16 Twos-Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X_7-X_0 and X_{15}-X_8), and so is the Y operand. Since the situation is that of a cross-product, four partial products are generated as follows:

$A = X_L * Y_L$

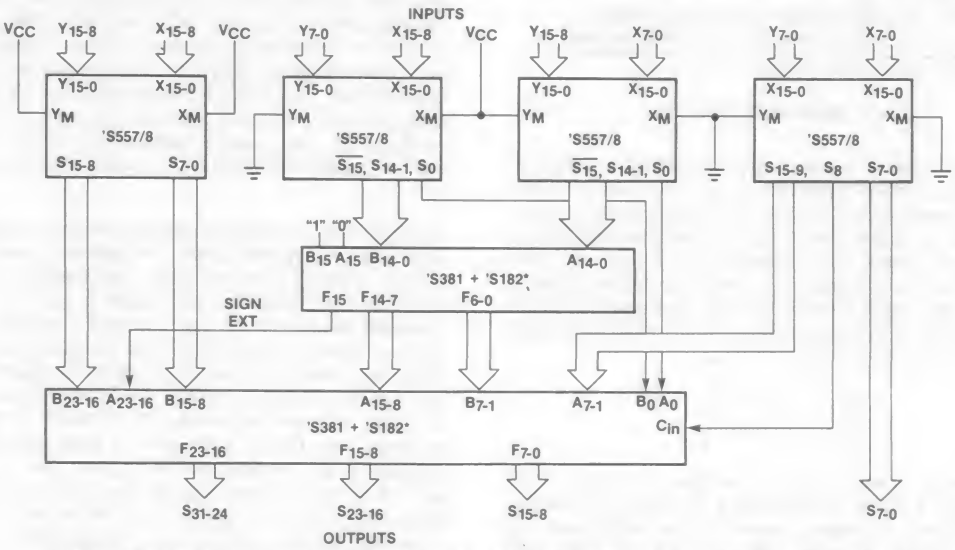
$B = X_L * Y_H$

$C = X_H * Y_L$

$D = X_H * Y_H$

where the subscript L stands for bits 7-0, ("low or least-significant half), and the subscript H stands for bits 15-8.

Expanded twos-complement multiplication requires a sign extension of the B and C partial products. Thus, B_{15} and C_{15} need to be extended eight positions to the left (to align with D_{15}). In this approach two more adders are required. But the complement of the MSB ($\overline{S}_{15}$) on the 'S558 can be used to save these two adders. Figure 2 shows the implementation of 16x16 signed twos-complement multiplication in this manner.



* THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH SPEED ADD OPERATION. THE 'S182 IA A LOOK-AHEAD CARRY GENERATOR AND IT REDUCES THE PROPAGATION DELAY. ALL THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 60+44+64 = 168 nsec

Figure 2. 16x16 Twos-Complement Signed Multiplication.

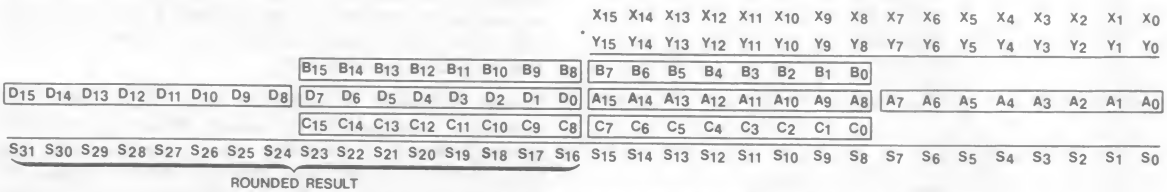


Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication.

Applications: How to Design Superspeed Cray Multipliers with '558s

by Chuck Hastings

Multiplication, as most of us think of it, is performed by repeated addition and shifting. When we multiply using pencil and paper, according to the familiar elementary-school method, we first write down the multiplicand, and then write down the multiplier immediately under it and underline the multiplier. Then we take the least-significant digit of the multiplier, multiply that digit by the entire multiplicand, and record the answer in the top row of our workspace, underneath the line. Then we repeat, using now the second-least-significant multiplier digit, and record that answer below the first one, pushed one digit position (that is, "shifted") to the left. This process continues until we run out of multiplier digits (or out of patience), at which point we add up the constants of the whole diamond-shaped workspace and record at the bottom an answer which consists of either m + n - 1 digits or m + n digits, where there are m digits in the multiplier and n digits in the multiplicand. An example, voila':

```
  125  (multiplicand)
 x107  (multiplier)
  875  (7 x 125)
  000  (0 x 125, shifted left one digit position)
125    (1 x 125, shifted left two digit positions)
-----
13375  (sum of the above)
```

Figure 4. Decimal Multiplication

The decimal number system has no monopoly on truth — our ancestors simply happened to have ten fingers at the time when someone came up with the idea of counting. Binary numbers, as you know, are more copacetic than are decimal numbers with digital-logic elements, which like to settle comfortably into one voltage state ("High) or another ("Low"), rather than into one of ten different states. So we can repeat the above example using binary numbers, right? First, we convert our multiplicand and multiplier to binary:

$$125_{10} = 01111101_2$$
$$107_{10} = 01101011_2$$

The subscripts 10 and 2 refer to the "base" or "radix" of the number system, 10 for decimal and 2 for binary. (Remember your New Math?) For sneaky reasons to be revealed soon, I've used 8-bit binary numbers, which is one bit more than necessary for my example, and added a leading zero. So, we multiply:

```
  01111101(2) = 125(10)
x 01101011(2) = 107(10)
----------
  01111101
 01111101
00000000
 01111101
00000000
 01111101
 01111101
00000000
----------------
0011010000111111 = 13375(10)
```

Figure 5. Binary Multiplication

I've left off the remarks this time, but they're just like the remarks in the decimal example, at least in principle. Just in case you doubt this answer, I'll convert it back:

```
1      1
1      2
1      4
1      8
1     16
1     32
0      0      (  64)
0      0      (  128)
0      0      (  256)
0      0      (  512)
1   1024
0      0      ( 2048)
1   4096
1   8192
0      0      (16384)
0      0      (32768)
-----
13375
```

Figure 6. Binary-to-Decimal Conversion

Now look carefully at the diamond-shaped array of numbers in the workspace in Figure 5. Each row is either the multiplicand 01111101, or else all zeroes. The 01111101 rows correspond to "1" digits in the multiplier, and the all-zero rows to "0" digits in the multiplier. Life does get simpler in some ways when we switch to binary numbers: "multiplying a multiplier digit by the multiplicand" now means just gating a copy of the multiplicand into that position if the digit is "1," and not doing so if the digit is "0."

Seymour Cray, the master computer designer from Chippewa Falls, Wisconsin whose career has spanned three companies (Univac, Control Data, and now Cray Research) and many inventions, first observed some time in the late 1950s that *computers* also could actually multiply this way, if one merely provided enough components. This last qualifying remark; in those days when even transistors, let alone integrated circuits, in computers were still a novelty was by no means a trivial one! To prove his point (and satisfy a government contract), Cray designed, and Control Data built, a 48x48 multiplier which operated in one microsecond, about 1960. This multiplier was part of a special-purpose array processor for a classified application, and was so big that a CDC 1604 (then considered a large-scale processor) served as its input/output controller. In principle, such a multiplier at that time would have had to consist of 48 48-bit full adders or "mills," each of which received one input 48-bit number from the outputs of the mill immediately above it in the array, and the other 48-bit number from a gate which either allowed the multiplicand to pass through, or else supplied an all-zero 48-bit number. Actually, these mills have to be somewhat *longer* than 48 bits. Anyway, that is at least 2304 full adders, and in 1960 a full-adder circuit normally occupied one small plug-in circuit card.

A later version of this multiplier, in the CDC 7600 super-computer, could produce one 48x48 product out every 275 nanoseconds on a pipelined basis. The pipelining was asynchronous, and the entire humungus array of adders and gating logic could have up to three different products rippling down it at a given instant!

Back to the 1980s. Monolithic Memories has for several years produced an 8x8 Cray multiplier, the 57/67558, as a single 600-mil 40-pin DIP. After we invented this part, AMD second-sourced it, and by now it has become an industry standard. We now also have faster pin-compatible parts, the 54/74S558 and 'S557. Like other West Coast companies 2,000 miles from Wisconsin and Minnesota where Seymour Cray does his inventing, Monolithic Memories has generally used the term "combinatorial multiplier" instead of "Cray multiplier" for this type of part. However, "combinatorial multiplier" has nine extra letters and five extra syllables, and also inadvertently implies that the technique involves combinatorial logic rather than arithmetic circuits. Some West Coast designs, including our 67558, use a modified internal array with only half as many full-adder circuits and slightly different interconnections, based on the two-bit "Booth-multiplication" algorithm (see reference 1), plus the "Wallace-tree" or "carry-save adder" technique (see references 2 and 3). Conceptually, however, the entire chip or system continues to operate as a Cray multiplier.

The '558, in particular can be thought of as a static logic network which fits exactly the binary multiplication example of Figure 5. (See now why I insisted on using 8-bit binary numbers?) There are no flipflops or latches whatever in the '558 — it is a "flow-through" device. Its 40 pins are used up as follows:

Use of Pins	Input, Output, or Voltage	Number of Pins
Multiplier	I	8
Multiplicand	I	8
Double-Length Product	O	16
Complement of Most-Significant Bit of Double-Length Product	O	1
3-State Output Enable	I	1
8-Bit-Input Number-Interpretation-Mode Control	I	2
Rounding Control for Product	I	2
Power and Ground	V	2
		40

Table 1. Use of Pins in the '558

The two number-interpretation-mode control pins, one for the multiplier and one for the multiplicand, allow the format for each of these two 8-bit input numbers to be chosen independently, as follows:

Control Input	Interpretation of 8-bit Input Number
L	8-bit unsigned
H	7-bit plus a sign bit

Table 2. Mode Control Input Encoding

The two rounding control pins allow either integer (right-justified) or fractional (left-justified) interpretation of the 14-bits-plus-sign double-length product of two 7-bits-plus-sign numbers for internal rounding of the double-length result to the most accurate 8-bit number. The control encoding is:

R_S Input	R_U Input	Effect
L	L	Disable Rounding
L	H	Round Unsigned
H	L	Round Signed
H	H	Nonsense (see below)

Table 3. Rounding Control Input Encoding

Rounding is normally disabled if the entire 16-bit double-length product output is to be used. If only an 8-bit subset of this product is to be used, this subset can be either bits 15-8 for unsigned rounding as shown in Figure 7, or bits 14-7 for signed rounding as shown in Figure 8. In either case, a "1" is forced into the '558's internal adder network at the bit position indicated by the arrow; adding a "1" into the bit position *below* the least-significant bit of the final answer has the effect of rounding, as you can see after a little thought. Obviously, forcing a "1" into *both* of these adder positions at the same time is a nonsense operation for most applications — it adds a "3" into the middle of the double-length result.

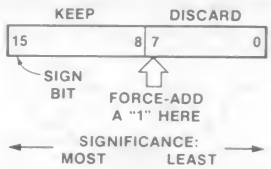


Figure 7. Unsigned Rounding

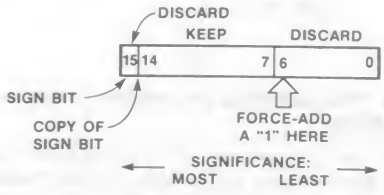


Figure 8. Signed Rounding

By now you probably have a fairly good idea of what a '558 is, and would like a few hints as to how to use it, right? First of all, there is an occasional application in things like video games for *very* fast multiplication, either 8x8 or 16x16, controlled by an 8-bit microprocessor, where there would be one '558 per system (see reference 4). More typically, however, the '558 is a building block, and several of them are used within one system; in fact, maybe more than several — "many." In the usual Silicon-Valley jargon, we can *cascade* a number of '558 (8x8) Cray-multiplier chips to create larger Cray multipliers at the systems level.

For the sake of concreteness, I'll discuss the case of 56x56 multipliers, which are appropriate in floating-point units which deal with "IBM-long-format" numbers which have a 56-bit mantissa. Any computer which emulates, or uses the same floating-point format as, any of the following computers can use such a multiplier:

IBM 360/370
Amdahl 470
Data General Eclipse
Gould/System Engineering SEL 32
Norsk Data 500 (different format)

There are two basic approaches: serial-parallel, and fully parallel. The serial-parallel approach uses seven '558s, and requires seven fully multiply-and-add cycles. On the first cycle, the least-significant eight bits of the multiplier are multiplied by the entire multiplicand, and this partial product is saved. On the second cycle, the next-least significant eight bits of the multiplier are multiplied by the multiplicand, and that product (shifted eight bit positions to the left) is added into the first partial product to form the new partial product. And so forth, for five more cycles. It's almost like our decimal-multiplication example of Figure 1, except that instead of base-10 decimal digits we now have base-256 superdigits.

The fully-parallel approach totally applies Cray's usual design philosophy (sometimes characterized as "big, fast, and simple") at the systems level. It uses 49 '558s, in seven ranks; the 'i'th rank performs an operation corresponding to that done during the 'i'th cycle in the serial-parallel implementation. A complete mill is used to add the outputs of one rank of '558s to those of the rank above it. Or, alternatively, these mills can be laid out in a "tree" arrangement, such as:

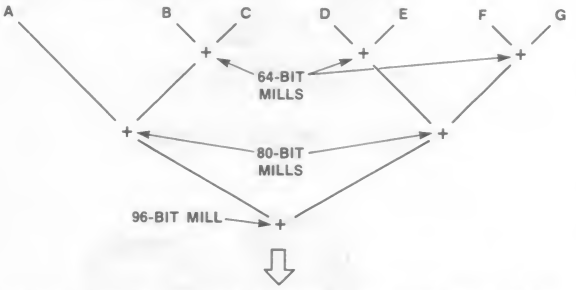


Figure 9. "Tree" Summing Arrangement of Mills for a 56x56 Cray Multiplier

Each letter stands for one rank of '558s, and each "+" stands for a mill of the indicated length. More involved "Wallace-tree" techniques are usually preferable. (See reference 3). If the least-significant half of the double-length product is *never* needed, only 34 'S558s are required. There is one subtlety which needs to be mentioned. If, conceptually, a '558 looks like a diamond —

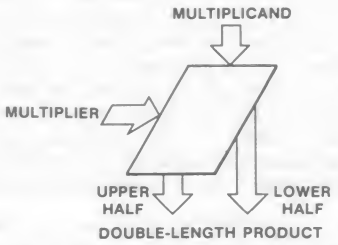


Figure 10. A Single '558 in "Diamond" Notation

then, the 8x56 multiplier for the serial-parallel configuration (which is also one rank of the fully-parallel configuration, which has seven such ranks) looks like this:

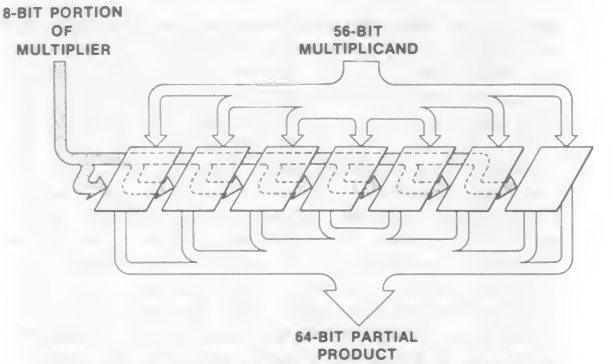


Figure 11. 8x56 Cray Multiplier in "Diamond" Notation

As you may discover after a moment's thought, *each* slanted double line in Figure 8 calls for addition of the outputs of *two* '558s — the eight most significant bits of one, and the eight least-significant bits of the next one to the left. There must also be an extra adder (or at least a "half adder") to propagate the carries from this addition all the way over to the left end of the result. The upshot is that an extra 56-bit mill is needed, in addition to the '558s. The eight least-significant bits of the least-significant '558 do not have to go through this mill, since they do not get added to anything else.

One final note: building up a large Cray-multiplier configuration out of '558s requires a *lot* of full adders, or else a lot of something else equivalent to them. Monolithic Memories also makes the 54/74S381 (a 4-bit "ALU" or "*A*rithmetic *L*ogic *U*nit") and the 54/74S182 (a carry-bypass circuit which works well with the '381); and two faster ALUs, the 54/74S381A and the 54/74S382A, are in design. These ALUs and bypasses are excellent building blocks from which to assemble the mills used for summation within a rank of '558s, and also the mills used for tree-summation of the outputs of all ranks. For how to put together one of these mills using '381s, '382s, and '182s, see reference 1. For how to use PROMs as Wallace trees, see reference 3.

Now you can go ahead, design your Cray multiplier out of '558s, and start multiplying full-length numbers together in a fraction of a microsecond. Sound like fun?

References

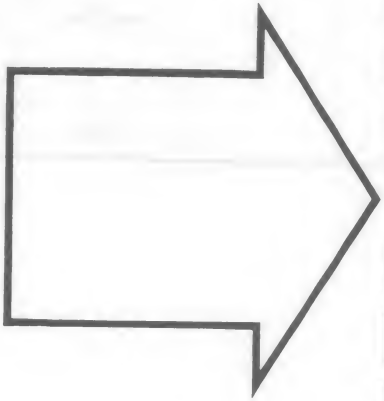
1. "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, *Proceedings of the Sixth West Coast Computer Faire*, San Francisco, California, April 3-5, 1981; pages 492-510.

2. "Real-Time Processing Gains Ground with Fast Digital Multiplier," Shlomo Waser and Allen Peterson, *Electronics*, September 29, 1977.

3. "Big, Fast and Simple — Algorithms, Architecture, and Components for High-End Superminis," Ehud "Udi" Gordon and Chuck Hastings, 1982 *Southcon Professional Program*, Orlando, Florida, March 23-25, 1982, paper no. 21/3.

4. "An 8x8 Multiplier and 8-bit μP Perform 16x16-bit Multiplication," Shai Mor, *EDN*, November 5, 1979.

NOTE: All of these references are available as application notes from Monolithic Memories.



8-Bit Interface

Part Number		Function	Power	Polarity	Feature
Commercial	Military				
SN74LS241	SN54LS241	Buffer	LS	Non-invert	—
SN74LS244	SN54LS244				—
SN74LS341	SN54LS341				Schmitt Trigger
SN74LS344	SN54LS344				Schmitt Trigger
SN74LS210	SN54LS210			Invert	—
SN74LS240	SN54LS240				—
SN74LS310	SN54LS310				Schmitt Trigger
SN74LS340	SN54LS340				Schmitt Trigger
SN74S241	SN54S241		S	Non-invert	—
SN74S244	SN54S244				—
SN74S731	SN54S731				MOS Driver
SN74S734	SN54S734				MOS Driver
SN74S210	SN54S210			Invert	—
SN74S240	SN54S240				—
SN74S700	SN54S700				MOS Driver
SN74S730	SN54S730				MOS Driver
SN74LS245	SN54LS245	Transceiver	LS	Non-invert	—
SN74LS645	SN54LS645				—
SN74LS645-1	—				48mA I_{OL}
SN74LS373	SN54LS373	Latch		Non-invert	—
SN74LS793	SN54LS793				Read Back
SN74LS533	SN54LS533			Invert	—
SN74S373	SN54S373		S	Non-invert	—
SN74S531	—				32mA I_{OL}
SN74S533	SN54S533			Invert	—
SN74S535	—				32mA I_{OL}
SN74LS273	SN54LS273	Register	LS	Non-invert	Master Reset
SN74LS374	SN54LS374				—
SN74LS377	SN54LS377				Clock Enable
SN74LS534	SN54LS534			Invert	—
SN74LS794	SN54LS794			Non-invert	Read Back
SN74S273	SN54S273		S		Master Reset
SN74S374	SN54S374				—
SN74S377	SN54S377				Clock Enable
SN74S383	SN54S383				Open Collector
SN74S532	—				32mA I_{OL}
SN74S534	SN54S534			Invert	—
SN74S536	—				32mA I_{OL}

Pick the Right 8-Bit – or 16-Bit – Interface Part for the Job

Chuck Hastings and Bernard Brafman

Introduction

A few years ago, 20-pin 8-bit buffers, registers, latches, and transceivers came into existence as a rather haphazard upwards evolution from the MSI devices available in the mid-1970s. As time went on, usage of these parts increased until they became one of the fundamental computer-system building-block "primitives"—the "glue" which holds the entire system together. System designers demanded, and semiconductor manufacturers provided, many refinements such as inverting outputs to reduce parts count in assertive-low-bus systems, high-drive outputs to rescue designs with overloaded buses, Schmitt-trigger inputs to likewise rescue designs troubled with severe bus noise, high-voltage outputs specifically suited for driving MOS inputs, series-resistor outputs for driving highly capacitative loads such as dynamic-MOS address buses, and so forth.

Today the demands are to reduce component costs and system board area. Reducing parts count achieves both of these objectives at one stroke. With the development of the 300-mil 24-pin SKINNYDIP™ package, it is now possible to effectively incorporate the equivalent of two 20-pin 8-bit interface parts into one 24-pin "16-bit interface" part. The approach is to look for common configurations of pairs of 8-bit parts, and implement the pair as a single chip. Common configurations include back-to-back "registered transceivers," with the same options already available in the 20-pin 8-bit parts, and pipeline registers.

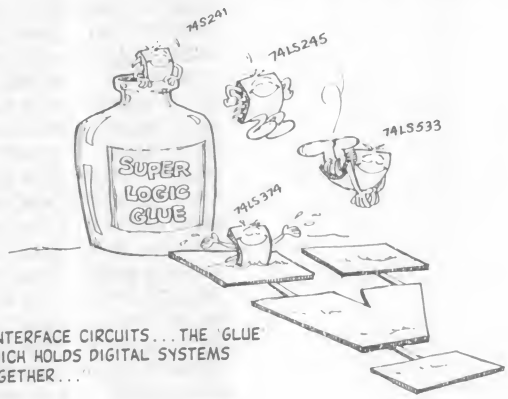
Interface Basics

Where Do Interface Circuits Fit In?

Interface circuits appear as unglamorous bread-and-butter commodity items, as compared to many of the other more complex integrated circuits of today: their sales volume is very high, their average selling price is comparatively low, and essentially interchangeable parts are offered by several suppliers. They have the humble role of being the "glue" which holds digital systems together; they are *means* rather than ends in themselves.

When preliminary system block diagrams turn into detailed schematics, the *blocks* turn into complex circuits—microprocessors, multipliers/dividers, automatic dynamic-MOSRAM refresh controllers, high-speed FIFOs, programmable-logic circuits, arithmetic-logic units, and so forth. But then, however, the *lines* between those blocks turn into interface circuits, which must be there in the final design but never explicitly get noticed during the conceptual-design stage!

The term "interface" is actually a bit of a misnomer, since it implies that these parts always occur at a boundary between two somewhat different types of logic. That may have been true once, and it is still true that many of the circuits commonly called "interface" have inputs and/or outputs which are different electrically from those of, say, triple three-input NAND gates produced using the identical solid-state-circuit technologies. But a general working definition of "interface circuits" also has to cover some other parts which get used in similar system roles, but have normal inputs and normal totem-pole or three-state outputs. One such definition, current today at Monolithic Memories, is



"INTERFACE CIRCUITS... THE 'GLUE' WHICH HOLDS DIGITAL SYSTEMS TOGETHER..."

"... ultra-high performance integrated circuits which do not lend themselves to higher levels of integration, due either to their parallel data structure or to the electrical properties of their inputs and/or outputs."

Interface circuits get used wherever data must be held, transmitted on demand, power-amplified, level-shifted, read from a noisy bus, inverted, or otherwise operated upon in some simple electrical way. If more complex transformations of the data are called for, of a predominantly mathematical rather than electrical nature, the designer will typically try to perform the required operations with readymade LSI or MSI circuits. Even here, of course, interface circuits often have the inconspicuous but crucial role of performing format conversion so that several LSI circuits can communicate with each other. Still, they are viewed as "overhead," which system designers try to minimize and semiconductor producers often rank well below their top level of corporate priorities.

But interface circuits are here to stay, at least for several more years. And the realization is growing among both users and producers of semiconductors that, since interface parts are not about to vanish soon, they need to be treated as something more than afterthoughts to the design process. Users who select interface circuits shrewdly are achieving real gains in system performance and reliability, and significant reductions in system size, weight, and power consumption. Producers who do a conscientious and professional job of developing and marketing these humble parts are finding increased demand for their wares, even during recessions.

Two major trends currently evident in the world of interface circuits are:

- **The emergence of an orderly, matrix-like approach to interface products, so that taken all together they form an *array* rather than simply a splendid jumble of assorted types.**
- **A strong emphasis on increasing the number of data bits which can be handled or accomodated by a single interface-circuit package.**

This paper will discuss each of these trends in some detail, and will then go on to present some realistic interface applications based on several actual designs.

What Kinds of Interface Circuits Are There?

Commonly, the label "interface circuit" is applied to any of a diverse collection of miscellaneous devices which don't seem to fit into any other classification. As the term is used here, however, it means either one of three basic 8-bit types—buffers, latches, and registers—which are *simple* interface circuits, or else one of several 16-bit *compound* interface circuit types such as transceivers and pipelines.

Buffers merely "pass" or transmit information at increased power levels.Most contemporary buffer circuits, including 20-pin 8-bit buffers, also have an electronically-selectable electrical-isolation capability. Such a *three-state* buffer has a type of output which can be switched into a "hi-Z" (high-impedance) state in which it does not drive, nor appreciably load, the circuit node to which it is attached.

True or *noninverting* buffers pass the input information along with the same polarity (i.e., conventions in the representation of ones and zeroes by high and low voltages) that it had when it was received. *Inverting* buffers reverse the polarity of the input information from what was received, complementing all ones to zeroes and all zeroes to ones.

Most buffers feature standard PNP inputs. However, the 'LS340/341/344/310 buffers feature Schmitt-trigger inputs, with a guaranteed 400-millivolt deadband (typically 800 millivolts) centered about the switching threshold voltage. (This notation is shorthand for "SN54/74LS340, SN54/74LS341, SN54/74LS344, SN54/74LS310," and will be used frequently hereafter.) These Schmitt-trigger buffers won't respond to input noise pulses which would make buffers with normal inputs start to switch, as long as the noise pulses do not completely cross the deadband; thus noise immunity is improved.

"...THE 'LS340/341/344/310 BUFFERS FEATURE SCHMITT-TRIGGER INPUTS WITH A GUARANTEED... DEADBAND..."

Latches and *registers* have the same basic capability as buffers, but also have the additional capability that they retain stored information as long as power is supplied to them. Each of these circuit types requires an additional control signal in order to perform its system function.

More specifically, *latches* use an *enable* signal. When this signal is on, they store information, and their outputs do not change even if the information presented to their inputs changes. When their enable signal is off, latches act just like buffers. Turning on the enable signal in effect "freezes" in place whatever information was passing through the latch, so that the latch stores it.

Registers use a *clock* signal instead of an enable signal. When the clock signal goes through a transition from off to on, this "rising edge" causes the information present at the inputs to be stored in the register, and then to remain present at the register outputs until another rising edge occurs. When the clock is in a steady-state condition (a "level"), either on or off, or even when the clock goes through a transition from on to off (a "falling edge"), the outputs of the register do not change. Thus, unlike latches, registers lack a mode in which they act exactly like buffers and pass information directly from their inputs to their outputs. This lack is a consequence of the control signal being "edge-sensitive" rather than "level-sensitive."

Transceivers are bidirectional interface circuits capable of interconnecting two buses so that information can pass in either direction. Most of the transceiver parts in production today are *buffer transceivers*—they are like two cross-coupled buffer circuits within a single 20-pin package. A 16-bit buffer transceiver has eight A-bus data pins and eight B-bus data pins. Either the A-to-B buffers may be enabled, or the B-to-A buffers, or neither; if both sets of buffers were to be enabled, obviously there would be a race condition on each of the data lines, and so the control structure of some buffer transceivers specifically disallows that mode of operation. (Some other types do allow it.) Buffers which are not enabled are, of course, in the hi-Z state. Thus each buffer transceiver interface circuit consists of eight logical elements, and each of these logical elements consists of two simple-buffer elements cross-coupled back-to-back so that the input line for one is the output line for the other and conversely.

Latch transceivers and *register transceivers* have not yet become major factors in the marketplace, but several semiconductor houses now have such devices in development. Two factors have delayed their introduction relative to that of buffer transceivers: they require too many control signals to fit into a standard 20-pin interface-circuit package, and they dissipate more power than buffer transceivers. Both of these problems have by now essentially been solved.

Pipelines are unidirectional interface circuits having more than one full-width internal latch/register or "stage," but typically having just one set of parallel data inputs and one set of parallel data outputs. Two-stage latch pipelines, and both two-stage and four-stage register pipelines, are coming soon also. The four-stage devices can store twice as much information per package, but the two-stage devices can be reconfigured more flexibly and have a greater degree of separate control for each stage.

Understanding and Using Interface

How Designers Choose Interface Circuits

In the real world, a digital-logic designer doesn't set out deliberately to use some particular interface circuit whose properties he has carefully learned, in the same way that he might for instance set out to use a bit-slice registered ALU or a multiplier/divider. Rather, as we have said, it is much more likely that it all starts with some innocent-looking little line between two blocks on his preliminary system block diagram which, it turns out, can't really be just a simple little line after all.

Maybe the data which travels on that little line goes away at the source unless the little line is actually also capable of seizing it at the proper time and remembering it. Or maybe the end of the little line is an assertive-low system bus, with enough loads hanging off it to call for almost 30 milliamps of drive capability in whatever contemplates driving the bus, which doesn't quite jibe with the 2-milliamp drive capabilities and assertive-high outputs of the MOS LSI device from which the data is coming.

At this point the designer needs an interface circuit, and—wittingly or unwittingly—he must go through a several-stage decision process to determine what interface circuit he needs to actually implement that little line, before his block diagram can turn into a system. He must also fervently hope that, by the time he gets to the final twig on his decision tree, the interface part he needs will turn out to actually exist. Figure 1 is an example.

A top-down design approach, as illustrated in Figure 1, isn't always wise with integrated circuits, simply because the chances are fairly good that the desperately needed circuit actually *won't* exist[r1]. And there was a time, not all that long ago, when only a quasi-random subset of all of the obviously possible variations of the basic interface parts had reached full production status, so that they could be bought and plugged in. The hapless designer just had to memorize what that subset was, and do his design bottom-up from there.

Today, chaos is giving way to order, and enough of the possible interface parts which a designer might want do by now exist (or will exist shortly) that the kind of top-down thought process portrayed in Figure 1 really *will* work out all right when designing with interface. For instance, the line of interface parts now in production at Monolithic Memories is sufficiently orderly to be organizable into the matrix of the Interface Selection Guide on page 13-2 of this data book. Although this Guide is still somewhat irregular, it is at least recognizable as first-cousin to a logic-design Karnaugh map, and you can actually get your hands on any of the interface parts in the matrix.

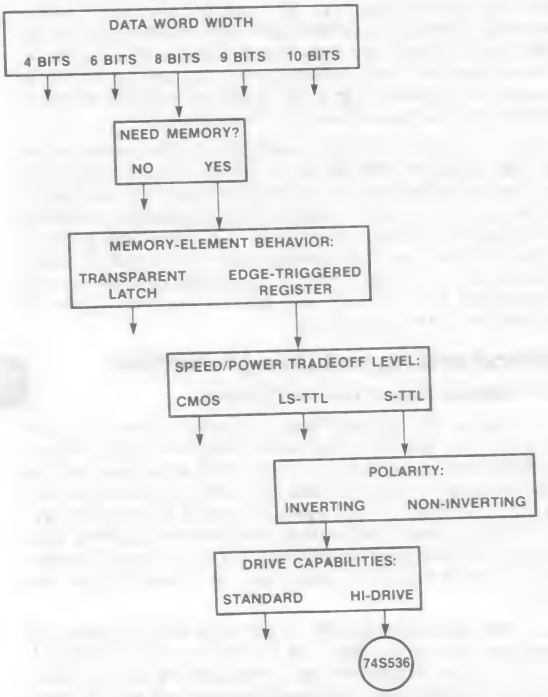


Figure 1. Interface-Circuit-Selection Decision Tree

The dimensions of variation for interface parts in any such Karnaugh map are, of course, two-valued "Boolean" variables. It is realistic from both logical and historical viewpoints to consider that all of the interface parts of the Interface Selection Guide have been derived from a very few basic types, by implementing those combinations which make sense of several two-valued properties of interface parts. These are:

- Commercial versus military temperature-range operation.
- High-speed Schottky (S-TTL) or low-power Schottky (LS-TTL) speed/power range.
- Noninverting or inverting outputs.
- No memory capabilities in the logical elements, so that they operate as buffers; or memory capabilities therein, further subdivided according to whether the logical elements operate as latches or registers.
- Compound 16-bit interface circuits or simple 8-bit interface circuits.
- Hi-drive or standard levels of current-sinking capability (I_{OL}) at the outputs.
- Schmitt-trigger or standard inputs.
- For non-three-state parts, master-reset or clock-enable control inputs.
- Series-resistor or standard outputs.

Obviously, not all imaginable combinations of the above properties actually exist as parts, or would even be useful if they did; and semiconductor houses cannot afford for long to offer 2^n interface-circuit part types for rapidly increasing n. Moreover, certain of the properties which today have just two possible major choices (e.g., S-TTL and LS-TTL) may soon have more than two.

Nevertheless, by now the matrix approach has been fully-enough implemented to offer a very helpful perspective to the working designer.

Part numbers today allow some of the properties of interface circuits to be directly inferred, at least if the part number follows the conventions of the industry-standard "54/74" numbering series. 54/74 part numbers have a well-defined format VVE4TxxxP, with the following interpretation:

- VV — a prefix which varies somewhat from vendor to vendor, although several vendors now use the prefix "SN."
- E4 — a temperature-range environmental specification. "54" implies the military temperature range (−55°C to +125°C), and "74" the commercial temperature range (0°C to +70°C for several vendors, and 0°C to +75°C for Monolithic Memories). In any case, interface circuits must run properly over a very wide temperature range.
- T — a solid-state-circuit technology. Upwards of a dozen of these have been promoted, with widely varying success, during the last decade. The earliest one, plain old gold-doped TTL, omitted using any special letter in part numbers. Today, the two dominant technologies are "S" (high-speed Schottky) and "LS" (low-power Schottky). Others likely to become quite important include "F" (for "FAST," a lower-power form of high-speed Schottky), "ALS" (advanced low-power Schottky), and "SC" and HCT" (isoplanar CMOS processed to be fully TTL-voltage-level compatible).
- xxx — a two-digit, three-digit, and today sometimes even four-digit number which uniquely specifies the *pin-out* of the part and its "functional behavior" (see the explanation which follows), independent of speed/power range.

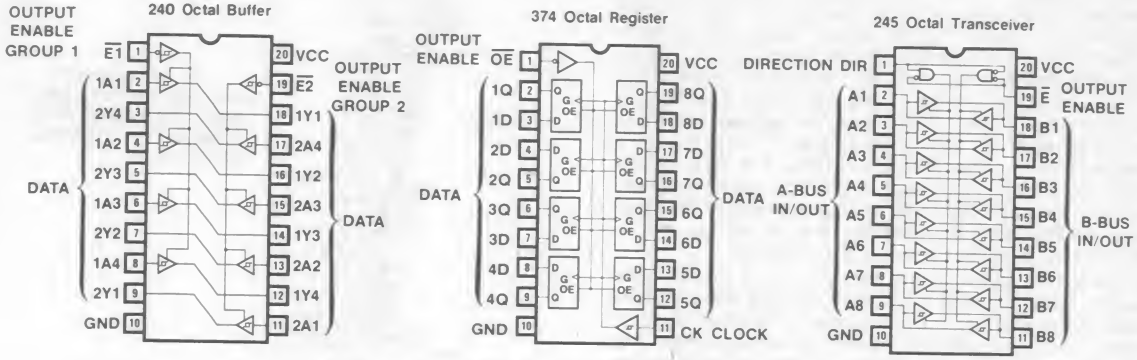
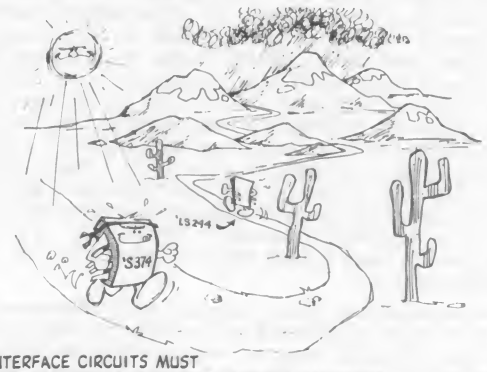


Figure 2. Pinouts for the Three Basic 20-Pin Interface Parts

- P — a package type: plastic, cerdip, flatpack, leadless chip carrier, sidebrazed ceramic, small-outline surface-mount, or whatever.

The functional behavior of a circuit can be defined somewhat circularly as **"what a designer needs to know about the circuit in order to construct designs which operate properly using parts from any supplier interchangeably."** This definition is akin to one classic definition of computer architecture as **"...the structure of the computer a programmer needs to know in order to be able to write any program that will correctly run on the computer."**[2]



"... INTERFACE CIRCUITS MUST RUN PROPERLY OVER A VERY WIDE TEMPERATURE RANGE..."

Two parts produced using different solid-state-circuit technologies may exhibit essentially the same functional behavior. If that is the case, and if either part will also satisfy system timing constraints (which is an issue quite separate from that of "functional behavior") and input/output voltage compatibility constraints, the designer does not need to care what kind of internal gates are used within the part—Schottky TTL, ECL, CMOS, NMOS, or water wheels. On the other hand, two parts produced using the same technology may have subtle, or even drastic, differences in their functional behavior; for example, one may have inverting outputs, or hi-drive outputs, or Schmitt-trigger inputs whereas the other does not.

The Matrix of Interface Part Types

The interface parts of the Interface Selection Guide all have one of just three different pinouts, shown in Figure 2, in their usual 20-pin plastic or cerdip SKINNYDIP™ form.

All of the buffers have the same pinout as the 'S240. They differ in speed/power range, in the polarity of the outputs, in the noise-rejection capabilities of the inputs (Schmitt-trigger or standard), and in enable structure (complementary or assertive-low) as shown in Figure 3, which really *is* unequivocally a Karnaugh map.

	COMPLEMENTARY ENABLES		ASSERTIVE-LOW ENABLES		
S-TTL	'S210	'S241	'S244	'S240	USUAL INPUTS
	'S310**	'S341*	'S344*	'S340*	SCHMITT-TRIGGER INPUTS
LS-TTL	'LS310	'LS341	'LS344	'LS340	
	'LS210	'LS241	'LS244	'LS240	USUAL INPUTS
	INVERTING OUTPUTS		NON-INVERTING OUTPUTS	INVERTING OUTPUTS	

NOTES: *—announced by Texas Instruments, and in development at Monolithic Memories.
**—in development at Monolithic Memories.

Figure 3. 8-Bit Three-State Buffers

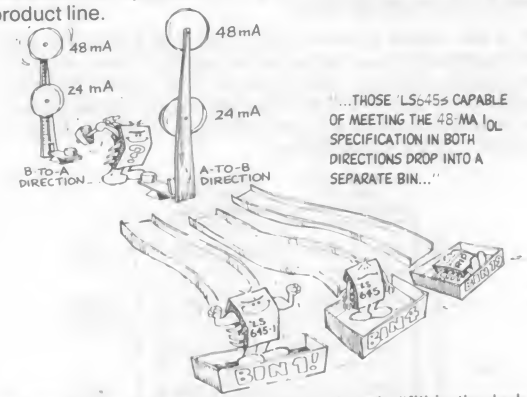
All of the latches and registers have the same pinout as the 'S374. They differ in whether the memory control line is level-sensitive (latch) or edge-sensitive (register), in speed/power range, in the polarity of the outputs, and in the I_{OL} (current-sinking drive) capability of the outputs as shown in the Karnaugh map of Figure 4.

	LATCHES		REGISTERS		
S-TTL	'S533	'S373	'S374	'S534	USUAL (20-mA) OUTPUTS
	'S535	'S531	'S532	'S536	HI-DRIVE (32-mA) OUTPUTS
LS-TTL	— —	— —	— —	— —	
	'LS533	'LS373	'LS374	'LS534	USUAL (24-mA) OUTPUTS
	INVERTING OUTPUTS		NON-INVERTING OUTPUTS	INVERTING OUTPUTS	

Figure 4. 8-Bit Three-State Latches and Registers

The three transceivers of the Interface Selection Guide are more specifically *buffer transceivers*—compound 16-bit interface circuits like two 8-bit buffer circuits cross-coupled "back-to-back" within a single device. They differ in input-current and output-leakage-current specifications, which here are indistinguishable for test purposes since every data pin is both an input and an output; the 'LS245 specification is tighter. (The 'LS245-1 is *also* specified as faster, but that is *not* a difference in "functional behavior.") There is also a difference in I_{OL} capability; the 'LS645-1 is specified as higher. Actually, all three devices undergo identical fabrication, and are separated only at final testing; for instance, those 'LS645s capable of meeting the 48-mA I_{OL} specification in both directions drop into a separate bin.

Upcoming developments in interface parts will tend in many cases to follow the matrix approach, at least partially. Even where the new parts do not fit perfectly into the matrix of existing parts, some attention is likely to be paid to issues of balance and symmetry over the entire interface-circuit product line.



In some cases, new interface parts directly "fill in the holes" in the matrix. For instance, the most recent additions to Monolithic Memories' line of interface parts are:

Function	Speed/ Power	Polarity	Feature	Part Number
Register	S	Noninv.	Master Reset	SN54/74S273
Register	S	Noninv.	Clock Enable	SN54/74S377 SN54/74S383@
Buffer	S	Noninv.	Series Output Resistor	SN54/74S734*
Buffer	S	Noninv.	Series Output Resistor	SN54/74S731
Buffer	S	Inv.	Series Output Resistor	SN54/74S730#
Buffer	S	Inv.	Series Output Resistor	SN54/74S700

NOTES: @—The 'S383 differs from the 'S377 only in having open-collector outputs rather than totem-pole outputs.
*—The 'S734 is a direct replacement for AMD's Am2966.
#—The 'S730 is a direct replacement for AMD's Am2965.

Table 1. Pending Additions to the Monolithic Memories Interface-Part-Type Matrix

"...THE 'S273 AND 'S377, LIKE THEIR LS-TTL COUNTERPARTS, ARE DESIGNED WITH STANDARD TTL 'TOTEM-POLE' OUTPUTS..."

The 'S273 and 'S377 bring to higher-performance TTL systems the same functional behavior which has long been available for medium-performance TTL systems, with the popular 'LS273 and 'LS377 parts. The 'S273 and 'S377, like their LS-TTL counterparts, are designed with standard TTL "totem-pole" outputs. Somehow, in the somewhat more chaotic early days of 8-bit interface, the need for high-speed Schottky versions of these parts got overlooked by most interface producers.

Since the 'S273 and 'S377 are totem-pole-output parts, the control pin which gets used on the 'S374 (whose pinout they otherwise follow) for "Output Enable" for the three-state outputs is available for something else. The 'S273 uses it as a "Master Reset" ($\overline{MR}$) input, capable of forcing all of the eight D-type flipflops on the chip into the off (low) state simultaneously, regardless of their previous state—*or* of the state of the clock line and/or the data-input lines. The 'S377, on the other hand, uses that same pin as a "Clock Enable" ($\overline{CK\ EN}$) input, which in effect either allows the clock signal to reach the eight D-type flipflops on the chip, or else cuts it off from reaching the flipflops so that they are not clocked and just sit there holding whatever information they contained previously.

The major applications for these parts are in situations where 'S374s would be difficult to control appropriately. Because of the 'S273's $\overline{MR}$ input, its forte is *control* applications—instruction registers, microinstruction registers, timing-pulse registers, and sequential circuits in general, and sometimes as eight *individual* separate D-type control flipflops in one package. In all of these applications, there *has* to be a way to force the system into some proper initial state, so that it "starts off on the right foot" and does not get into some unplanned-for, untestable, unpredictable machine-psycho condition on power-up. The 'S377, on the other hand, because of its $\overline{CK\ EN}$ input, is the optimum choice for the highest-performance TTL pipeline paths for data, instructions, microinstructions, and address parameters in "overlapped-architecture" machines such as array processors and high-performance minicomputers. Its open-collector counterpart, the 'S383, can be used to drive open-collector buses or to provide wired-OR or wired-AND logic functions.

The 'S700, 'S730, 'S731, and 'S734 feature a new type of output stage incorporating a series resistor, designed to efficiently drive highly-capacitative loads such as arrays of dynamic-MOSRAM inputs. Rise and fall times are more

symmetric than with 'S240-type buffers, and the latter need an *external* series limiting resistor for their own protection when driving highly capacitative loads.

Consequently, although 'S240-type buffers may exhibit greater speed when tested under light loading conditions, 'S730-type buffers are likely to perform better under realistic system conditions when driving large distributed capacitative loads is a major factor in the application.

Of these four new buffers, two—the 'S730 and 'S734—are second-source versions of the Am2965 and Am2966 respectively, originally introduced by AMD. The other two—the 'S700 and 'S731—are complementary-enable versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244 respectively. Complementary-enable buffers excel in driving buses with two multiplexed sources for the information, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system.

The four new 'S730-type parts may be grouped with Monolithic Memories' existing line of buffers in a 2 × 2 matrix chart or Karnaugh map, with the dimensions of this map chosen to be the polarity of the second-buffer-group enable input E_2 (here across the top) and the polarity of the data-buffer logical elements themselves (here down the side), thus:

		Polarity of E_2*	
		$\overline{E}_2$	E_2
Polarity of Data Buffers	Inverting	'LS240 'LS340 'S240 'S340# 'S730	'LS210 'LS310 'S210 'S310# 'S700
	Noninverting	'LS244 'LS344 'S244 'S344# 'S734	'LS241 'LS341 'S241 'S341# 'S731

NOTES: *— Since $\overline{E}_1$ is assertive-low for *all* of these parts, the parts with an assertive-low $\overline{E}_2$ are "assertive-low enable" parts, whereas the parts with an assertive-high E_2 are "complementary-enable" parts.

#— In development at Monolithic Memories.

Table 2. 8-Bit Buffers Grouped by Polarity and Enable Structure

By this time, many presently-unused SN54/74xxx part numbers have already been reserved for other potential new parts, even though not all of these parts are yet in production. Nevertheless, it was at least possible to part-number these four series-output-resistor buffers in such a way that the relationship among the four types remains the same as for 'S240-type buffers. To state this another way, one can add 490 to the last three digits of the usual buffer part number to get the part number for the corresponding series-output-resistor part, e.g., 'S241 + 490 = 'S731, etc.

Directions In The Evolution of Interface Parts

More Bits per Package

Historically, the first interface parts were 16-pin TTL devices offered during the early 1970s, usually with four or six "logical elements" per package. One "logical element" handles one data bit; in simple interface parts, a logical element may be a buffer, a latch, or a register (with "register" here implying an edge-triggered flipflop).

As the digital-electronics industry shifted from MSI to LSI integrated circuits, and from the quaint and irregular old-time computer word lengths to word lengths which are multiples of eight bits (most often 8, 16, or 32), 8-bit interface devices became the only way to go for simple electrical data transformations—chip counts got intolerably high with 4-bit devices, and 6-bit devices were awkward misfits in most of the newer designs![3] And, to have eight input data lines, eight output data lines, power and ground, and two control signals, an integrated-circuit package has to have 20 pins.

To conserve board space, the width of this 20-pin package was chosen to be 300 mils (.300") like that of the overwhelming majority of the then-existing bipolar MSI and SSI devices. Hence, during the 1970s, the present 20-pin 300-mil SKINNYDIP™ package became the standard for interface circuits. One 20-pin SKINNYDIP™ takes up only about half as much board space as one of the older 600-mil 24-pin packages, which were then being used for a few early 8-bit interface parts such as the Intel 8212.

"...ONE 20-PIN SKINNYDIP™ TAKES UP ONLY ABOUT HALF AS MUCH BOARD SPACE AS ONE OF THE OLDER 600-MIL 24-PIN PACKAGES..."

24-pin interface parts are obviously the next major development to come. In the early 1980s, mechanical packaging problems which previously had inhibited the introduction of a 24-pin 300-mil SKINNYDIP® where solved and this package is now also coming into widespresd use for PROMs, PAL® programmable-logic circuits and so forth. So what might one do with four additional pins in an interface part?

One answer is to spend all four of them for additional *control* signals in order to achieve more flexible parts, such as the Monolithic Memories SN54/74LS380 "multifunction" 8-bit register. (See page 8-16 of this data book.) This part is actually implemented with "hard-array logic" technology, and has an internal structure like one form of PAL®.

Another answer is to spend all four of them for additional *data* signals, equally for inputs and outputs. The result is 10-bit interface parts with functionality similar to that of existing 20-pin 8-bit parts.

A middle-of-the-road answer is to divide them equally between control signals and data signals. This approach leads to 9-bit interface parts with improved functionality.

16-bit "double-density" interface™-circuits—dual 8-bit circuits in a single 24-pin SKINNYDIP™—are a more far-reaching answer than the preceding ones. These circuits use the four extra pins to provide separate control inputs for *both* 8-bit internal groups, and also to provide improved functionality. The number of data pins is held at 16 by *multiplexing* the use of two 8-bit groups of input and/or output pins.

The motivation for 16-bit interface parts is, first of all, to cut component counts by replacing two parts with one in as many situations as possible, in order to save board space and assembly costs. Particularly in high-performance computers and array processors, the packaging itself is expensive when it must be designed to provide a proper signal-transmission environment for ultra-fast logic. An almost-50% cut in the board area required for the interface parts—here, as always, the "glue" which holds the whole system together—may result in major indirect savings.

But there are other incentives besides sheer cost reduction which favor cramming as much logic as possible into a given board area. There usually is only one board size in a chassis (or even in a system), and any logic subsystem which cannot fit onto one such board immediately incurs a *speed* penalty attributable to board-to-board communications—extra buffers for noise-free signal transmission, extra signal-path length on each board over to the edge where the connectors are, more extra length in the backplane wiring, and lots of additional inductance and capacitance permeating all of the above.

So, saving board area is very likely to improve *both* system cost *and* system performance, by increasing the probability that a given logic subsystem will fit onto just one board.

Interface-part internal element density has for many years been increasing at a rate which is, to say the least, unspectacular. Going from four to six to eight to sixteen logical elements in an interface-circuit package doesn't seem like a whole lot, compared for instance to going from 1K to 4K to 16K to 64K to 256K bits in a single dynamic-MOSRAM package in roughly the same number of years.

But, consider what a *true* LSI interface circuit would have to look like—one with the same magnitude of "equivalent gate count" being bandied about for today's microprocessors, dynamic MOSRAMs, and so forth. First of all, it would need to have *several hundred data inputs* and *several hundred data outputs,* so that the most immediately-plausible mechanical design for a package would resemble a sea urchin! And, if it were implemented using any present-day TTL technology, the part would dissipate enough *watts* to need cooling fins like a Porsche cylinder head!

And so it has turned out that progress over time in increasing the logical-element density for interface parts has been more or less linear, while progress in increasing the level of integration for microprocessors and dynamic MOSRAMs has been more or less exponential. It is no accident that a basic phrase of the definition for "interface circuits" quoted earlier in this paper is **". . . which do not lend themsIves to higher levels of integration . . ."** If these same density trends continue, digital electronic systems of the future may actually have a *higher* proportion of packages allocated to interface circuits than is typical today, which if it happens is likely to surprise quite a few people.

Structure of 16-Bit Interface Circuits

Common configurations of two 8-bit interface parts used together furnish a natural starting point for the definition of useful 16-bit interface parts. When the same configuration tends to occur over and over again, it is natural to "draw a boundary around it and put it all on one chip," unless of course the resulting compound chip turns out to need too many pins.

Figure 5 illustrates three such two-part configurations which are observably very common, and intuitively very plausible:

- "Back-to-back" or "cross-coupled." (Figure 5A).
- "Nose-to-tail" or "pipelined." (Figure 5B.)
- "Side-by-side" or "parallel." (Figure 5C.)

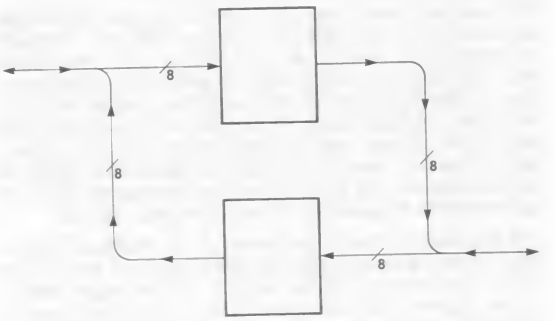


Figure 5A. Back-to-Back Configuration

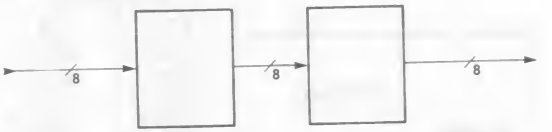


Figure 5B. Nose-to-Tail Configuration

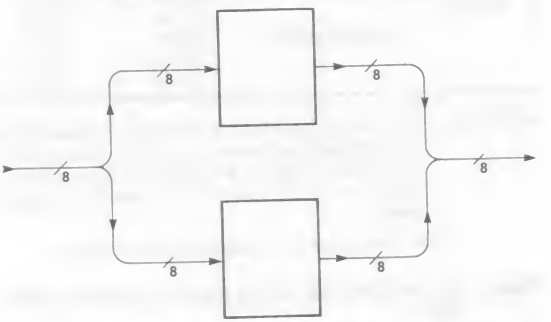


Figure 5C. Side-by-Side Configuration

Figure 5. Common Configurations of Two 8-Bit Interface Parts

The back-to-back configuration, when applied to simple 8-bit buffers, leads to buffer transceivers such as the 'LS245. The 'LS245 is, of course, still a 20-pin part; the choice was made to change its enable structure from that which would be strictly implied by placing two 'LS244s back-to-back, in order to hold the package size to 20 pins and to disallow having both directions simultaneously enabled. These same statements continue to hold for the 'LS645 and 'LS645-1. The 'LS640 and 'LS640-1 are inverting buffer transceivers, and the 'LS643 and 'LS643-1 incorporate an 8-bit inverting buffer back-to-back with an 8-bit noninverting buffer; there are also open-collector equivalents to these parts and the 'LS645 and 'LS645-1. The entire series features the same

enable structure, with a master enable line $\overline{E}$ controlling *both* sets of buffers and a direction line DIR to allow just one direction to be enabled at a time.

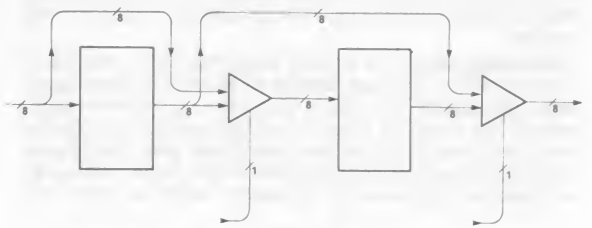


Figure 6. Two-Stage Pipeline Register Configuration

Applied to 'LS373 latches and 'LS374 registers, the back-to-back configuration leads to the 24-pin 'LS547 latch transceiver and the 'LS546 register transceiver respectively. These parts are just what one would expect them to be, with individual output-enable and clock control inputs for each 8-bit group, except that there are enough pins to also give each group clock-enable control inputs like the 'S377. The 'LS567 and 'LS566 are the corresponding inverting parts.

The nose-to-tail and side-by-side configurations do not lead to anything very interesting with buffers, at least as long as there are only enough pins for one 8-bit input data path and one 8-bit output data path. Latches and registers, however, are entirely another matter. It turns out to be attractive to *combine* these two configurations, even though at first glance they look quite dissimilar, into a single "two-stage pipeline" configuration as shown in Figure 6. Such a two-stage pipeline can operate in either a nose-to-tail mode or a side-by-side mode, according to the setting of the two internal multiplexers shown in Figure 6. Applied to 'LS373 latches and 'LS374 registers, this more powerful configuration leads to the 24-pin 'LS549 latch pipeline and the 'LS548 register pipeline. For these parts, the control inputs are a final-stage output enable, selects for each mux, a common clock (or latch-enable for the 'LS549) input for both stages, and individual clock-enable inputs for each stage.

To clarify the timing control of these parts, the 16-bit register parts ('LS546, 'LS566, and 'LS548) have individual clock-enable signals for each 8-bit group, and either individual clock signals ('LS546 and 'LS566) or a common clock signal ('LS548). The 16-bit latch parts ('LS547, 'LS567, and 'LS549), since the "clock" signal turns into a level-sensitive latch-enable signal, have two independent ways of enabling storage in each of the two stages. Thus, the 'LS547 and 'LS567 parts feature two separate and equivalent latch-enable control inputs for each 8-bit group, either one of which can cause the group to "latch up" and store information. The 'LS549 part has the same operating mode, except that each 8-bit group has one *separate* latch-enable control input and there is one more latch-enable input *common* to both groups.

As with other TTL 8-bit latches and registers, the part-numbering scheme assigns odd numbers to latches and even numbers to registers.

Front-loading latches are one other type of 16-bit interface part. The 'LS646 (noninverting) is to a first approximation an 'LS645 superimposed upon an 'LS546. (The numbering scheme wasn't *planned* to be that cute—it just happened.) The 'LS648 is a similar inverting part. To clarify what is meant, each of the eight logical elements of an 'LS646 consists of two back-to-back buffers and two back-to-back flipflops, with a parallelled buffer and flipflop pointing in the A-to-B direction and a similar buffer-flipflop pair pointing in the B-to-A direction. The 'LS646 and 'LS648 are three-state parts; there are also equivalent open-collector parts, and some other similar parts with a slightly different control structure.

32-bit interface parts are also visible on the horizon. Two four-stage pipelines, the Am29520 and Am29521, are offered by AMD as members of a series of signal-processing parts, and Monolithic Memories plans to make them also. As compared to the 'LS548 and 'LS549, they offer twice as many stored bits per square inch of board, but considerably less flexibility in accessing and controlling register contents.

The matrix approach to classifying various interface parts can be extended to encompass transceivers and pipelines, as is done in Table 3. The correspondence between the various 8-bit simple-interface parts and the 16-bit compound interface parts which are in a sense derived from them, is summarized in Table 4.

Configuration	Buffers	Latches	Registers	Front-Loading Latches
Simple	'210 '310 '240 '340 '241 '341 '244 '344	'373 '531 '533 '535	'374 '532 '534 '536	---
Back-to-Back	'245 '640 '640-1 '643 '643-1 '645 '645-1	'547 '567	'546 '566	'646 '648
Two-Stage Pipeline	---	'549	'548	---

Table 3. Matrix Classification Scheme for 8-Bit and 16-Bit Interface Parts

Simple Interface Type	Compound Interface Type	Number Of Pins	Buffer	Latch	Register
Transceivers:					
'244	'245 '645 '645-1	20	X		
'240	'640 '640-1	20	X		
'240/'244	'643 '643-1	20	X		
'373	'547	24		X	
'374	'546	24			X
'533	'567	24		X	
'534	'566	24			X
Pipelines:					
'373	'549	24		X	
'374	'548	24			X

Table 4. Equivalences Between Simple and Compound Interface Types

Various Applications of Interface Parts

Some Logic-Design Examples

Several illustrative designs using various interface parts may suggest some design insights and some creative ways to use interface. The designs presented have generally been excerpted from actual digital systems.

Reading a switch setting to establish an externally-defined system parameter, such as a device address, is a mundane but essential task in many microprocessor-based systems. Figure 7 illustrates how a group of eight switches may conveniently be read using a byte-wide buffer such as the 'LS244. Since the switches must be electrically isolated from the bus, the 'LS244's three-state outputs are disabled by control signals originated by the microprocessor until the time comes to read in the switch settings. Because the 'LS244 can supply up to 24 milliamps of I_{OL} to drive the bus, this simple scheme can be utilized even on heavily-loaded system data buses.

If still more drive capability is needed, an 'S244 in the same configuration can sink up to 64 milliamps. And, if the system is to be operated in an industrial environment and the switch signals entering the buffer inputs are subject to severe noise, the Schmitt-trigger 'LS344 type of buffer can also be substituted for the 'LS224 with no other change to the circuit.

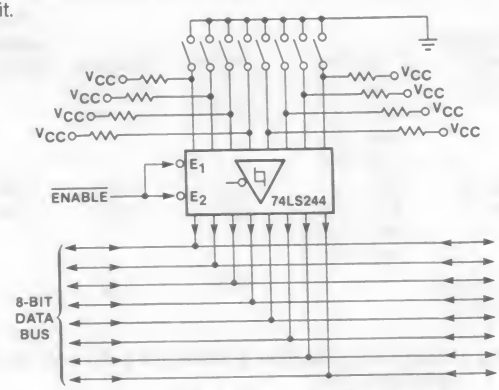


Figure 7. Switch-Setting Readin Circuit

Interfacing two separate buses is a very standard application for transceivers. Figure 8 shows an 'LS245, which has a control structure such that one control signal selects the *direction* of data transfer and the other one independently allows data transfer to be *enabled or disabled*. Thus, the two buses can be operated totally isolated from each other, or else either one may be made to follow the other. Depending on the drive-capability and polarity requirements of the application, any of the other buffer transceivers might be used here instead. Or, if memory as well as cross-coupling is required, a latch transceiver or register transceiver might also be used in a similar manner.

Driving a dynamic-MOSRAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9. This part is an inverting complementary-enable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.

First of all, a TTL inverting buffer normally has one less transistor — and hence one less delay — in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOSRAMs really don't care if their addresses come in "true" or "complemented" form as long as that form *never* changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here CAS or "Column Address Strobe") is tied directly to both $\overline{E}_1$ and E_2 and the two 4-bit groups of outputs are tied together.

Finally, because of the internal series resistor in the'S700's output structure, this part (like the 'S730/1/4) can drive highly capacitative loads, of say up to 70 dynamic-MOSRAM inputs, without the need for external limiting resistors to control undershoot, resulting in a net system speed gain since signal rising and falling transition times remain symmetric. Otherwise, the effective logic delay of the buffer (which is simply the

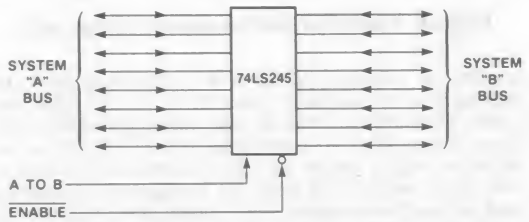


Figure 8. Interfacing Two Separate Buses

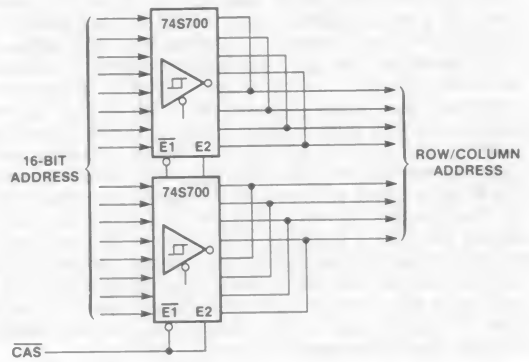


Figure 9. Multiplexed Row/Column Address Drivers

worse of the two transition times) would get degraded, since the use of an external series resistor would have greatly lengthened the low-to-high transition time.

Demultiplexing and holding address and data words for single-bus microprocessors is an application which takes advantage of the strong points of the 'S531 as shown in Figure 10. Since the 'S531 is a "transparent latch" and can operate as a buffer when necessary, the memory system designer can take advantage of the *full* time slots when the address and data signals are present on the microprocessor outputs. Because the address and data signals are then present for a longer period of time at the 'S531 outputs, it may be possible to use slower (and therefore less expensive!) memory devices than if edge-triggered registers had been used here instead. The three-state outputs of the 'S531 allow the designer to implement bidirectional data buses and DMA address schemes. Variations on this approach can use 'S373s if less drive capability is needed, or 'LS373s if less speed is needed as well; or 'S535s, 'S533s, or 'LS533s under the same respective circumstances if the address and data buses to be driven are assertive-low

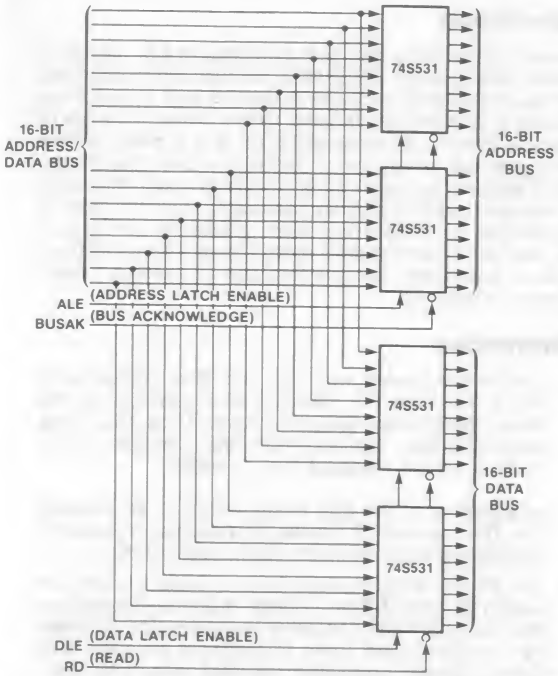


Figure 10. Address/Data Demultiplexer for Single-Bus Microprocessors

ıccording to the system definition. If the data-bus interface ıeeds to have latching capability also for data returning to he microprocessor, then 'LS547s are an excellent choice.

Synchronizing the state changes of a PROM-based control sequencer is easily performed using a register with a clock-enable feature, like the 'LS377 shown in Figure 11. In his simple sequencer, a 4-bit counter steps through the PROM addresses. The counter may be reset to address 0000, or loaded with any 4-bit address. The 32 × 8 PROM, with five address lines, allows for one external input as well as the four bits from the counter. The PROM outputs are pipelined using the 'LS377, which eliminates PROM output glitches, synchronizes the state changes of the sequencer with the system clock, and speeds up the effective cycle ime. The availability of enable control inputs on both the counter and the 'LS377 allows forcing "wait" states, where both the counter and the register hold their current state for extended periods of time. If a higher-speed implementation of this design is needed, a 74S161 or 93S16 counter can eplace the 74LS161, one of Monolithic Memories' new 3S081 ultra-speed 32 × 8 PROMs (25 nanoseconds worst-ase and 9 nanoseconds typical for t_{AA}, instead of 50 and 7 nanoseconds respectively) can replace the 6331-1, and n 'S377 can replace the 'LS377.

Saving Designs at the Last Minute, or Planning Ahead

Designs hanging out over the edge of unworkability can ometimes be salvaged without any redesign effort, by eplacing standard interface parts with hi-drive, Schmitt-rigger-input, or even just inverting pin-compatible parts. Ii-drive parts such as the 'S532 or 'LS645-1 get dropped nto 'S374 or 'LS645 sockets respectively late in the design ycle, when the designer suddenly discovers that he has ung several too many inputs on his main system bus. chmitt-trigger-input parts such as the 'LS341 likewise get dropped into 'LS241 sockets shortly after the designer has recovered from his first observation of his actual bus waveforms on a good laboratory oscilloscope—it's that or back to the old drawing board. And, when he suddenly remembers after laying out a tightly packed board that "Oh, xxxx, that particular bus is assertive-*low*," it's nice to be able to simply substitute an 'S534 for an 'S374 in a few places rather than having to find room for several inverter packages. So a designer who has learned to think of interface parts in terms of the matrix approach will now and then find a particularly quick route to saving his skin.

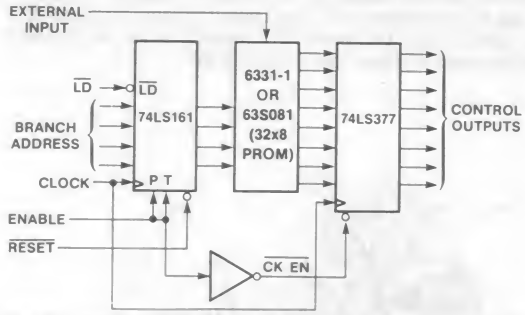


Figure 11. Synchronous PROM-Based Control Sequencer

However, an astute designer may use hi-drive, Schmitt-trigger-input, and inverting parts quite deliberately in order to gain speed, economy, drive capability, or noise immunity. A number of the industry-standard buses in the microcomputer world are assertive-low; and inverting buffers, latches, and registers are much more appropriate for connecting these to a microprocessor, or to a bit-slice arithmetic unit, than non-inverting parts with extra inverters in series just to make the polarity come out right. Similarly, Schmitt-trigger hex inverters whose only function in the data path is to provide noise immunity can be eliminated by using 'LS340-type buffers, which also provide significant drive capability and three-state outputs. The need to parallel three-state drivers and registers and split drive lines, just for extra drive capability, can be reduced or eliminated by using hi-drive parts. And, in an obvious but not trivial switch, substituting a high-speed Schottky part for a low-power Schottky equivalent part can beef up drive capability considerably.

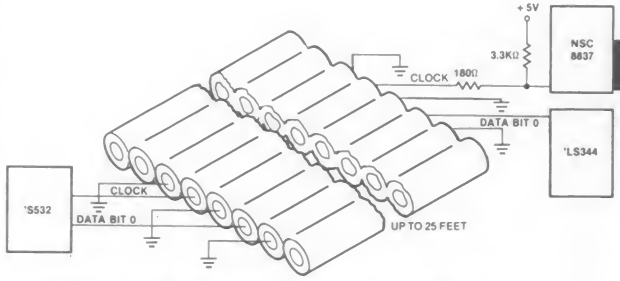
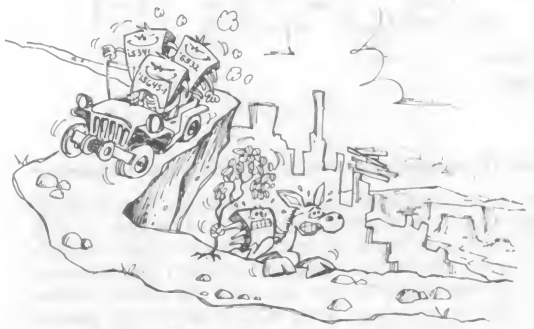


Figure 12. Flat-Cable Transmission Scheme Using Hi-Drive and Schmitt-Trigger-Input Interface Parts

Board-to-board signal transmission via flat cable is a particularly nice application for both hi-drive and Schmitt-trigger-input interface parts. The 32-milliamp outputs of, say, an 'S532 are better matched to the characteristic impedance of flat cable (usually 100 to 120 ohms) than 20-milliamp outputs would be. An adequate scheme, in many cases, for the

transmission of *data* from board to board uses 3M or similar flat cable. Every second cable wire is grounded at both ends for shielding, so that signal wires alternate with ground wires ("signal-ground-signal-ground"), and there is at least one ground wire at each edge of the cable. Signal wires are driven by 32-mA hi-drive latches or registers, and the receivers are Schmitt-trigger-input buffers, and that's all there is to it—no resistors, capacitors, or black magic. For a strobe, clock, or control signal, a linear receiver such as a National Semiconductor 8837 is used together with a 180-ohm series resistor and a 3300-ohm shunt resistor to V_{CC}, as shown in Figure 12. This overall scheme is compatible with some Digital Equipment Corporation buses, and is good for transmission distances of up to 25 feet.



"...DESIGNS HANGING OUT OVER THE EDGE OF UNWORKABILITY CAN SOMETIMES BE SALVAGED..."

Conclusion

Interface parts seem primitive alongside of LSI microprocessors and dynamic MOSRAMs, but they are inescapable and smart designers today have learned how to use them astutely. A powerful aid in doing so is to think of the set of interface parts as an array, which fits into a matrix whose dimensions are various circuit properties. Even though the rate of progress seems slow, the bit-density and functionality of interface parts is steadily increasing, and the time is approaching for designers to learn to take the next logical step and use 16-bit interface parts extensively in their systems, in order both to save cost and to improve overall system performance.

References

r1. "Bottom-Up Design with LSI and MSI Components," Chuck Hastings, *Conference Proceedings of the Fourth West Coast Computer Faire*. 11-13 May 1979, pages 359-365. Available from the Computer Faire, 570 Price Avenue, Redwood City, CA 94063

r2. "Architecture of the IBM System/360," G. M. Amdahl, G. A. Blaauw, and F. P. Brooks, *IBM Journal of Research and Development*, Volume 8 (1964), pages 87-101.

r3. "The 20-Pin Octal Interface Family—Today's Computer-System Building Blocks," Chuck Hastings, applications note available from Monolithic Memories, Inc. A longer paper written when buffer transceivers were the only visible 16-bit parts, but with more detail on the 8-bit parts.

8-Bit Buffers

SN54/74LS210 SN54/74S210
SN54/74LS240 SN54/74S240
SN54/74LS241 SN54/74S241
SN54/74LS244 SN54/74S244

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '210 and '241 types combine multiplexer and driver functions

Description

These 8-bit buffers provide high speed and high current interface capability for bus organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the low-power Schottky buffers and 0.4 mA I_{IL} on the Schottky buffers.

The '240 and '244 provide inverting and non-inverting outputs respectively with assertive low enables. The '210 and '241 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

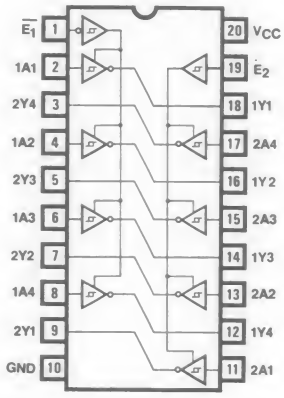
All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

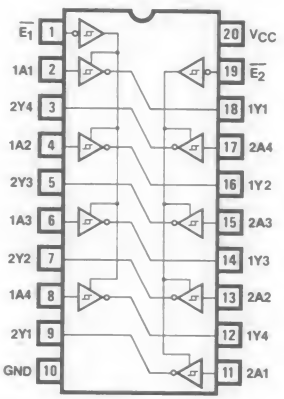
PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54LS210	J,F,L,W	Mil	High-Low	Invert	LS
SN74LS210	N,J,L	Com			
SN54LS240	J,F,L,W	Mil	Low		
SN74LS240	N,J,L	Com			
SN54LS241	J,F,L,W	Mil	High-Low	Non-Invert	
SN74LS241	N,J,L	Com			
SN54LS244	J,F,L,W	Mil	Low		
SN74LS244	N,J,L	Com			
SN54S210	J,F,L,W	Mil	High-Low	Invert	S
SN74S210	N,J,L	Com			
SN54S240	J,F,L,W	Mil	Low		
SN74S240	N,J,L	Com			
SN54S241	J,F,L,W	Mil	High-Low	Non-Invert	
SN74S241	N,J,L	Com			
SN54S244	J,F,L,W	Mil	Low		
SN74S244	N,J,L	Com			

Logic Symbols

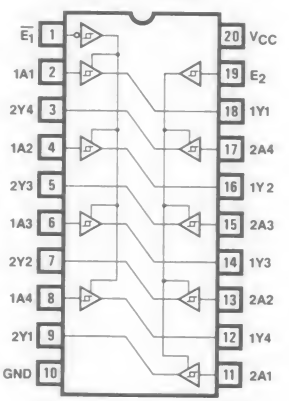
210 8-Bit Buffer



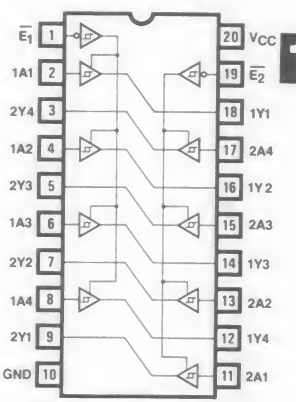
240 8-Bit Buffer



241 8-Bit Buffer



244 8-Bit Buffer



13

Function Tables

210

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

240

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

241

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

244

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

Absolute Maximum Ratings

Supply Voltage VCC 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis ($V_{T_+}-V_{T_-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA			0.4			0.4	V
				I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN,	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
			V_{IL} = 0.5V,	I_{OH} = −12mA	2						
			V_{IH} = 2V	I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
I_{OZH}				V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	LS210, LS240		17	27		17	27	mA
				LS241, LS244		17	27		17	27	
		Outputs Low		LS210, LS240		26	44		26	44	
				LS241, LS244		27	46		27	46	
		Outputs Disabled		LS210, LS240		29	50		29	50	
				LS241, LS244		32	54		32	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS210, LS240			LS241, LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}	Output Enable delay			20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				10	18		10	18	ns

13

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
ΔV_T	Hysteresis ($V_{T_+} - V_{T_-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.5V			−0.4			−0.4	mA
		Any E					−2			−2	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 48mA			0.55				V
				I_{OL} = 64mA						0.55	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −1mA				2.7			V
				I_{OH} = −3mA	2.4	3.4		2.4	3.4		
				I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}				V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	S210,S240		80	123		80	135	mA
				S241,S244		95	147		95	160	
		Outputs Low		S210,S240		100	145		100	150	
				S241,S244		120	170		120	180	
		Outputs Disabled		S210,S240		100	145		100	150	
				S241,S244		120	170		120	180	

†Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

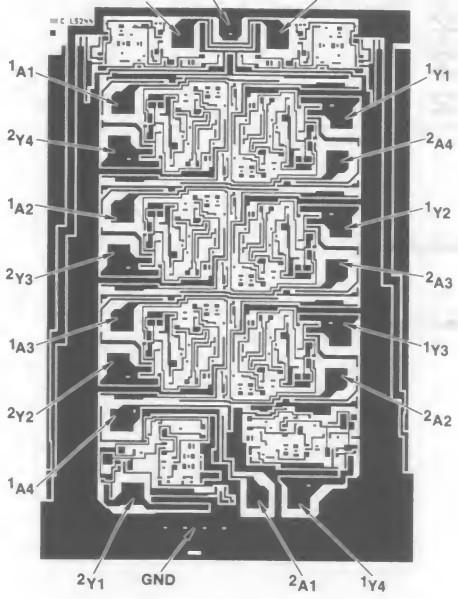
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S210, S240			S241, S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 50pF R_L = 90Ω		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output Enable delay			10	15		10	15	ns
t_{PZH}				6.5	10 *		8	12	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 90Ω		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

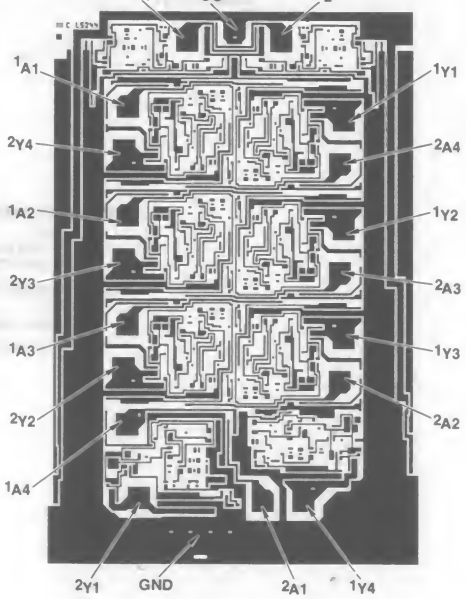
* For the S210 add 2 ns for the E_2 (Pin 19) enable

Die Configuration

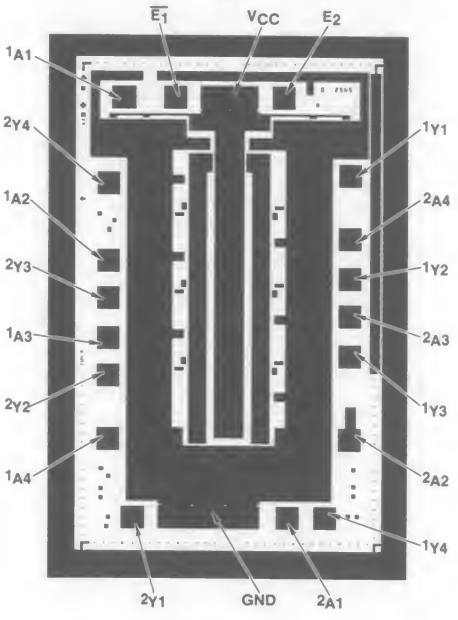
S210



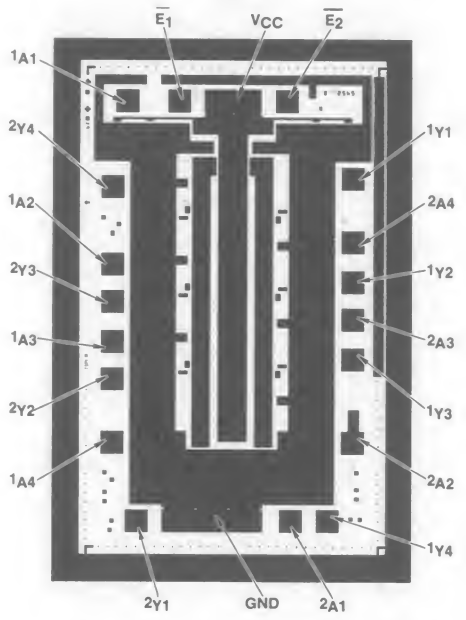
S240



S241



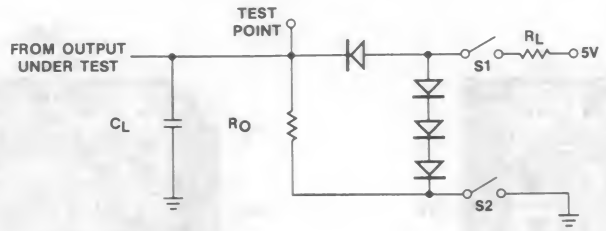
S244



Die Size: 85 x 146 mil

13

Test Load



FOR THE 'S210 SERIES
R_O = 1KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

FOR THE 'LS210 SERIES
R_O = 5KΩ
R_L,C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

Octal Buffers with Schmitt Triggers

SN54/74LS310 SN54/74LS341
SN54/74LS340 SN54/74LS344

Features/Benefits

- Schmitt trigger guarantees high noise margin
- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74LS210/240/1/4 — can be direct replacement in systems with noise problems

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54LS310	J,F,L,W	Mil	High-Low	Invert	LS
SN74LS310	N,J,L	Com			
SN54LS340	J,F,L,W	Mil	Low		
SN74LS340	N,J,L	Com			
SN54LS341	J,F,L,W	Mil	High-Low	Non-Invert	
SN74LS314	N,J,L	Com			
SN54LS344	J,F,L,W	Mil	Low		
SN74LS344	N,J,L	Com			

Description

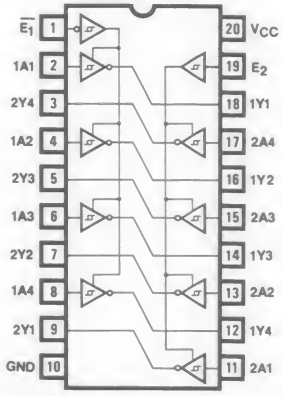
In addition to the standard Schottky and low-power Schottky octal buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 hex Schmitt-trigger and guarantee a full 400 mV noise immunity. The Schmitt-trigger operation makes the LS buffers ideal for bus receivers in a noisy environment.

The octal buffers provide high-speed and high-current interface capability for bus-organized digital systems. The PNP inputs provide improved fan-in with 0.2 mA I_{IL}. The '340 and '344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The '310 and '341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.

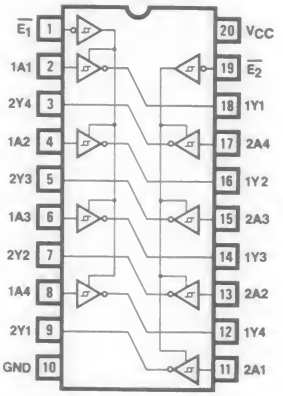
All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Logic Symbols

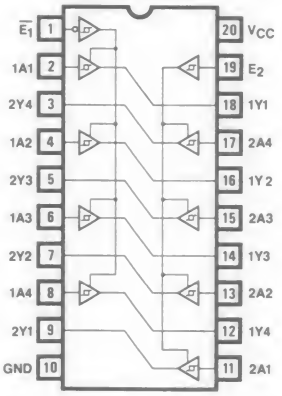
310 Octal Buffer



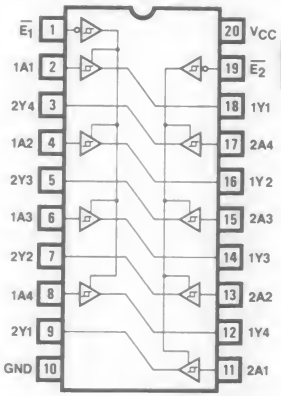
340 Octal Buffer



341 Octal Buffer



344 Octal Buffer



SKINNYDIP is a registered trademark of Monolithic Memories

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Function Tables

310

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

340

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

341

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

344

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive threshold voltage		V_{CC} = 5V		1.5	1.7	2.0	1.5	1.7	2.0	V
V_{T-}	Negative threshold voltage		V_{CC} = 5V		0.6	0.9	1.1	0.6	0.9	1.1	V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 5V		0.4	0.8		0.4	0.8		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20				μA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{T+} = 2V, V_{T-} = 0.6V	I_{OL} = 12mA			0.4			0.4	V
				I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{T+} = 2V, V_{T-} = 0.6V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{T+} = 2V, V_{T-} = 0.6V	V_O = 0.4V			−20			−20	μA
I_{OZH}				V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	LS310, LS340		17	27		17	27	mA
				LS341, LS344		18	35		18	35	
		Outputs Low		LS310, LS340		26	44		26	44	
				LS341, LS344		32	46		32	46	
		Outputs Disabled		LS310, LS340		29	50		29	50	
				LS341, LS344		34	54		34	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS310, LS340			LS341, LS344			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		19	25		19	25	ns
t_{PHL}				19	25		19	25	ns
t_{PZL}	Output Enable delay			32	40		25	40	ns
t_{PZH}				23	35		24	35	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	30		21	30	ns
t_{PHZ}				15	25		18	25	ns

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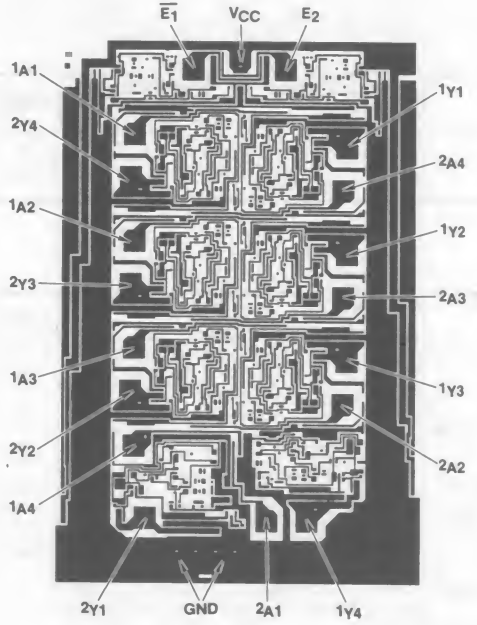
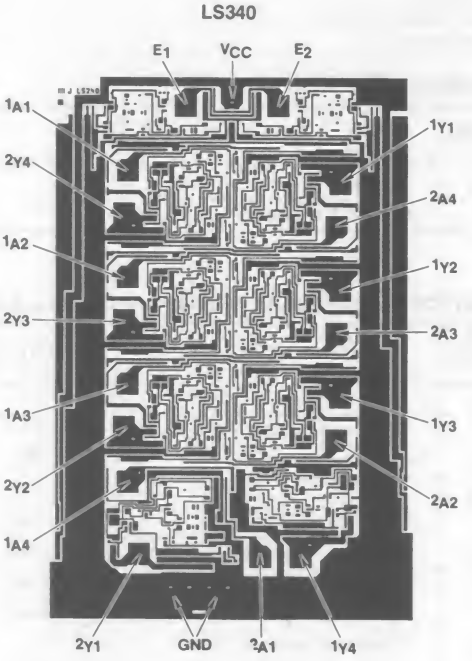
Die Configuration

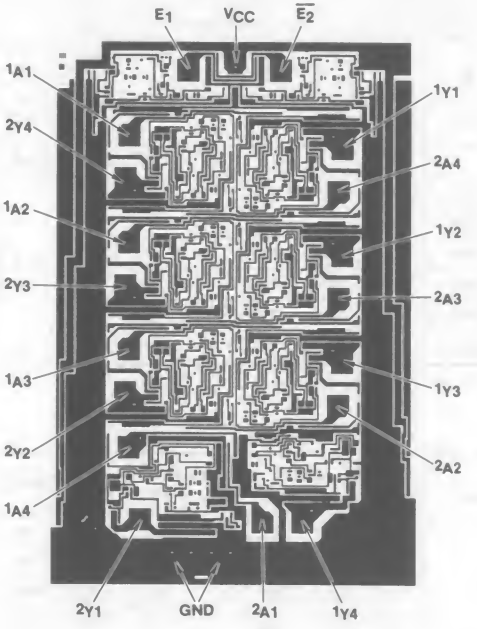
LS310



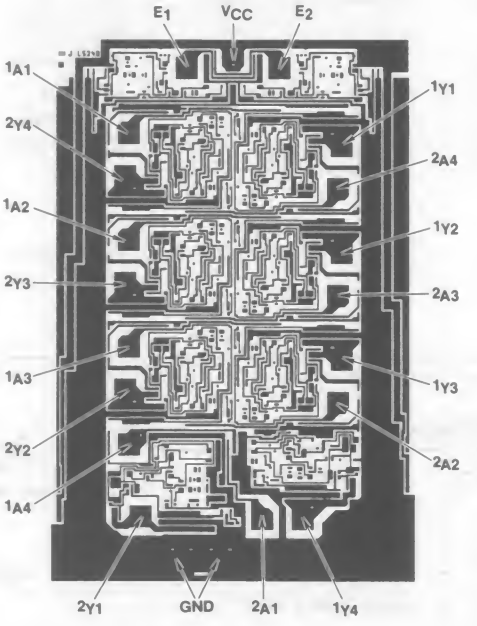
LS340



LS341

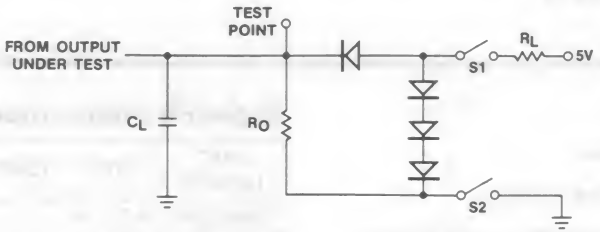


LS344



Die Size: 85 x 146 mil

Test Load



FOR THE 'LS310 SERIES
R_O = 5KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

NOTE THAT THE PROPAGATION DELAYS ARE MEASURED FROM THE INPUTS AT V_{T+} = 1.7V OR V_{T-} = 0.9V TO HE OUTPUT V_T = 1.3V

Octal Transceiver

SN54/74LS245

Features/Benefits

- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric -- equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS645 -- improved speed, I_{IL} and I_{OZL} specifications

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J, F, L, W	mil	Non-invert	LS
SN74LS245	N, J, L	com		

Description

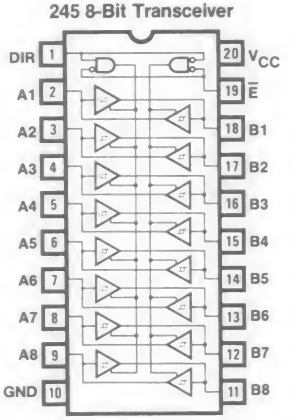
These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated. All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol



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Monolithic Memories MMI

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis ($V_{T_+}-V_{T_-}$) A or B		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
		DIR or $\overline{E}$		V_I = 7.0V			0.1			0.1	
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −12mA	2			2			
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−200			−200	μA
I_{OZH}				V_O = 2.7V			10			10	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open			48	70		48	70	mA
		Outputs Low				62	90		62	90	
		Outputs Disabled				64	95		64	95	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	A to B DIRECTION			B to A DIRECTION			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	12		8	12	ns
t_{PHL}				8	12		8	12	ns
t_{PZL}	Output Enable delay			27	40		27	40	ns
t_{PZH}				25	40		25	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

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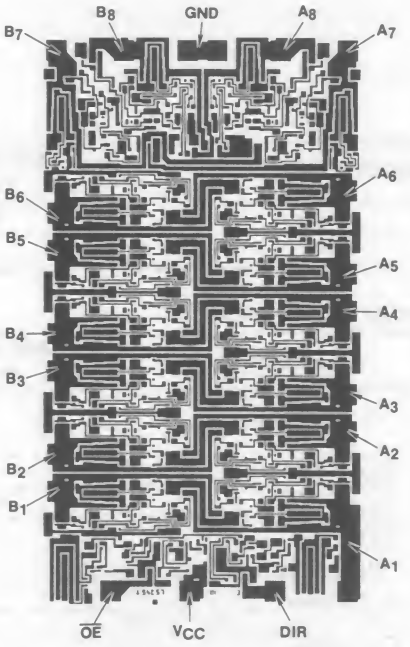
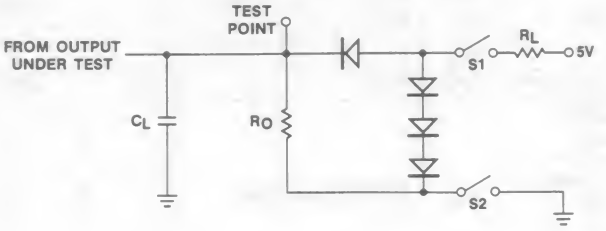
Die Configuration



Die Size: 65 x 111 mil

Test Load



R_O = 5KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

Octal Transceivers

SN54/74LS645 SN74LS645-1

Features/Benefits

- 3-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric — equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at I_{OL} = 48 mA

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J, F, L, W	mil	Non-invert	LS
SN74LS645	N, J, L	com		
SN74LS645-1	J, F, L	com		

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

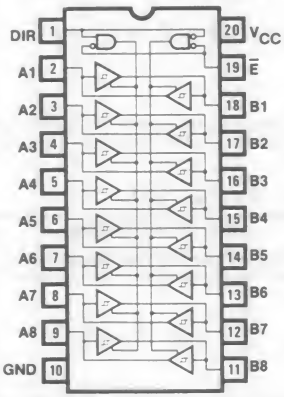
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated. All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol

645/645-1 8-Bit Transceiver



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Monolithic Memories MMI

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

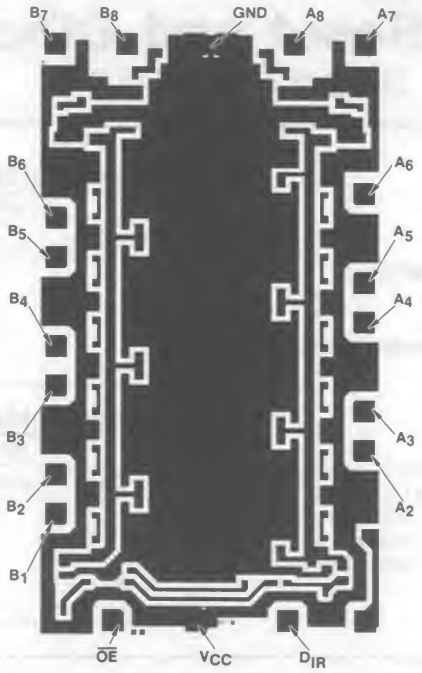
SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
	Hysteresis ($V_{T_+}-V_{T_-}$) A or B		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5V			0.1			0.1	mA
		DIR or $\overline{E}$		V_I = 7V							
V_{OL}	Low-level output voltage		V_{CC} = MIN,	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			V_{IL} = MAX,	I_{OL} = 24mA					0.35	0.5	
			V_{IH} = 2V	I_{OL} = 48mA†					0.4	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN,	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
			V_{IL} = MAX,	I_{OH} = −12mA	2						
			V_{IH} = 2V	I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX,	V_O = 0.4V			−400			−400	μA
I_{OZH}			V_{IL} = MAX, V_{IH} = 2V	V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open			48	70		48	70	mA
		Outputs Low				62	90		62	90	
		Outputs Disabled				64	95		64	95	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†This specification applies only to the SN74LS645-1.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

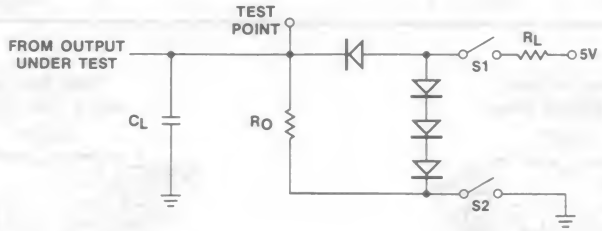
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	A TO B DIRECTION			B TO A DIRECTION			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	15		8	15	ns
t_{PHL}				11	15		11	15	ns
t_{PZL}	Output Enable delay			31	40		31	40	ns
t_{PZH}				26	40		26	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

Die Configuration



Die Size: 65 x 111 mil

Test Load



R_O = 5KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

13

Octal Registers With Master Reset and Clock Enable

SN54/74LS273 SN54/74LS377

Features

- 20-Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Ideal for Microprogram Instruction Registers
- Ideal for Microprocessor Interface
- Suitable for Pipeline Data Registers
- Useful in Timing, Sequencing, and Control Circuits
- 3 LS273s May Replace 4 LS174s
- 3 LS377s May Replace 4 LS378s

Description

These octal registers contain 8 D-type flip-flops and feature very low ICC (17 mA typ). The LS273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, $\overline{MR}$, is low. The LS377 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{CK\ EN}$, is low.

Function Table LS273

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0
H	H	X	Q_0

Function Table LS377

INPUTS			OUTPUT
CK EN	CLOCK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0
X	H	X	Q_0

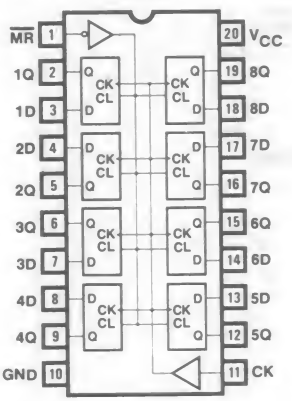
Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	CONTROL OPTION	POWER
SN54LS273 SN74LS273	J, F, L, W N, J, L	mil com	Non-invert	Register	Clear	LS
SN54LS377 SN74LS377	J, F, L, W N, J, L	mil com			Clock Enable	

Logic Symbols

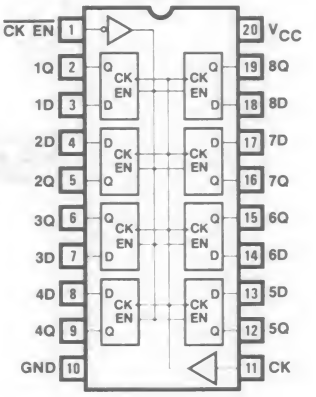
Octal Register with Master Reset

LS273



Octal Register with Clock Enable

LS377



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Monolithic Memories MMI

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of Clock/Master Reset	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	Data input	20↑			20↑			ns
		Reset inactive state ('LS273 only)	25↑			25↑			
		Clock enable active state ('LS377 only)	25↑			25↑			
		Clock enable inactive state ('LS377 only)	10↑			10↑			
t_h	Hold time	Data input	5↑			5↑			ns
		Clock enable ('LS377 only)	5↑			5↑			

↑↓The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 4mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −400μA	2.5	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current †	V_{CC} = MAX, Outputs open	LS273		17	27		17	27	mA
			LS377		17	28		17	28	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†I_{CC} is measured after first a momentary ground, and then 4.5V, is applied to clock, while the following other input conditions are held:
(a) for the 'LS273 — 4.5V on all data and master-reset inputs.
(b) for the 'LS377 — ground on all data and clock-enable inputs.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS273 MIN	LS273 TYP	LS273 MAX	LS377 MIN	LS377 TYP	LS377 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 2kΩ	30	40		30	40		MHz
t_{PLH}	Clock/Reset to output delay				27			27	ns
t_{PHL}					27			27	ns

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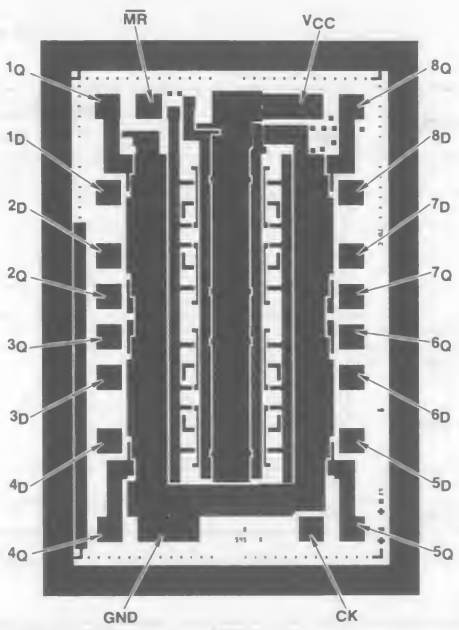
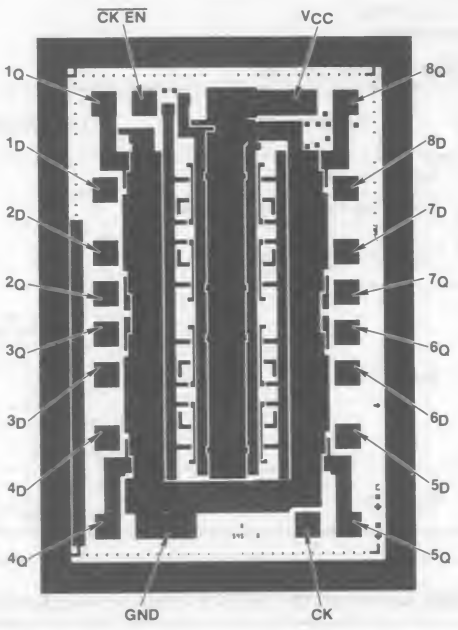
Die Configuration

LS273

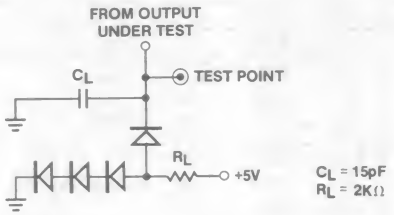


LS377



Die Size: 56 x 87 mil

Test Load



8-Bit Registers With Master Reset and Clock Enable

SN54/74S273 SN54/74S377

Features

- 20-Pin SKINNYDIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Ideal for Microprogram Instruction Registers
- Ideal for Microprocessor Interface
- Suitable for Pipeline Data Registers
- Useful in Timing, Sequencing, and Control Circuits
- 3 'S273s May Replace 4 'S174s
- 3 'S377s May Replace 4 'S378s/Am 25S07s

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTION	POWER
SN54S273 SN74S273	J,F,L,W N,J,L	mil com	Non-invert	Master Reset	S
SN54S377 SN74S377	J,F,L,W N,J,L	mil com		Clock Enable	

Description

These 8-bit registers contain 8 D-type flip-flops and feature very fast switching. The 'S273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, $\overline{MR}$, is low. The 'S377 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{CK\ EN}$, is low.

All the 8-bit devices are packaged in the popular 20-pin SKINNYDIP™.

Function Table 'S273

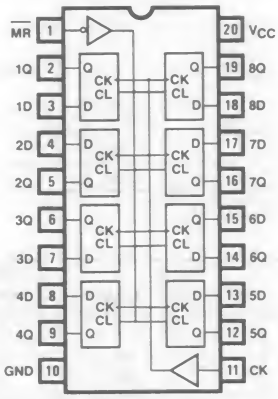
INPUTS			OUTPUT
$\overline{MR}$	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0
H	H	X	Q_0

Function Table 'S377

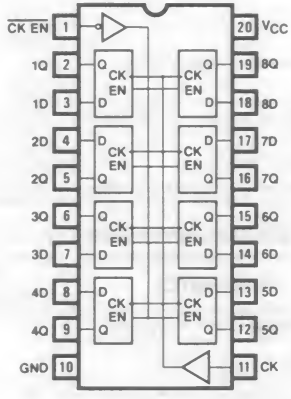
INPUTS			OUTPUT
$\overline{CK\ EN}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0
X	H	X	Q_0

Logic Symbols

8-Bit Register with Master Reset SN54/74S273



8-Bit Register with Clock Enable SN54/74S377



SKINNYDIP™ is a trademark of Monolithic Memories

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Absolute Maximum Ratings

Supply voltage V_{CC} ..... −0.5V to 7V
Input voltage ..... −1.5V to 5.5V
Off-state output voltage ..... −0.5V to 5.5V
Storage temperature range ..... −65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_W	Width of Clock	High-t_{WH}	1	7			7			ns
		Low-t_{WL}	1	7			7			
t_{WMR}	Width of Master Reset ('S273 only)	Low-t_{WMRL}	2	10			10			ns
t_{rec}		$\overline{MR}$ to CK ('S273 only)	2	7†			7†			ns
t_{su}	Setup time	Data input to CK	3	5†			5†			ns
		Low $\overline{CK\ EN}$ to CK ('S377 only)	4	9†			9†			
		High $\overline{CK\ EN}$ to CK ('S377 only)	4	9†			9†			
t_h	Hold time	Data input	3	3†			3†			ns
		Low $\overline{CK\ EN}$ to CK ('S377 only)	4	3†			3†			
		High $\overline{CK\ EN}$ to CK ('S377 only)	4	0†			0†			
T_A	Operating free air temperature			−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			-250			-250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.5	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'S273			150			150	mA
			'S377			160			160	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'S273 MIN	'S273 TYP	'S273 MAX	'S377 MIN	'S377 TYP	'S377 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω	75	110		75	110		MHz
t_{PLH}	Clock to output delay			6	15		6	15	ns
t_{PHL}				9	15		9	15	ns
t_{PHL}	Master Reset to output delay ('S273 only)			13	22				ns

CLOCK PULSE WIDTH AND CLOCK TO OUTPUT DELAYS

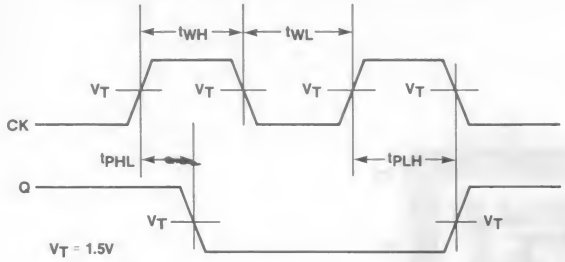


Figure 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME FOR 'S273

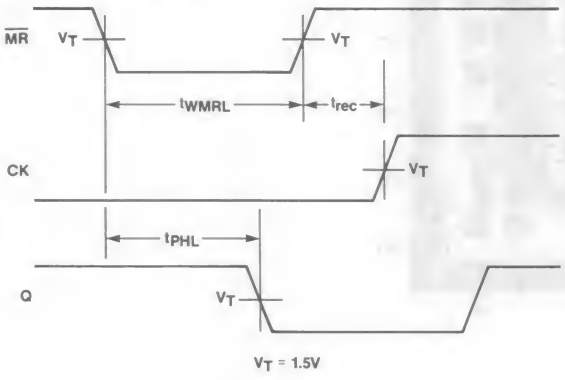


Figure 2

DATA SET-UP AND HOLD TIMES

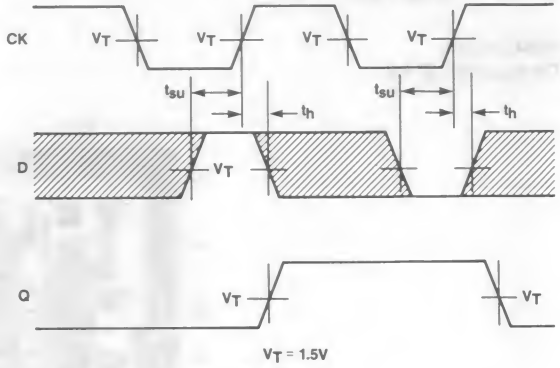


Figure 3

CLOCK ENABLE SETUP AND HOLD TIMES FOR 'S377

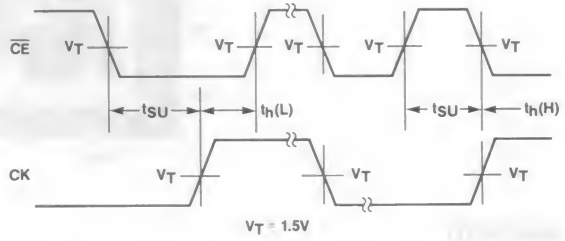
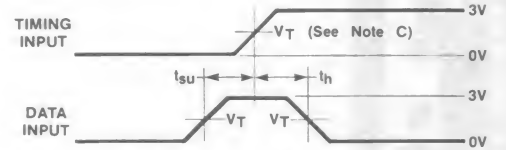
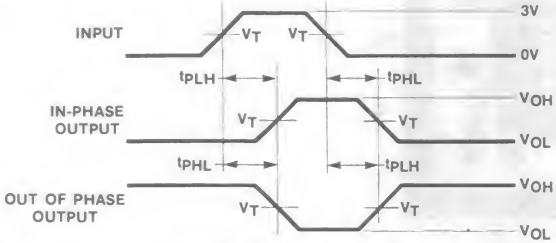


Figure 4

Test Waveforms

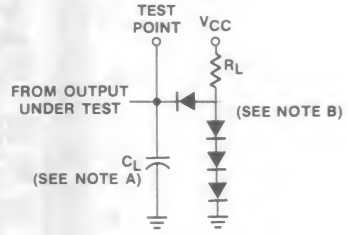


SETUP AND HOLD



PROPAGATION DELAY

Standard Test Load



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. V_T = 1.5V.
D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50Ω and: For Series 54/74S, t_R ≤ 2.5 ns, t_F ≤ 2.5 ns.

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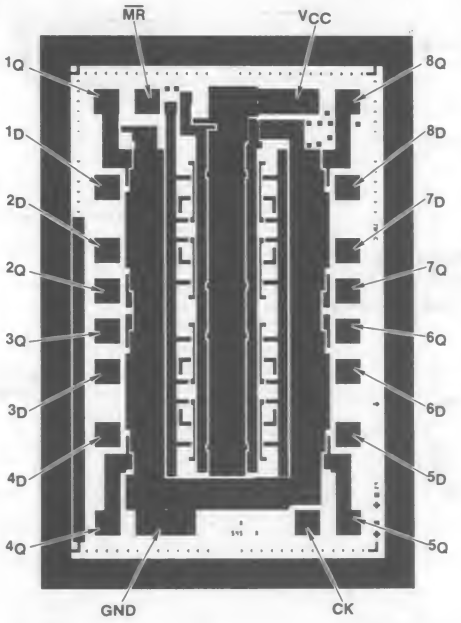
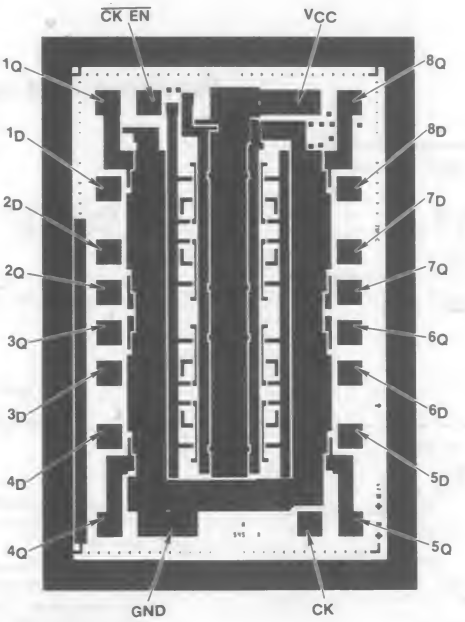
Die Configurations

SN54/74S273
Die Size: 56 x 87 mil



SN54/74S377
Die Size: 56 x 87 mil



Octal Latches, Octal Registers

SN54/74LS373 SN54/74S373
SN54/74LS374 SN54/74S374

Features/Benefits

- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373 SN74LS373	J,F,L,W N,J,L	mil com	Non-invert	Latch	LS
SN54LS374 SN74LS374	J,F,L,W N,J	mil com		Register	
SN54S373 SN74S373	J,F,L,W N,J,L	mil com		Latch	LS
SN54S374 SN74S374	J,F,L,W N,J	mil com		Register	

Description

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

373 Octal Latch

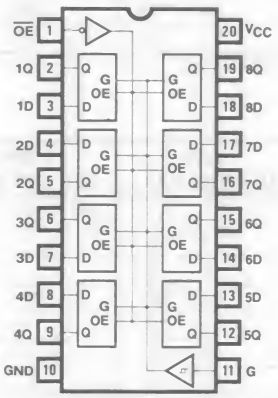
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

374 Octal Register

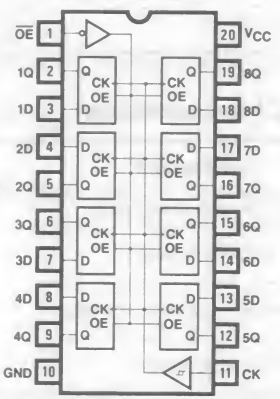
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Symbols

373 Octal Latch



374 Octal Register



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Absolute Maximum Ratings

Supply Voltage, VCC 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time	LS373	5↓				5↓		ns
		LS374	20↑			20↑			
t_h	Hold time	LS373	20↓			20↓			ns
		LS374		0↑		0↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS373		24	40		24	40	mA
			LS374		27	40		27	40	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS373 MIN	LS373 TYP	LS373 MAX	LS374 MIN	LS374 TYP	LS374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/Enable to output delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	ns
t_{PZL}	Output Enable delay			25	36		21	28	ns
t_{PZH}				15	28		20	28	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		14	25	ns
t_{PHZ}				12	20		12	20	ns

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Set up time	S373	0↓			0↓			ns
		S374	5↑			5↑			
t_h	Hold time	S373	10↓			10↓			ns
		S374	2↑			2↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	2.4	3.4					V
			I_{OH} = −6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S373		105	160		105	160	mA
			S374		90	140		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S373 MIN	S373 TYP	S373 MAX	S374 MIN	S374 TYP	S374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Enable to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

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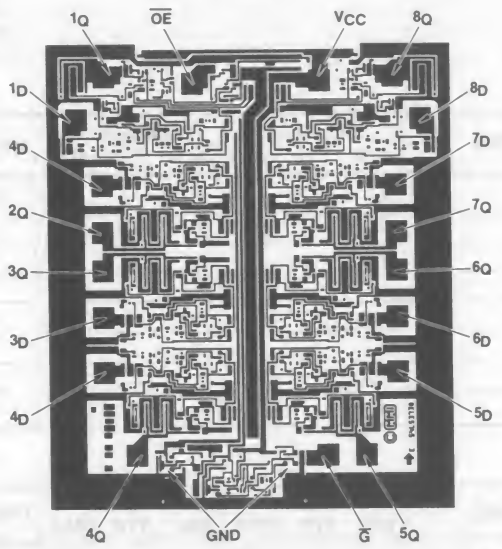
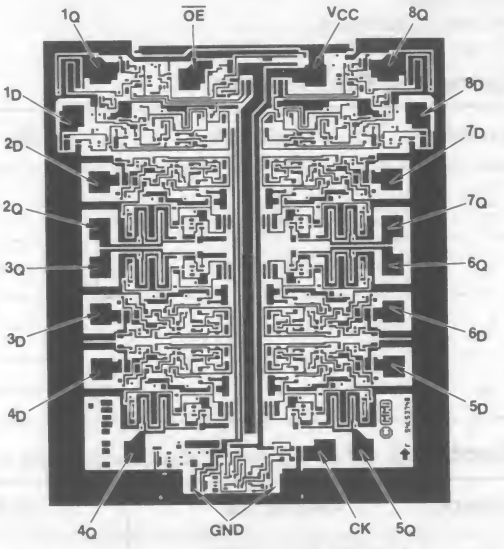
Die Configuration

LS374

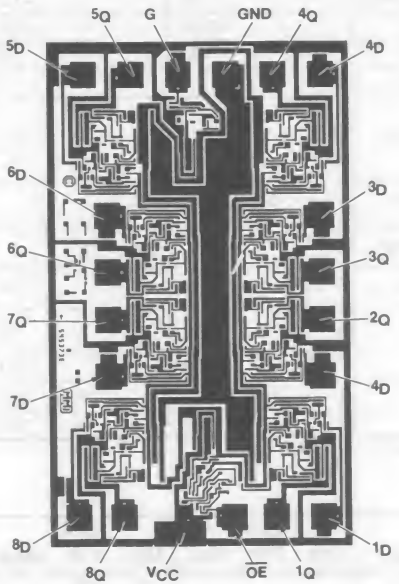


S374

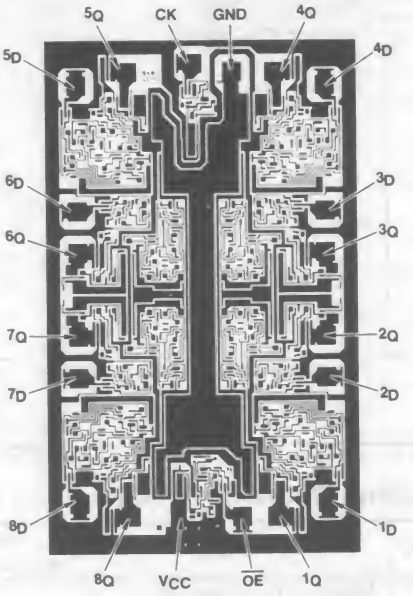


Die Size: 63 x 100 mil

LS373

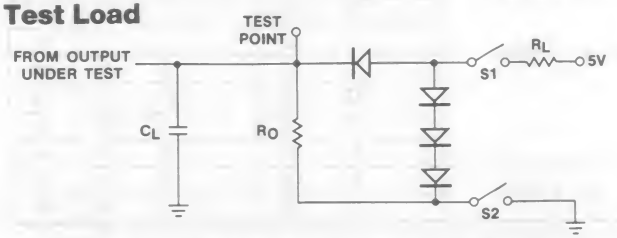


S373



Die Size: 76 x 87 mil

Test Load



FOR THE 'S373/374
R_O = 1KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

FOR THE 'LS373/374
R_O = 5KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

8-Bit Register With Clock Enable and Open-Collector Outputs
SN54/74S383

Features

- 20-Pin SKINNYDIP® Saves Space
- 8 Bits Matches Byte Boundaries
- Only Available TTL Open-Collector-Output Register
- Ideal for Certain Microprocessor System Buses
- Suitable for Pipeline Data Registers
- Excellent for Multiple, Physically-Separated Connections to Buses in Microprocessor-Based Systems
- Wired-Or or Wired-And Logic with Outputs

Description

This 8-bit register contains 8 D-type flip-flops and features very fast switching. The 'S383 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{CK\ EN}$, is low. Like other 8-bit interface devices, the 'S383 is packaged in the popular 20-pin SKINNYDIP.

Ordering Information

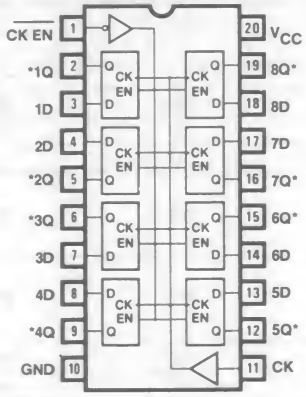
PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTIONS	POWER
SN54S383	J,F,L	mil	Non-invert	Clock Enable	S
SN74S383	N,J	com			

Function Table 'S383

INPUTS			OUTPUT
$\overline{CK\ EN}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0
X	H	X	Q_0

Logic Symbol

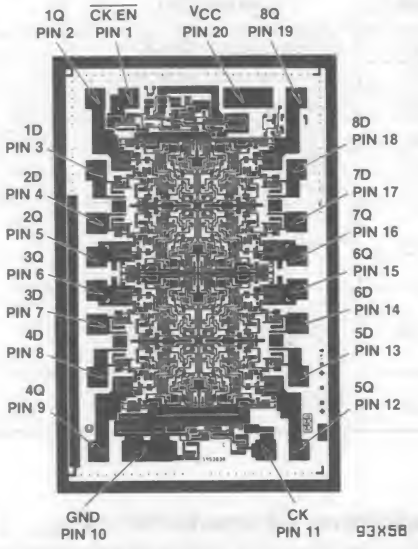
8-Bit Register with Clock Enable and Open-Collector Outputs
SN54/74S383



*Indicates Open-Collector Output

Die Configuration

SN54/74S383



Die Size 0.093" x 0.058"

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SKINNYDIP™ is a trademark of Monolithic Memories

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −0.5V to 7V
Input voltage ..... −1.5V to 5.5V
Off-state output voltage ..... −0.5V to 5.5V
Storage temperature range ..... −65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FIGURE	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.74	5	5.25	V
t_W	Width of Clock	High-t_{WH}	1	7			7			ns
		Low-t_{WL}	1	7			7			
t_{su}	Setup time	Data input to CK	2	5†			5†			ns
		Low $\overline{CK\ EN}$ to CK	2	9†			9†			
		High $\overline{CK\ EN}$ to CK	2	9†			9†			
t_h	Hold time	Data input	2	3†			3†			ns
		Low $\overline{CK\ EN}$ to CK	2	3†			3†			
		High $\overline{CK\ EN}$ to CK	2	0†			0†			
T_A	Operating free air temperature			−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			-250			-250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 24mA			0.5			0.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	V_{OH} = 5.5			250			250	μA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	Outputs HIGH			160			160	mA
			Outputs LOW			160			160	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'S383 MIN	'S383 TYP	'S383 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15 pF R_L = 280Ω	75	110		MHz
t_{PLH}	Clock to output delay			10	17	ns
t_{PHL}				14	22	ns

CLOCK PULSE WIDTH AND
CLOCK TO OUTPUT DELAYS

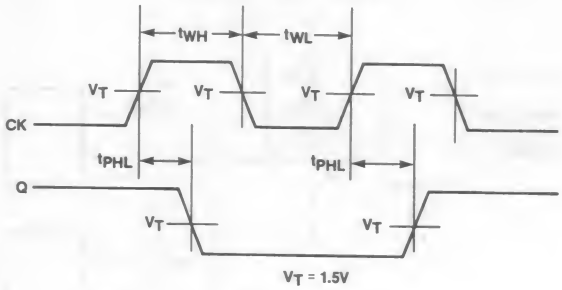


Figure 1

DATA AND CLOCK ENABLE
SETUP AND HOLD TIMES

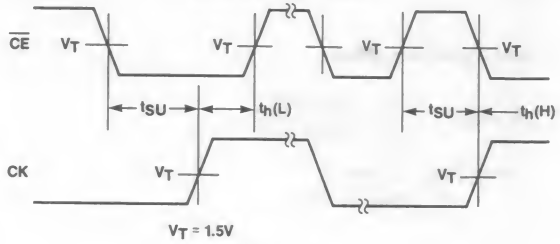
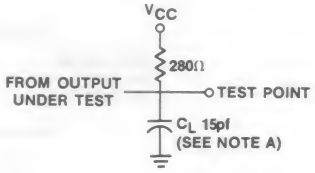


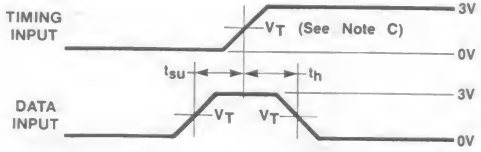
Figure 2

Standard Test Load

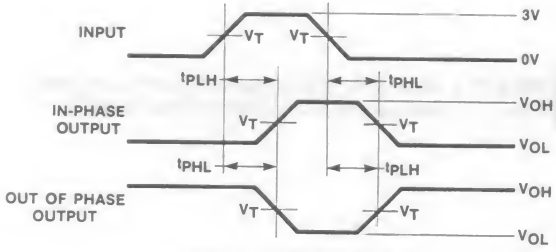


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

Test Waveforms



SETUP AND HOLD



PROPAGATION DELAY

A. Includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and:
For Series 54/74S, t_R ≤ 2.5 ns, t_F ≤ 2.5 ns.

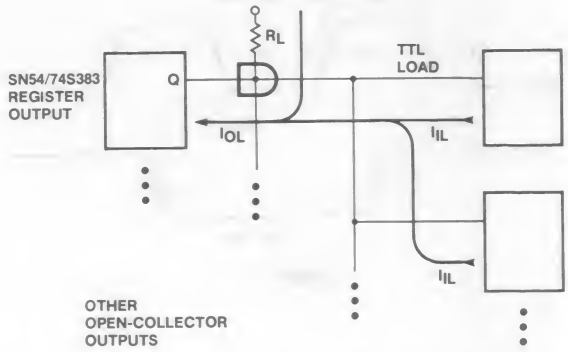
E. V_T = 1.5V

Open Collector Bus Application Information For Determination of R_L For Wired-And Applications

1. **CALCULATE R_L(Min):**

$$R_L(\text{Min}) = \frac{V_{CC} - V_{OL}(\text{Max})}{I_{OL} - (\text{TOTAL } I_{IL})}$$

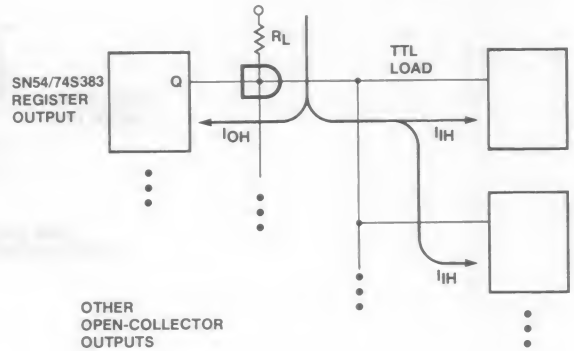
where I_{OL} = 24 mA at
V_{OL}(Max) = 0.5 V



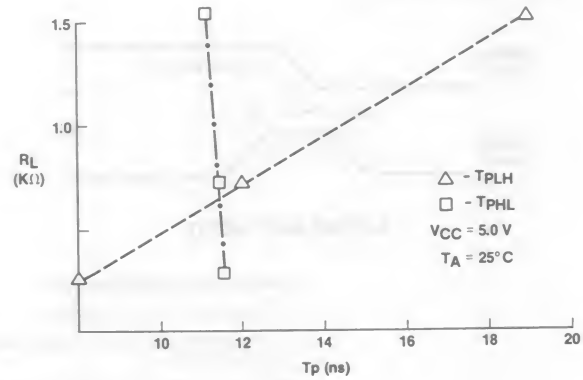
2. **CALCULATE R_L(Max):**

$$R_L(\text{Max}) = \frac{V_{CC} - V_{OH}(\text{Min})}{(\text{TOTAL } I_{OH} + \text{TOTAL } I_{IH})}$$

where I_{OH} = 250 μA at
V_{OH}(Min) = 2.5V



3. **SELECT** a value for R_L in the range of R_L(Min) to R_L(Max), based on power consumption and speed requirements:



R_L vs. Tp FOR SN54/74S383

8-Bit Latches, Octal Registers With Inverting Outputs

SN54/74LS533 SN54/74S533
SN54/74LS534 SN54/74S534

Features/Benefits

- Inverting outputs
- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS373/4 or SN54/74S373/4 — can be direct replacement when bus polarity must be changed

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion an in interfacing the Am2901A 4-Bit Slice to an assertive-low bus.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
54LS533 74LS533	J,F,W N,J	mil com	Invert	Latch	LS
54LS534 74LS534	J,F,W N,J	mil com		Register	
54S533 74S533	J,F,W N,J	mil com		Latch	S
54S534 74S534	J,F,W N,J	mil com		Register	

Function Tables

533 Octal Latch (Inverting)

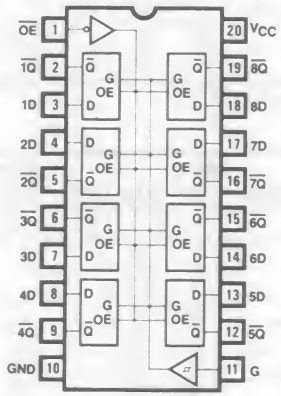
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

534 Octal Register (Inverting)

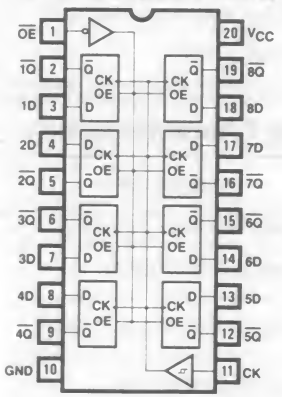
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

Logic Symbols

533 Octal Latch (Inverting)



534 Octal Register (Inverting)



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Absolute Maximum Ratings

Supply Voltage, VCC 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Set up time	LS533	0↓			0↓			ns
		LS534	20↑			20↑			
t_h	Hold time	LS533	10↓			10↓			ns
		LS534	0↑			0↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V						−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS533		36	48		36	48	mA
			LS534		27	48		27	48	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS533 MIN	LS533 TYP	LS533 MAX	LS534 MIN	LS534 TYP	LS534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			17	25				ns
t_{PHL}				12	25				ns
t_{PLH}	Clock/Enable to output delay			20	35		19	30	ns
t_{PHL}				18	35		15	30	ns
t_{PZL}	Output Enable delay			25	36		21	30	ns
t_{PZH}				17	30		20	30	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	29		18	29	ns
t_{PHZ}				16	24		16	24	ns

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Set up time	S533	0↓			0↓			ns
		S534	5↑			5↑			
t_h	Hold time	S533	10↓			10↓			ns
		S534	5↑			5↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	2.4	3.4					V
			I_{OH} = −6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S533		105	160		105	160	mA
			S534		90	140		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S533 MIN	S533 TYP	S533 MAX	S534 MIN	S534 TYP	S534 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

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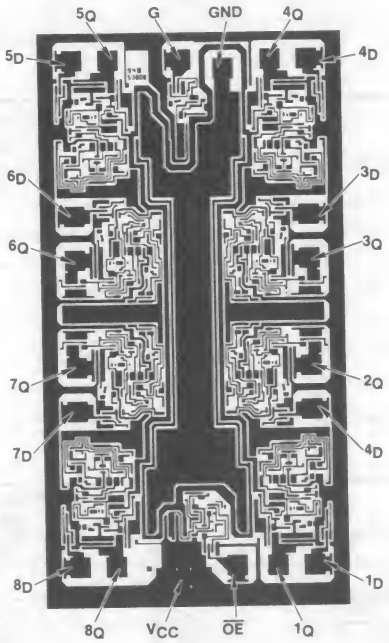
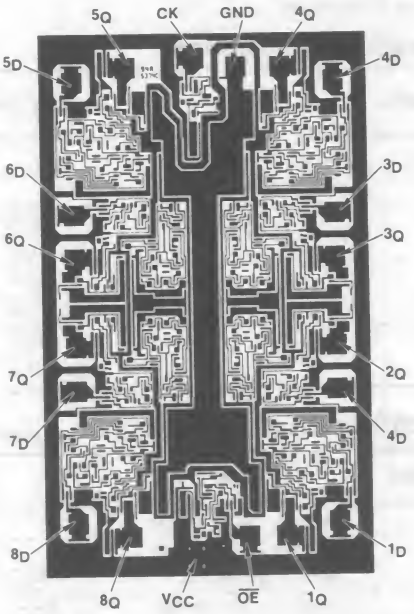
Die Configuration

S533

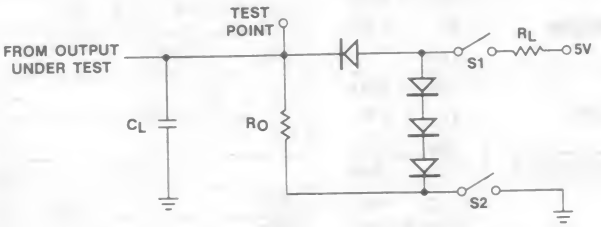


S534



Die Size: 106 x 66 mil

Test Load



FOR THE 'S533/534
R_O = 1KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

FOR THE 'LS533/54
R_O = 5KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

8-Bit Latches, Octal Registers With 32mA Outputs

SN74S531 SN74S532

Features/Benefits

- 32mA I_{OL}
- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S373/4 — can be direct replacement when high drive capability is required

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S531	N,J	com	Non-invert	Latch	S
SN74S532	N,J	com		Register	

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365A, 366A, 367A, 368A, hex buffers.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

531 8-Bit Latch

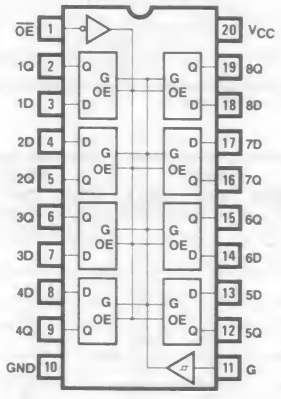
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

532 8-Bit Register

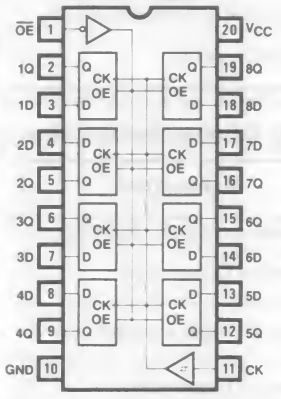
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Symbols

531 8-Bit Latch



532 8-Bit Register



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Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S531	0↓	0↓		ns
		S532	5↑	5↑		
t_h	Hold time	S531	10↓	10↓		ns
		S532	2↑	2↑		

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX,		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S531		105	160	mA
			S532		90	140	

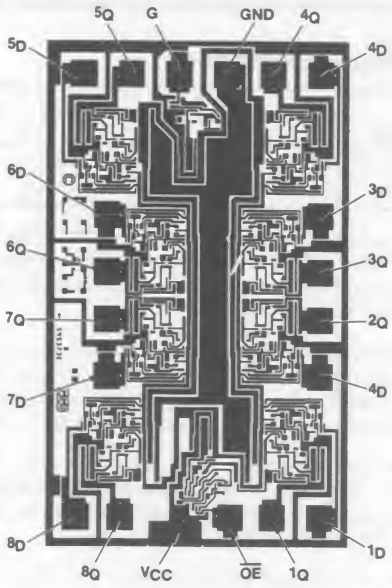
*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S531 MIN	S531 TYP	S531 MAX	S532 MIN	S532 TYP	S532 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Enable to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns

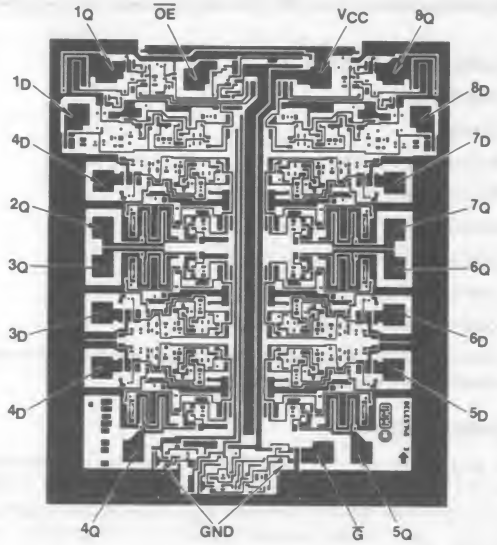
Die Configuration

S531



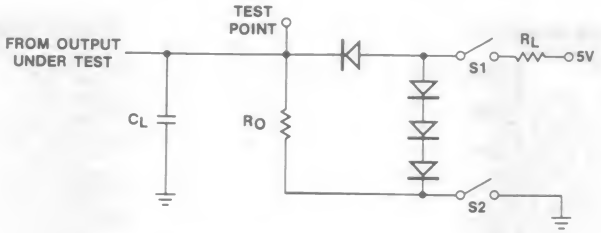
Die Size: 63 x 100 mil

S532



Die Size: 76 x 87 mil

Test Load



R_O = 1KΩ
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

13

8-Bit Latches, Octal Registers With Inverting, 32 mA Outputs

SN74S535 SN74S536

Features/Benefits

- Inverting outputs
- 32 mA I_{OL}
- 3-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8 bits matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S533/4 — can be direct replacement when hi-drive capability is required

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA, also inverting outputs instead of the standard non-inverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, hex buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-Bit Slice to an active low bus.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S535	N,J	com	Invert	Latch	S
SN74S536	N,J	com		Register	

Function Tables

535 8-Bit Latch (Inverting)

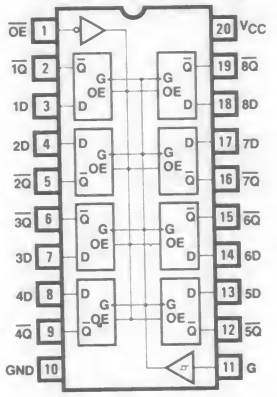
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

536 8-Bit Register (Inverting)

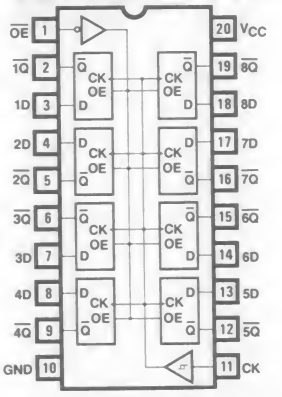
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

Logic Symbols

535 8-Bit Latch (Inverting)



536 8-Bit Register (Inverting)



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Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S535	0↓	0↓		ns
		S536	5↑	5↑		
t_h	Hold time	S535	10↓	10↓		ns
		S536	5↑	2↑		

Electrical Maximum Ratings Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC}		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S535		105	160	mA
			S536		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

Switching Charcteristics V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S535 MIN	S535 TYP	S535 MAX	S536 MIN	S536 TYP	S536 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

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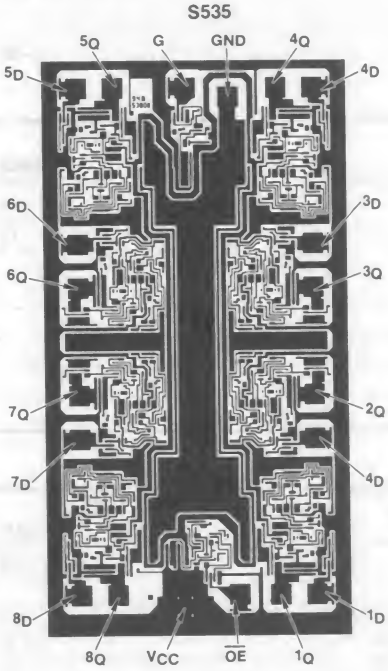
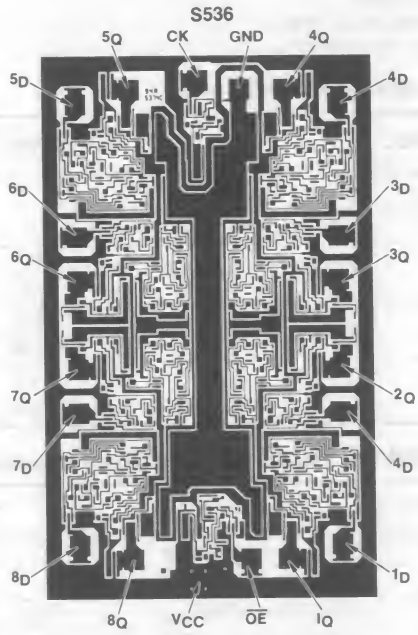
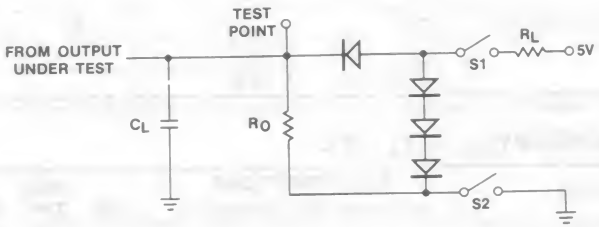
Die Configuration





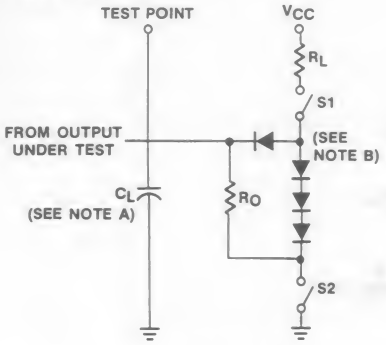
Die Size: 106 x 66 mil

Test Load

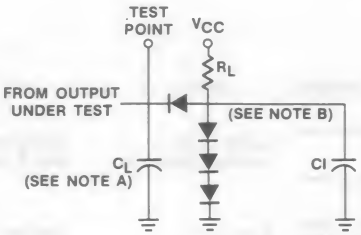


R_O = 1 K Ω
R_L, C_L ARE SPECIFIED BY THE SWITCHING CHARACTERISTICS TABLE

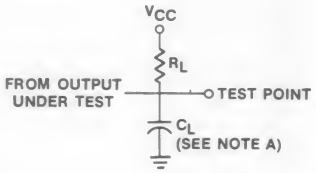
Test Load



LOAD CIRCUIT FOR THREE-STATE OUTPUTS

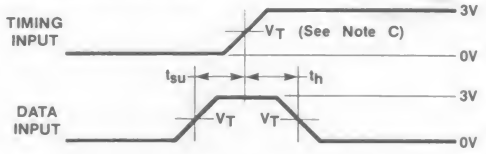


LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

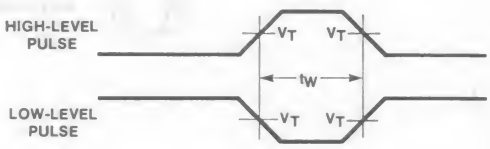


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

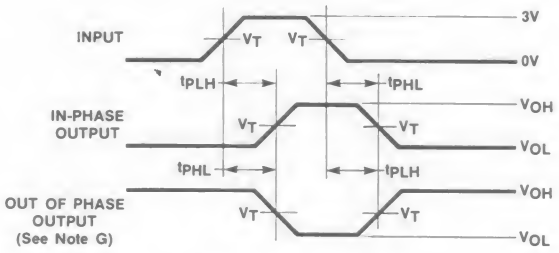
Test Waveforms



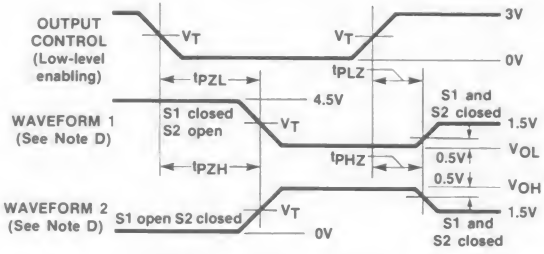
SETUP AND HOLD



PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE

13

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S, R_O = 1K, V_T = 1.5V.
For Series 54/74LS, R_O = 5K, V_T = 1.3V excepting 54/74LS310, 340, 341, 344.
For Series 54/74LS310, 340, 341, 344 R_O = 5K, $V_T = V_{T+}$ = 1.7V for low to high input transition.
For Series 54/74LS310, 340, 341, 344 R_O = 5K, $V_T = V_{T-}$ = 0.9V for high to low input transition.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ns, $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

Octal Dynamic-RAM Driver with 3-state Outputs

SN54/74S700/-1 SN54/74S730/-1 SN54/74S731/-1 SN54/74S734/-1

FOR MORE DETAIL SEE SECTION 10

Features/Benefits:

- Provides MOS voltage levels for 16 K and 64 K D-RAMs
- Undershoot of low-going output is less than -0.5 V
- Large capacitive drive capability
- Symmetric rise and fall times due to balanced output impedance
- Glitch-free outputs at power-up and power-down
- 20-pin SKINNYDIP® saves space
- 'S730/734 are exact replacement for the Am2965/66
- 'S700/730/731/734 are pin-compatible with 'S210/240/241/244, and can replace them in many applications
- 'S700-1/730-1/731-1/734-1 have a larger resistor in the output stage for better undershoot protection
- Commercial devices are specified at $V_{CC} \pm 10\%$.

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S700/-1	J,F,L	Mil	High-Low	Invert	S
SN74S700/-1	N,J	Com			
SN54S730/-1	J,F,L	Mil	Low		
SN74S730/-1	N,J	Com			
SN54S731/-1	J,F,L	Mil	High-Low	Non-Invert	
SN74S731/-1	N,J	Com			
SN54S734/-1	J,F,L	Mil	Low		
SN74S734/-1	N,J	Com			

Description:

The 'S700, 'S730, 'S731, and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S700 and 'S730 are inverting drivers and the 'S731 and 'S734 are non-inverting drivers. The 'S700/731 are pin-compatible with the 'S210/241 and have complementary enables. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular octal buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S700, 'S730, 'S731, and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC} - 1.15 volts, limit undershoot to 0.5V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

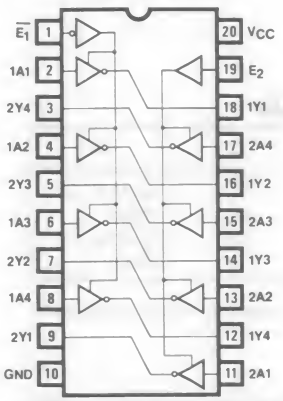
For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S700-1, 'S730-1, 'S731-1, 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S700-1 series.

A typical fully-loaded-board dynamic-RAM array consists of 4 banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50pf and 500pf load capacitances, and the commercial-range specifications are extended to $V_{CC} \pm 10\%$.

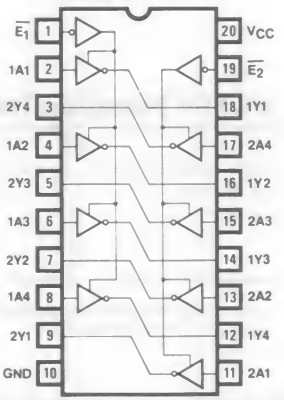
All of the octal devices are packaged in the popular 20-pin SKINNYDIP™

Logic Symbols

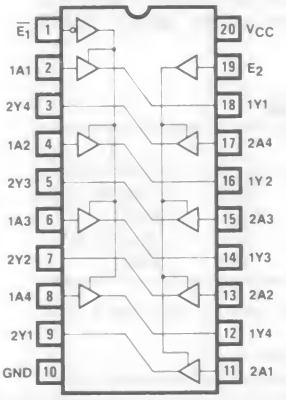
'S700/-1



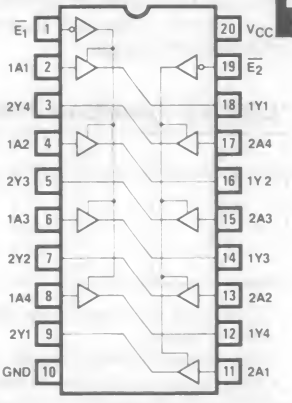
S730 (AM2965)
S730-1



'S731/-1



S734 (AM2966)
S734-1



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2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

8-Bit Latches/ Registers with Readback

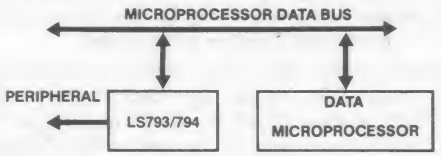
SN54/74LS793 SN54/74LS794

Features

- **I/O port configuration enables output data back onto input bus**
- **20-pin SKINNYDIP® saves space**
- **8 bits matches byte boundaries**
- **Ideal for microprocessor interface**

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an 'LS793/4, for verification and/or updating.



The data is loaded in the registers on the low-to-high transition of the clock (CK), from the 'LS794. The data is passed through the 'LS793 when the gate (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{OE}$ is used to enable data on D0-D7. When $\overline{OE}$ is low the output of the latches/registers is enabled on D0-7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OE}$ is high, D0-7 are inputs to the latches/registers configuring D as an input bus.

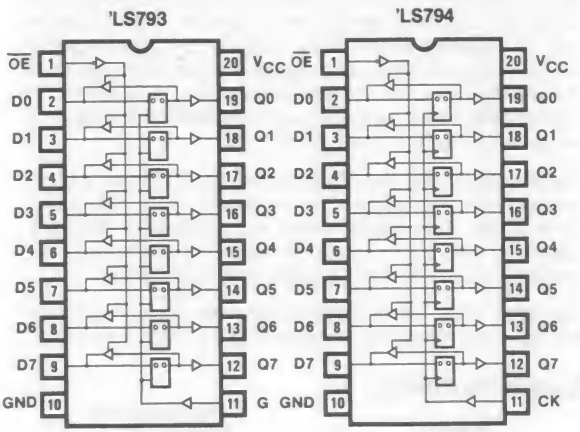
The output drive of these commercial parts for any output pin is I_{OL} = 24 mA. They are available in the popular 20-pin SKINNYDIP® package.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS793 SN74LS793	J,F,L N,J,L	mil com	Non-invert	Latch	LS
SN54LS794 SN74LS794	J,F,L N,J,L	mil com	Non-invert	Register	LS

* W (Cerpak), D (Side-brazed ceramic dual-in-line) packages are also available for both parts.

Logic Symbol



'LS793 Function Table

G	OE	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

'LS794 Function Table

CK	$\overline{OE}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

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Monolithic Memories

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 7 V
Off-state output voltage ..... 5.5 V
Storage temperature range ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature			−55		125	0		75	°C
t_w	Width of Clock/Gate	High		15			15			ns
		Low		15			15			
t_{su}	Setup time		'LS793	15↓			10↓			ns
			'LS794	15↑			15↑			
t_h	Hold time		'LS793	10↓			10↓			
			'LS794	0↑			0↑			

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERIAL MIN	COMMERIAL TYP	COMMERIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−250			−250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			40			40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−250		−250		μA
I_{OZH}			V_O = 2.7V			40			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'LS793			120			120	mA
			'LS794			120			120	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

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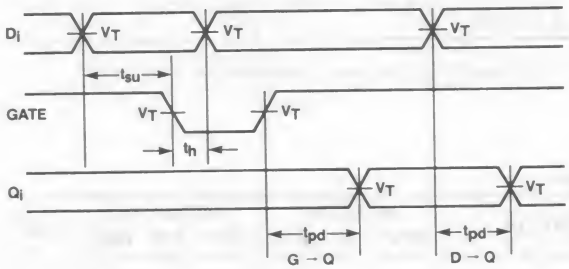
Switching Characteristics V_{CC} = 5V, T_A = 25°C

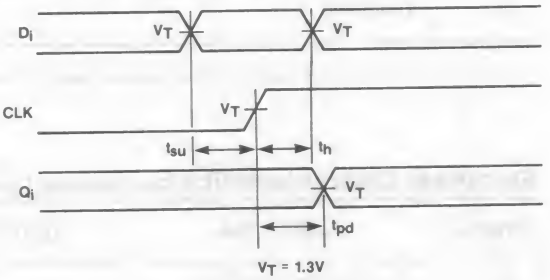
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'LS793 MIN	'LS793 TYP	'LS793 MAX	'LS794 MIN	'LS794 TYP	'LS794 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45pF R_L = 280 Ω				35	50		MHz
t_{PLH}	Data to output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/gate to output delay			17	25		9	20	ns
t_{PHL}				12	25		14	20	ns
t_{PZL}	Output enable delay†			15	20		15	20	ns
t_{PZH}				11	20		11	20	ns
t_{PLZ}	Output disable delay†	C_L = 5pF R_L = 280 Ω		8	20		8	20	ns
t_{PHZ}				9	20		9	20	ns

† For the 'LS793, G should remain LOW during these tests.

'LS793 Timing Diagrams



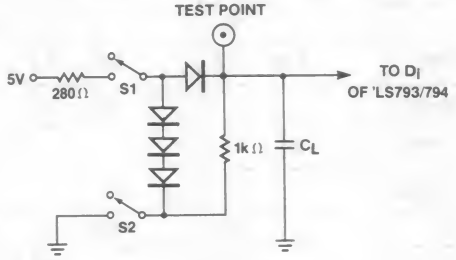
'LS794 Timing Diagrams



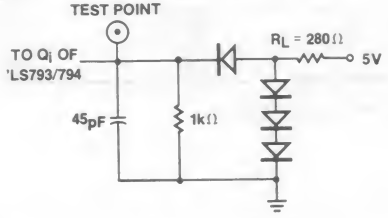
The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Test Loads

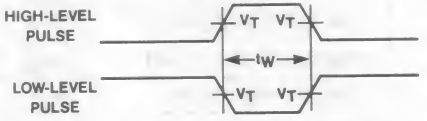
FOR D OUTPUTS-ENABLE AND DISABLE



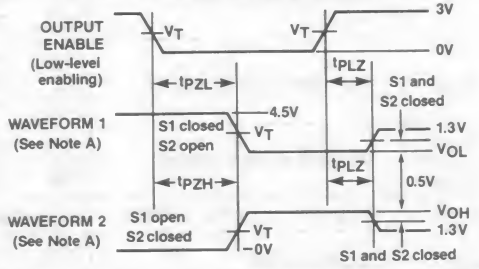
FOR Q OUTPUTS



PULSE WIDTH



ENABLE AND DISABLE WAVEFORMS

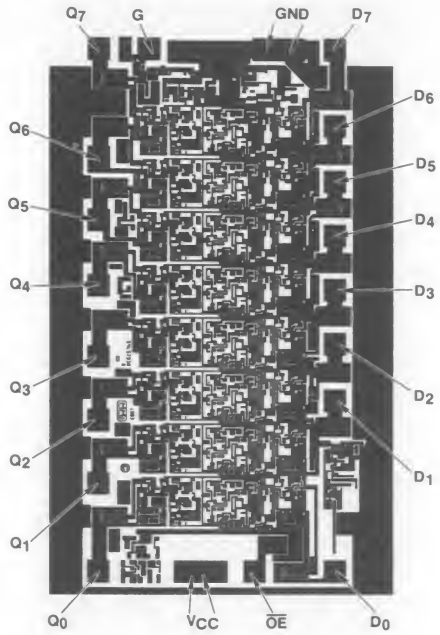


For the 'LS793, the latch control "G" should be low while testing the enable and disable times, so that the output (Q) does not change. (V_T = 1.3V).

NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

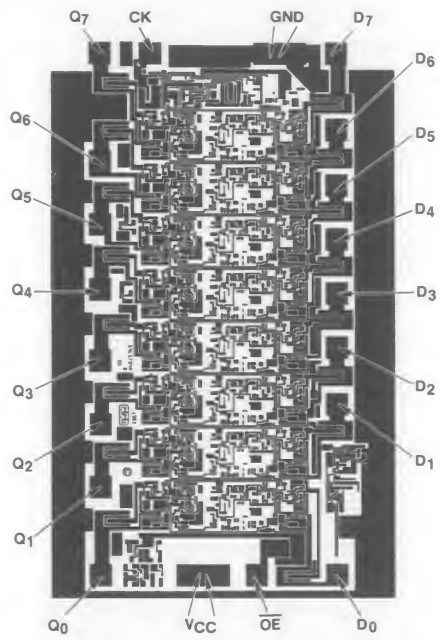
Die Configuration

SN54/74LS793



Die Size: 79 x 127 mil

SN54/74LS794



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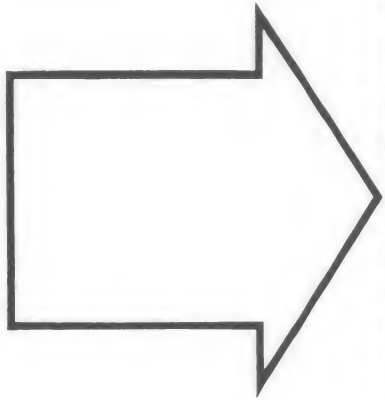


Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IC}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_T

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Positive-going threshold voltage, V_{T+}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

Truth Table Explanations

H	=	high level (steady-state)
L	=	low level (steady-state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.

Clock Frequency

Maximum clock frequency, f_{max}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}

The current into * an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, I_{CEX}

The high-level leakage current of an open collector output.

Low-level input current, I_{IL}

The current into * an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}

The current into * an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into * an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into * the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

Hold Time

Hold time, t_h

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices. t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{AA} is the address (to output) access time of memory devices.

Pulse Width

Pulse width, t_w

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Programming Input Formats

Monolithic Memories can program your ROM or PROM from input data in any of several types: truth table, punched cards, paper tape or preprogrammed ROM or PROM. However, the preferred input data for PROMs is paper tape and for ROMs punched cards.

Truth Table Inputs

Devices are programmed at our facility from Monolithic Memories truth table forms (available on request). For customers desiring to make their own forms, examples are shown below:

4-BIT OUTPUT

WORD NUMBER	PIN	OUTPUTS 10 O_4	11 O_3	12 O_2	13 O_1
0		H	H	H	L
1		L	H	L	H
.		.	.	.	.
.		.	.	.	.
255		L	H	H	H

8-BIT OUTPUT

WORD NUMBER	PIN	17 O_8	16 O_7	15 O_6	14 O_5	13 O_4	11 O_3	10 O_2	9 O_1
0		H	H	H	L	H	L	H	H
1		L	H	L	H	L	H	L	H
.		.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.
511		L	H	H	H	H	H	H	L

NOTE: A high voltage on the data out lines is signified by an "H." A low voltage on the data out lines is signified by an "L." The word number assumes positive logic on the address pins, so for example, word 1023 = HHHHHHHHHH'.

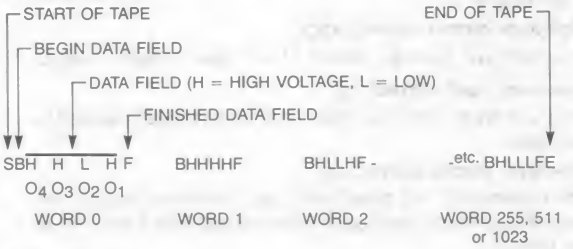
Paper Tape Format Inputs

Truth tables can also be sent Monolithic Memories in an ASCII tape in either a 7 or 8 level format. Send information air mail or TWX 910-339-9224. The tape reading equipment at Monolithic Memories only recognizes ASCII characters S, B, H, L, F and E interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 31, 255, 511 or 1023 respectively.

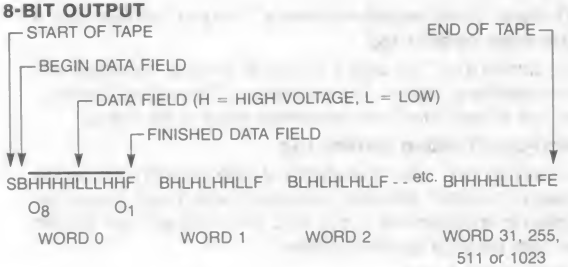
In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O_4, O_3, O_2, O_1, not O_1, O_2, O_3, O_4.

A typical list of characters and their machine interpretations is shown below:

4-BIT OUTPUT



8-BIT OUTPUT



The required heading information at the beginning of the tape is as follows:

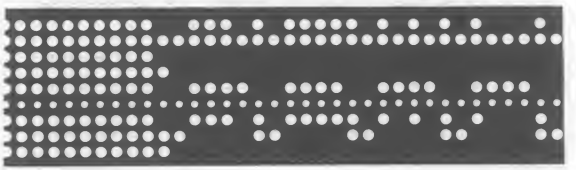
CUSTOMER'S NAME AND PHONE _____
CUSTOMER'S TWX NUMBER _____
PURCHASE ORDER NUMBER _____
MONOLITHIC MEMORIES' PART NUMBER _____
CUSTOMER SYMBOLIZED PART NUMBER _____
TRUTH TABLE NUMBER _____
NUMBER OF TRUTH TABLES _____
TOTAL NUMBER OF PARTS _____
NUMBER OF PARTS OF EACH TRUTH TABLE _____
25 BELL OR RUBOUT CHARACTERS _____

An example is shown below for a 256 x 4 PROM (6300)

SCOTT ELECTRONICS 408 426-6134
TWX 911-338-9225
PO142
6300
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 level
TWX



ROM Programming Punched Card

ROMs can be programmed using several input methods. These are truth table, punched cards in the format shown below, paper tape in the same format as cards, and paper tape in the ASCII BHLF format of the equivalent PROM.

Punched Card or Tape Input

First card or line (80 columns max.): enter Company Name, Part Number, Data, Number of "L's" in Pattern.
(Free Form Entry: no commas; Paper Tape Format: terminate each line with carriage return and linefeed).

Hexadecimal Format

In this format the heading required is identical to the BHLF format but the data is different. Instead of an "S," the hexadecimal data begins with the SOH character (control A). The data is then represented by the hexadecimal character (0-9 and A-F) which represents the output data of address 0, followed by a space. Next comes the output data of address 1 followed by a space, etc. The character ETX (control C) is used to end the data. Carriage return and the line feed may be included to format the data when the tape is printed.

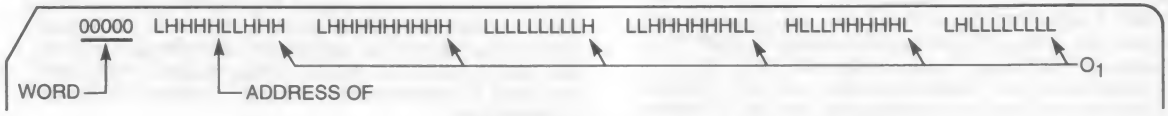
CARD 1

COMPANY NAME CX 1816—2052 7—12—70 L = 796

2nd Card Or Line thru Last (80 Columns Max.)
ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5

Enter First Data Field	(O_{10}—O_1) in Columns 8 thru 17
Enter Second Data Field	(O_{10}—O_1) in Columns 19 thru 28
Enter Third Data Field	(O_{10}—O_1) in Columns 30 thru 39
Enter Fourth Data Field	(O_{10}—O_1) in Columns 41 thru 50
Enter Fifth Data Field	(O_{10}—O_1) in Columns 52 thru 61
Enter Sixth Data Field	(O_{10}—O_1) in Columns 63 thru 72

CARD 2



NOTE: Output 1 (O_1) is always in cols. 17,28,39,50,61,72

CARD 3

00006 LHLLLLLLLL HLHHHHHHHH LHLHHLLHHL HLHHHHLLLL LLLLHHHLHL HLHHHHHLH

LAST CARD

01020 HLLLLLLLL HHLHHHHHLL LHLHLHLHLH LLHLHLLHHH

14

NOTES:

1. Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.
2. Regardless of the number of outputs which a particular ROM has, the data for a specific output always goes in a specific column.

Output 1 (01)	Columns 17, 28, 39, 50, 61, 72
Output 2 (02)	Columns 16, 27, 38, 49, 60, 71
Output 3 (03)	Columns 15, 26, 37, 48, 59, 70
Output 4 (04)	Columns 14, 25, 36, 47, 58, 69
Output 5 (05)	Columns 13, 24, 35, 46, 57, 68
Output 6 (06)	Columns 12, 23, 34, 45, 56, 67
Output 7 (07)	Columns 11, 22, 33, 44, 55, 66
Output 8 (08)	Columns 10, 21, 32, 43, 54, 65
Output 9 (09)	Columns 9, 20, 31, 42, 53, 64
Output 10 (10)	Columns 8, 19, 30, 41, 52, 63

3. 0 and 1 may replace L and H, but the customer must define for MMI whether 0 = L or 0 = H.

AVAILABLE LITERATURE

IdeaLogic Brochure
Military Products Division Brochure
PAL Engineering Reference Card
PROM Cross Reference Guide
Reliability Report
Reliability Report (Plastic Packages)
SHRP—Super High Reliability Products Brochure
Testing Your PAL Devices

HANDBOOKS

PAL Handbook
System Design Handbook

APPLICATION NOTES

AN-100
PROMs, PALs, FIFOs, AND MULTIPLIERS TEAM UP TO IMPLEMENT SINGLE-BOARD HIGH-PERFORMANCE AUDIO SPECTRUM ANALYZER
(System Design Handbook, Section 1)

The teamwork of a logic device (PAL), a memory device (PROM), a buffer (FIFO), and multiplier chips makes cost-effective and efficient digital signal processing (DSP). This idea is illustrated through the audio spectrum analyzer, but is not limited to that use. Creative designers will soon develop low cost/high performance architectures that can perform as well as the example given.

AN-103
A DEDICATED MULTIPLIER/DIVIDER SPEEDS UP MULTIPLICATION AND DIVISION FOR 8-BIT MICROPROCESSORS

This paper presents a dedicated chip to upgrade the performance level of the 8-bit microprocessor. Implementation with the Intel 8085 and Motorola 6800 microprocessors are examined in detail. This multiplier diminishes the software overhead and accelerates the execution time by a FACTOR OF 20. With minimal interfacing of Monolithic Memories' 74S508 the 8-bit microprocessor can use its hardware to do the "number crunching." Examples and block diagrams clarify the process.

AN-104
IMPLEMENTING A VIDEO CONTROLLER USING PROGRAMMABLE ARRAY LOGIC
(PAL Handbook, Section 7)

A video controller is needed to bridge the outside world (such as a keyboard or computer) with the screen. An overview of video starting with the basics is presented in this paper, the author follows with a detailed design of a video-controller board. There are many possibilities to implement the video-controller board, but an efficient one using PALs is given. The complete PAL designs and the PC-board artwork are included.

AN-105
CYCLIC REDUNDANCY CHECK (CRC)—USING PALS
(PAL Handbook, Section 6)
(System Design Handbook, Section 2)

There is a growing interest in providing data communication links to connect several processors and peripherals into one local area network. One of the most popular networks is the Ethernet. To insure reliable communications in the network an efficient error detection scheme is required. The Ethernet protocol specifies a 32-bit Cycle Redundancy Check which must operate at 10 Mbits/sec.

The following article opens with a tutorial on the CRC and then shows a detailed implementation of the Ethernet CRC using Programmable Array Logic (PAL). The use of fuse programmable devices allows easy modification to accommodate other data communications protocols as well as other applications (CRC in disk drives, etc.), that operates at rates up to 13 Mbits/sec.

Computer Aided Design (CAD) is a key tool in semicustom designs such as PAL and other gate arrays. Therefore the actual CRC design was automated by a CAD software called PALASM. The Appendix contains the entire computerized documentation of the design.

AN-107
REGISTERED PROMs IMPACT COMPUTER ARCHITECTURE
(System Design Handbook, Section 3)

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register, which holds the microinstruction during execution, is now incorporated into the PROM chip. This feature saves power, improves cycle times and decreases printed circuit board area over the present technique of using an external instruction register. Those designs which were previously non-pipelined can now be upgraded with little additional cost.

AN-109
HIGH-QUALITY MUSICAL SOUND GENERATOR
(System Design Handbook, Section 1)

The recent production of fast mutliplier ICs and large PROMs as well as the low cost of MSI TTL has made possible the development of a digital symphony or large group of new musical sounds. This tutorial paper describes a few basic acoustic parameters of musical sound. Then a digital architecture is developed for the synthesis of a modest sized orchestra. Only a minimal amount of musical knowledge is required to read this paper.

AN-110
USING ADPCM FOR IMAGE COMPRESSION
(System Design Handbook, Section 1)

Digital communication is a rapidly growing area causing new concern for efficient transmission and storage of data, voice and video information coding and compression by reducing the bandwidth required for transmission and the memory needed for storage to decrease the system cost. A simple method of compression Adaptive Differential Pulse Code Modulation (ADPCM) is explained and illustrated for video signals.

AN-111
BIG, FAST, AND SIMPLE—ALGORITHMS, ARCHITECTURE, AND COMPONENTS FOR HIGH-END SUPERMINIS
(System Design Handbook, Section 4)

This paper presents cost/performance-effective design, alternatives for conventional Von Neuman uniprocessors, based on the supercomputer design philosophy of "Big, Fast, and Simple" which is attributed to Seymour Cray.

The vehicle for presenting those alternatives is a preliminary design for a multi-MIPS 64-bit floating-point RRL supermini which incorporates arrays of 8 x 8 Cray Multipliers (74S558) and 16 x 16 Shifters (74S530), supported by other high-speed components such as 4-Bit ALUs (74S381A and 74S382A), Carry Bypasses (74S182), 8:3 Priority Encoders (74S148 and 74S348), FIFOs (67401 and 67402), and various PROMs, PALs, and interface circuits.

AN-112
FIFOs: RUBBER-BAND MEMORIES TO HOLD YOUR SYSTEM TOGETHER
(LSI Databook, Section 9)
(System Design Handbook, Section 7)

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting or intermittently halting your microprocessor. FIFO is one of those made-up words, or *acronyms*, formed from the initials of a phrase—in this case, "*F*irst-*I*n, *F*irst-*O*ut." FIFOs may be thought of as "elastic storage" devices—"local rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time. This tutorial paper both describes what FIFOs are in general, and introduces the 64 x 4 and 64 x 5 Monolithic Meories FIFOs in particular.

AN-113
PICK THE RIGHT 8-BIT —OR 16-BIT— INTERFACE PART FOR THE JOB
(LSI Databook, Section 13, Page 13-3)

A few years ago, 20-pin 8-bit buffers, registers, latches, and transceivers came into existence as a rather haphazard upwards evolution from the MSI devices available in the mid-1970s. As time went on, usage of these parts increased until they became one of the fundamental computer-system building-block primitives—the "glue" which holds the entire system together. More recently, there has emerged an orderly, matrix-like approach to combining useful attributes of interface circuits, such as Schmitt-trigger inputs, inverting outputs, high-drive outputs, and series-resistor outputs, into specific parts.

Today the demands are to reduce component costs and system board area. Reducing parts count achieves both of these objectives at one stroke; it is now possible to effectively incorporate the equivalent of two 20-pin 8-bit interface parts into one 24-pin "16-bit interface" part. The approach is to look for common configurations of pairs of 8-bit parts, and implement the pair as a single chip.

AN-114
SN54/74S516 CO-PROCESSOR SUPERCHARGES 68000 ARITHMETIC

Specialized arithmetic logic, used together with your microprocessor, can provide extra muscle for handling formidable problems like extensive number-crunching operations. In particular, the Monolithic Memories SN54/74S516 bipolar multiplier/divider/accumulator can team up with a 16-bit microprocessor such as the 68000 in a co-processor arrangement that significantly improves arithmetic throughput.

The 'S516 uses special hardware and Booth-algorithm techniques to perform multiplication nine times faster than the 68000, and division eight times faster than the precision arithmetic, and chained operations such as sum-of-products. These capabilities, coupled with the raw speed advantage, permit a number-crunching throughput improvement of 1.7 to 10 times (or more) over 68000-only systems, even when I/O overhead is considered.

The 'S516 is the only bipolar *divider* currently on the market. Its single-bus design and speed are well-matched to 16-bit systems. (However, the 'S516 is also useful in 8-bit systems where 16-bit arithmetic is required.) In general, the 'S516 can dramatically extend the life cycle of existing microcomputer systems based on microprocessors which either don't have multiplication and division instructions, or perform these operations relatively slowly. Even the 68000, a comparatively powerful microprocessor, can benefit.

The 68000 and the'S516 can, therefore, team up to multiply and divide on a bus at an optimum price/performance.

AN-115
THE DESIGN AND APPLICATION OF A HIGH-SPEED MULTIPLY/DIVIDE BOARD FOR THE STD BUS.
Northcon/82 Session 15
(System Design Handbook, Section 5)

A fundamental limitation in most microcomputer systems is high-speed arithmetic computing speed, especially when multiplications or divisions are required. A hardware multiply/divide board designed to work efficiently with a STD BUS microcomputer in an industrial control system is presented.

The application described includes the simultaneous calculation of several digitally-controlled servo loops which allow control of machinery to within the resolution of servo position sensors at a bandwidth that software alone cannot accomplish.

AN-116
FOUR NEW WAYS TO GO FORTH AND MULTIPLY
(LSI Databook, Section 12, Page 12-3)
(System Design Handbook, Section 4)

For the last year or so, it has seemed as if every time you turned around Monolithic Memories was announcing *another* new multiplier. These parts generally fall into two categories: 8 x 8 flow-through Cray multipliers, and bus-oriented sequential multiplier/dividers. Although all of these parts get referred to rather casually as "multipliers," there are major differences between the two general types as to where they fit into designs, how they operate internally, how they are controlled externally, and what they can do and at what speed.

The essential idea of a Cray multiplier, as originally put together by Seymour Cray in the late 1950s with discrete logic at Control Data Corporation, is to wire up an array of full adders in the form of a binary-arithmetic-multiplication pencil-and-paper example. The Monolithic Memories 57/67558, introduced about half a decade ago, was the original *single-chip* Cray multiplier. Many higher-speed versions of this part have since appeared.

In contrast, the Monolithic Memories 'S516 and 'S508 bus-oriented sequential multiplier/dividers are intelligent peripherals for microprocessors, somewhere in between arithmetic sequential circuits and specialized bipolar microprocessors. The 'S516 and 'S508 each can perform any of 28 different multiply and multiply-and-accumulate instructions, plus any of 13 different divide instructions, at bipolar speeds, under the control of an internal state counter.

AN-117
IMPROVING YOUR MEMORY WITH 'S700-FAMILY MOS DRIVERS
(LSI Databook, Section 10, Page 10-3)
(System Design Handbook, Section 6)

Dynamic-MOS random-access-memory integrated circuits (DRAMs) are the basic components used today as building blocks for larger computer-memory systems. Even though using DRAMs may seem very straightforward, there are some major pitfalls which designers must avoid.

This applications note discusses the circumstances which arise when designing DRAM-array memory boards, such as wiring-trace capacitance and inductance, signal reflections, voltage undershoot, and asymmetric driver-circuit output impedances. Great improvements over a naive design approach are possible by practicing more sophisticated printed-writing layout techniques, and by using second-generation dynamic-MOS drivers rather than first-generation high-current drivers.

The 'S700/730/731/734 8-bit buffers are second-generation parts having electrical and switching characteristics which are especially tailored to driving the distributed-capacitance loads presented by large DRAM arrays. The rationale behind these new parts is presented here, and specific applications are discussed: avoiding information loss from a-c power failure, and fast multiplexing of row addresses with column addresses using the complementary-enable 'S700/731 drivers.

AN-118
PSEUDO RANDOM NUMBER GENERATOR (A DISGUISED PAL)
(System Design Handbook, Section 9)

Due to their interesting properties, Pseudo Random Numbers (PRN) are useful across a wide spectrum of applications, including secure communication, test pattern generation, scramblers, and radar ranging systems. For the requirements of a given application, a "customized" PRN generator is readily implemented using PALs.

AN-119
68000 INTERRUPT CONTROLLER
(PAL Handbook, Section 6)
(System Design Handbook, Section 3)

Commercial and industrial microprocessor based systems consist of the basic block units of CPU, memory, and I/O devices. While executing the instructions in the memory the CPU must somehow be interrupted to service requests from various I/O devices. The 68000 microprocessor is a powerful 16-bit processor which makes provisions for 256 different interrupt routines. A simple and cost effective way of interfacing a peripheral's interrupt request signal to the CPU is through a Programmable Array Logic. This paper introduces two ways of designing such an interface with PALs.

AN-120
AN INTERFACE BETWEEN AN SN74S409 DYNAMIC RAM CONTROLLER AND A 68000 CPU
(System Design Handbook, Section 6)

Dynamic RAMs were introduced to increase the compactness of a memory unit in a microprocessor based system. In order to efficiently control a dynamic RAM, some controllers are needed. Most controllers are not compatible with the microprocessor used in the system, so an interface may be needed. This interface may be implemented using Programmable Array Logic devices (PALs), as the example described in this paper (interfacing a 68000 CPU with one or more SN74S409 dynamic RAM controllers). This interface should select the desired controller, provide a refresh cycle clock to the dynamic RAM controllers and control signals to the CPU, the dynamic RAM controllers, and the dynamic RAMs. The exact implementation of other interfaces of this kind may vary dependng on the CPU and the functions which can be provided by the controllers.

AN-121
ENHANCING 8086 ARITHMETIC USING THE SN54/74S516 MULTIPLIER/DIVIDER
(System Design Handbook, Section 4)

A serious limitation in most microcomputers is arithmetic computation at high speed, especially when multiplications or divisions are required. With minimal interface and programming overhead, the operations can be performed at very high speed by the SN54/74S516 multiplier. This paper describes how a PAL is used to interface the SN54/74S516 to the INTEL 8086 Microprocessor.

AN-123
SHADOW REGISTER ARCHITECTURE SIMPLIFIES DIGITAL DIAGNOSIS
(System Design Handbook, Section 2)

A series of new devices including register and PROMs with diagnostics now make it easier for system designers to include diagnostic circuitry in microprogrammed systems. When in the diagnostic mode, these devices allow for complete system controllability and observability with a minimum of additional hardware. Other schemes such as embedding diagnostic code in a digital system and LSSD (Level-Sensitive Scan Design) have been used in the past, but these techniques have their drawbacks. This new series of products as well as microprogrammed architectures using these products will be explored in this paper.

AN-125
IMPLEMENTATION OF SERIAL/PARALLEL CRC USING PAL DEVICES
(System Design Handbook, Section 2)

CRC, or Cycling Redundancy Check, is an error detection technique widely used in digital data communication and storage systems. CRC can be performed either serially or in parallel. Serial CRC is implemented in an environment where data is transmitted in a bit-wise manner. In systems where data is transmitted in form of bytes, it is more desirable to implement CRC in parallel. The following article will describe the hardware required for implementing both serial and parallel CRC. It will then discuss how the family of Programmable Array Logic devices can be applied in such implementations. Detailed PAL design examples of a serial CRC-16 generator and an 8-bit parallel CRC-CCITT generator are included in the appendix for reference.

CONFERENCE PROCEEDINGS

CP-102
DOING YOUR OWN THING IN HIGH-SPEED DIGITAL ARITHMETIC
(System Design Handbook, Section 4)

This tutorial paper presents in detail two of the standard tricks of the trade in high-speed arithmetic: carry prediction and bypassing, and Booth multiplication. Emphasis is placed on gaining understanding of these techniques, but there is also some information on actual products which incorporate them.

CP-109
MINIMUM CHIP-COUNT NUMBER CRUNCHER USES BIPOLAR CO-PROCESSOR
(System Design Handbook, Section 4)

The high speed, programmability, and flexibility of bipolar parts are exploited in a floating-point arithmetic co-processor board which is presented in this paper. The operation of the co-processor and the detailed implementation is supplied. The paper concludes with a comparison of the performance of the bipolar co-processor with other implementations. This design is found to have much better performance while maintaining a low chip count, thus providing a cost-effective solution.

CP-110
SUPERCHARGING MICROPROCESSOR ARITHMETIC
(System Design Handbook, Section 4)

MOS or bipolar microprocessors have fairly extensive instruction sets. However applications requiring high-speed arithmetic computations such as multiply and divide operations, may preclude the use of the microprocessors. In situations where extensive number crunching is required with minimal external hardware, low cost, and a short development cycle, the Monolithic Memories SM54/74S516, 16-bit multiplier/divider, provides an excellent solution.

This paper presents simple hardware interfaces for using the 'S516 with the Am29116 in a graphics environment. Another application using the 'S516 with the 8086 is also discussed. The performance of these microprocessors with and without the 'S516 are tabulated and the speed enhancements achieved are 6:1 for the AM29116 and 3:1 for the 8086, for a multiply operation.

CP-111
FAST 64 x 64 MULTIPLICATION USING 16 x 16 FLOW-THROUGH MULTIPLIER AND WALLACE TREES
(System Design Handbook, Section 4)

The Monolithic Memories SN54/74S556 is a high-speed fully-parallel 16 x 16 multiplier and it provides the entire 32-bit product on a flowthrough basis from a single part. It is available in an 84-pin Leadless Chip Carrier (LCC) and 88-pin, pin-grid array packages. 8 x 8 40-pin array-multipliers such as the SN54/74S557/8 have been available for several years, however there is a large parts count for implementing longer wordlengths.

This paper describes the design philosophy and internal architecture of the 'S556 and applications for larger word-length multiplications such as 32, 48, and 64 bits using these multipliers and high-speed PROMs and ALUs also available from Monolithic Memories.

The system advantages for using the 'S566 over the MPY-16H-class multipliers is also discussed; the main advantages being the availability of the entire product each cycle and the space savings on the board.

ARTICLE REPRINTS

AR-100
PAL SHRINKS AUDIO SPECTRUM ANALYZER (PART 1 OF 2)

Using an audio spectrum analyzer as the example, the author demonstrates how PALs can reduce board space, maximize performance, save money, and improve quality for DSP. Specific diagrams offer ways a designer can build versatility into the microprogram to create other applications.

AR-101
PAL SPECTRUM ANALYZER IMPROVES PERFORMANCE (PART 2 of 2)

Continuing the idea from the first part of this two part paper (AR-100), the author adds ideas from the reality of high performance to the use of PALs in DSP architecture. Control logic is the key to success since PALs have flexible coding. Simplified tables and diagrams round out the author's illustration.

AR-108
STATE-OF-THE-ART IN HIGH SPEED ARITHMETIC INTEGRATED CIRCUITS

Use of bipolar technology to construct arithmetic ICs has resulted in devices with increasing switching speed and gate density and low power dissipation. Future technological advances should have an even greater impact on product performance through larger wafer diameters and sharper pattern fabrication.

AR-109
AN 8 x 8 MULTIPLIER AND 8-BIT MICROPROCESSOR PERFORM 16 x 16 BIT MULTIPLICATION

A special algorithm implemented in software doubles an 8 x 8-bit multiplier's usual capabilities, permitting efficient 16 x 16 multiplications of signed, unsigned or mixed two's-complement numbers. The article presents this requisite multiplication algorithm as it is implemented on a Z80 μP utilizing the SN74S558.

AR-110
REAL-TIME PROCESSING GAINS GROUND WITH FAST DIGITAL MULTIPLICATION

Refinements in algorithm and hardware have improved the speed and power of single-chip multipliers. These chips can speed the complex operations needed for digital treatment, which previously could be carried out off line using large computers. Functions like autocorrelation and fast Fourier transforms necessary for digital filtering and compression, for example, can now be done in real time using these new multipliers. Algorithms and specific applications for these new multipliers are given in this paper.

AR-112
SINGLE-CHIP CONTROLLER INCREASES MICRO-PROCESSOR THROUGHPUT
(PAL Handbook, Section 8)

A design technique using Programmable Array Logic to minimize hardware in a DMA controller that combines fast response with the potential to service multiple input or output devices and the flexibility to handle many different applications is presented in this paper.

AR-113
FPLA ARBITER CONCEPT ADAPTS TO APPLICATION NEEDS
(PAL Handbook, Section 8)

The FPLA arbiter, specifically the PAL, implements an efficient, easily customized arbiter whose versatile Boolean statement format meets numerous system requirements. Applications illustrating the advantages of the PAL concept are explored in this article.

AR-114
PROGRAMMABLE ARRAY LOGIC TO FLEXIBLE APPLICATIONS OF 8-BIT WIDE MEMORIES
(PAL Handbook, Section 8)

The flexible application of memory devices in small microprocessor based systems has been enhanced by the introduction of 8-bit wide static random access memories. Using programmable logic technology in conjunction with 8-bit wide memory devices adds even more flexibility and helps to reduce parts count. The three basic types of programmable logic available are PLA, PROM, and PAL. The advantages of using PALs over PLAs and PROMs for this application are explored. A detailed implementation example is also provided.

AR-115
FIELD-PROGRAMMABLE LOGIC ARRAYS BRIDGE THE STANDARD-IC/GATE ARRAY GAP

Once considered endangered species in light of rapidly developing gate-array and custom-VLSI technologies, field-programmable logic arrays are receiving increased attention from designers striving to make their digital circuits more compact without incurring large engineering costs. The devices' unique internal architectures, coupled with their ability to promote fast, interactive product design cycles, allow high-speed, medium-density systems to benefit from low production costs, optimized logic implementations and simple revisability. Moreover, field-programmable logic families consist of standard, second-sourced components and thus allow designers to create customized circuit elements without risking long delivery times and without making production commitments to unproven designs. The advantages of programmable array logic and available software tools are explored in this article.

AR-116
ON-CHIP CIRCUITRY REVEALS SYSTEM'S LOGIC STATES

As computer and data processing systems grow in size and complexity, designers must continue to refine the methods needed to test them. One method, based on serial scan diagnostics, affords a systematic diagnostic technique for pinpointing hardware failures in a digital system. The diagnostic capability is implemented in a system by adding special hardware that enables key test points to be sampled and important control signals to be stimulated. Systems containing the diagnostic hardware are simple to test and are usually more reliable. This diagnostic technique and the two families of devices which incorporate this diagnostic hardware (Diagnostic PROMs and 8-Bit Register) are the subject of this paper.

AR-117
SINGLE-CHIP CONTROLLERS COVER RAMS

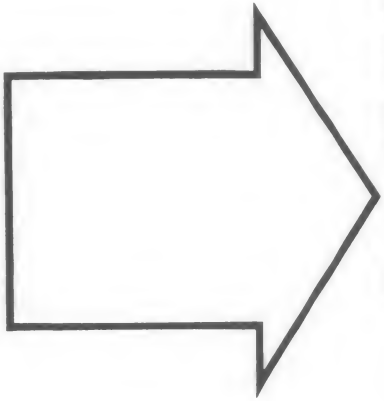
As dynamic RAMs become widely used, demand is growing for automatic sequencing of RAM access signals and refresh controls. NSC's DP8408 and DP8409 are single-chip dynamic RAM controllers available also from Monolithic Memories as the 74S408/9 series.

A short description of dynamic RAM operation is provided and both devices are described in several applications.

AR-118
PROGRAMMING LOGIC CHIPS ON PERSONAL COMPUTERS

Programmable Array Logic chips are fast becoming an economical alternative to custom integrated circuits. Personal computers can assist in the design of programmable arrays, further reducing the cost of developing custom electronic logic. PALASM, the CAD tool for PALs, which was previously available only for mainframes and minicomputers, is now available for many popular personal computers. This article outlines the design process for PALs using PALASM and personal computers.

Available through the Advertising Department of Monolithic Memories.



Package Drawings

Package Engineer — Robert Newman
Draftsman — Phuong Tran

Introduction

Flat Pack

Cerdip

Leadless Chip Carrier

Molded

Top Brazed Ceramic

CerPack

Leads/Finish

Monolithic Memories Incorporated provides high strength nickel iron steel (Alloy 42) leads on all flat pack and side braze packaged devices. In addition, the user is offered a choice of two finishes, standard gold plate and solder dip over gold plate.

***Alloy 42**

Composition (Nominal)	Nickel	42.0%
	Manganese	.50%
	Cobalt	.19%
	Silicon	.07%
	Chromium	.06%
	Aluminum	.024%
	Carbon	.012%
	Phosphorous	.006%
	Sulfur	.001%
	Iron	Balance

***Physical Properties**

Melting Point	1,427°C
Curie Temperature	380°C
Density (g/cc)	8.11
Coefficient of Thermal Expansion cm/cm°C(21 - 343°C)	5.4×10^{-6}
Thermal Conductivity cal-cm/sq cm-sec°C	.03
Electrical Resistivity (micro ohm-cm at 20°C)	71
Modulus of Elasticity (psi)	21.1×10^{6}
Tensile Strength (ksi)	97
Elongation	10%
Vickers Hardness	208

* Stamping Technology Data Sheet
CarTech Data Sheet

Lids

Monolithic Memories Incorporated utilizes high durability KOVAR lids on all Flatpack, chip carriers and sidebrazed packages.

***Composition**

Nickel	29.0%
Cobalt	17.0%
Manganese	.30%
Silicon	.20%
Carbon	.02% Maximum
Iron	balance
Lid Finish — Gold plating	
Melting Point	1,450°C
Curie Temperature	435°C
Density (g/cc)	8.36
Thermal Conductivity (cal-cm/sq cm-sec°C)	.05
Electrical Resistivity (micro ohm-cm at 20°C)	49

*CarTech Data Sheet

Package Body

Monolithic Memories Incorporated utilizes high reliability multilayer ceramics in the body of all side brazed packages. The body ceramic is comprised of a mixture of 90% alumina (AL_2O_3) with other ceramics such as silica (SiO_2), MgO and CaO.

***Physical Properties (nominal)**

Bulk Density	3.6 grams/cc
Water Absorption	~0%
Vickers Hardness	1,300
Flexural Strength	40,000 psi
Young's Modulus	39×10^{6} psi
Coefficient of Linear Expansion	6.5×10^{-6} (40°C-00°C)
Thermal Conductivity	.04 Cal/cm · Sec · °C
Specific Heat	.20 Cal/g°C
Dielectric Strength	10 kv/mm
Volume Resistivity	10^{14} ohm · cm (20°C)
Volume Resistivity	10^{9} ohm · cm (300°C)

* Kyocera International Data Sheet

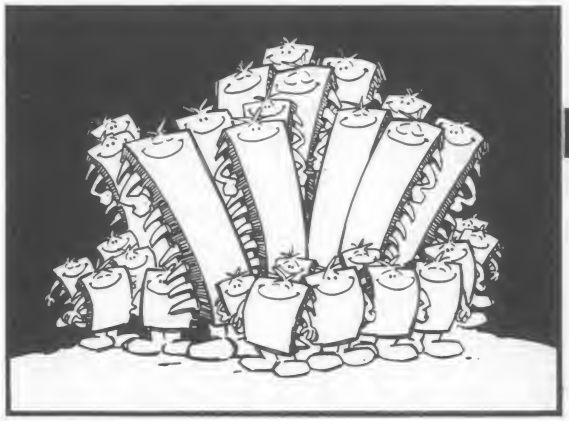
Bonding Wire

Monolithic Memories Incorporated uses 1.25 mil aluminum wire to connect I.C. chips to all hermetic packages. The same high reliability wire is used in side brazed packages, flat packs, cerpacks, chip carriers and cerdip packages.

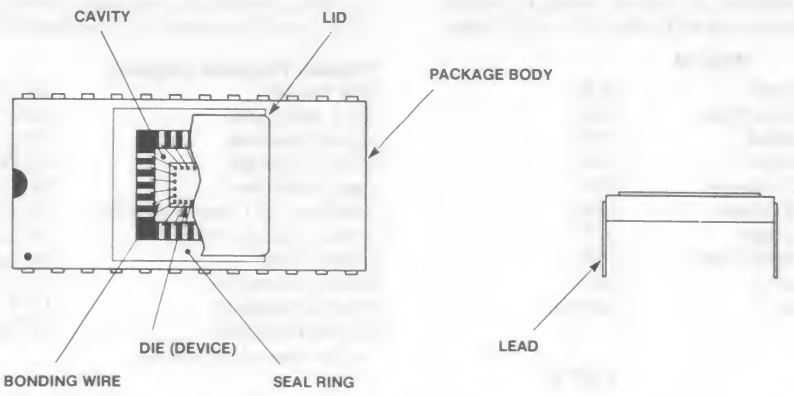
***Physical Properties**

Composition	Aluminum	99%
	Silicon	.85% to 1.15%
	Other	.009% maximum
Tensile Strength	17 to 21 grams	
Elongation	1% 70 4%	
Resistance (ohms/inch)	.94 to 1.1	
Weight (mg/foot)	.61 - .68	

* Secon Metals Corp., Data Sheet, 1975



Sidebrazed Package



PACKAGE BODY

1. Alumina (Standard Dark)

LID

1. Metal (Plated Kovar) Soldered to Gold, Plated Seal Ring
2. Ceramic Frit

LEAD MATERIAL

1. Alloy 42

BONDING WIRE

1. 1.25 Mil Aluminum

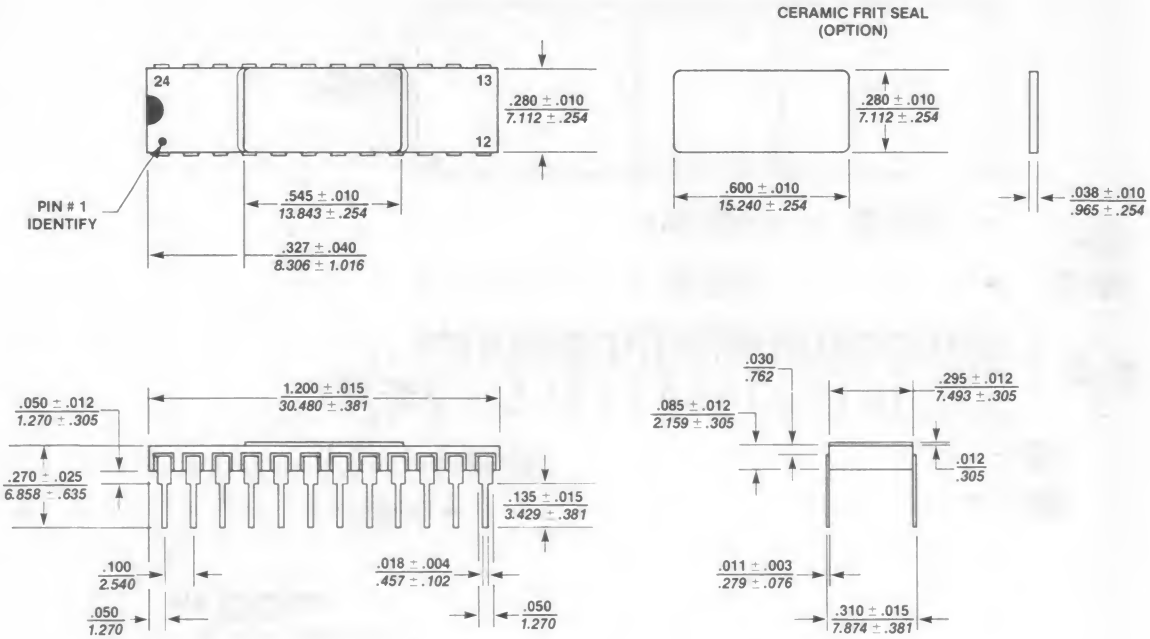
CAVITY

1. Gold Over Tungsten for Au/Si Eutectic Die Attach

LEAD FINISH

1. Gold Plate (Standard)
2. Solder Dip Over Gold Plate

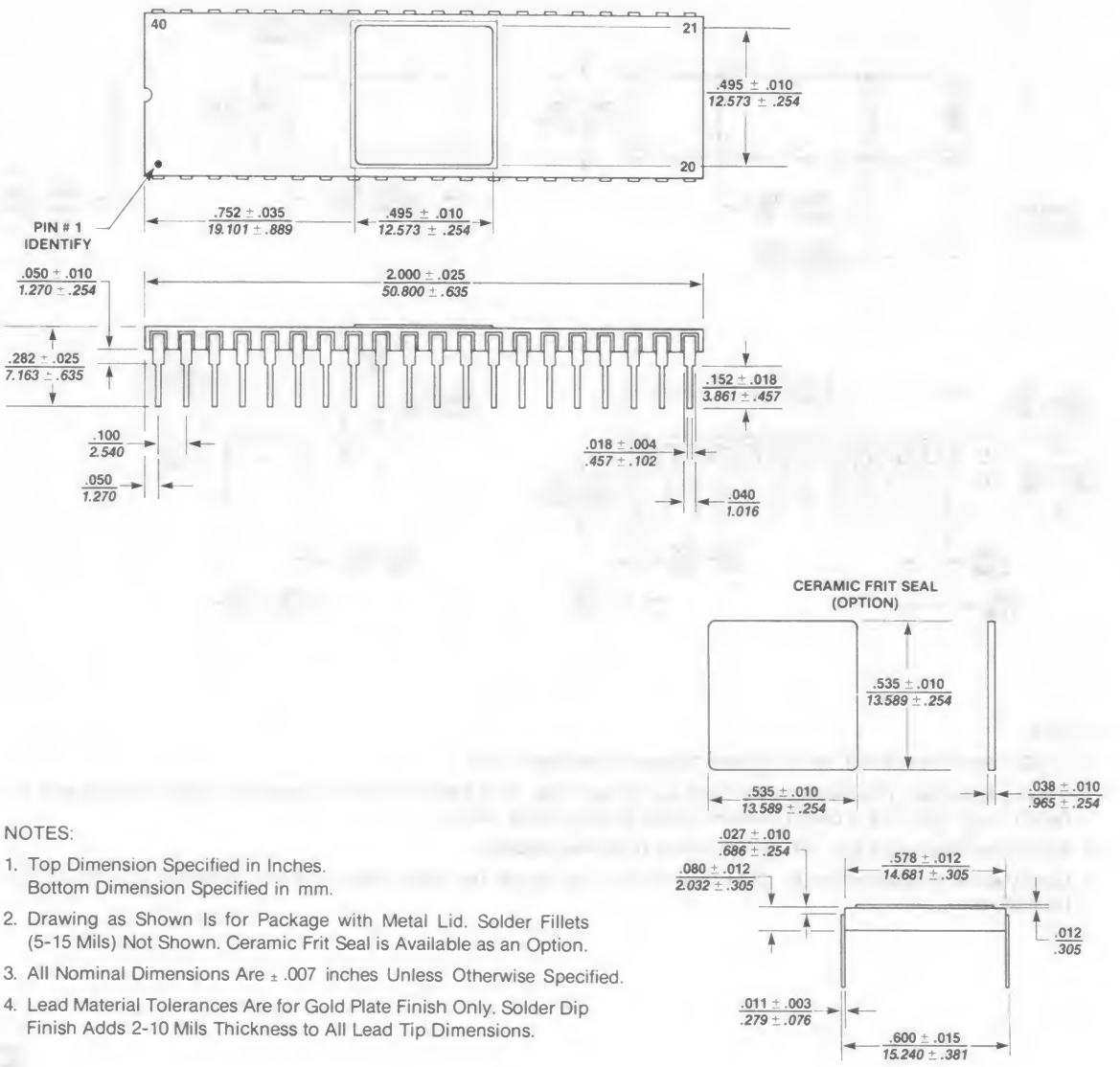
D24S Side Brazed Ceramic SKINNYDIP



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. Drawing as Shown Is for Package with Metal Lid. Solder Fillets (5-15 Mils) Not Shown. Ceramic Frit Seal is Available as an Option. Large Tolerance Is Due to Different Lids for Different Cavity Options.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Gold Plate Finish Only. Solder Dip Finish Adds 2-10 Mils Thickness to All Lead Tip Dimensions.

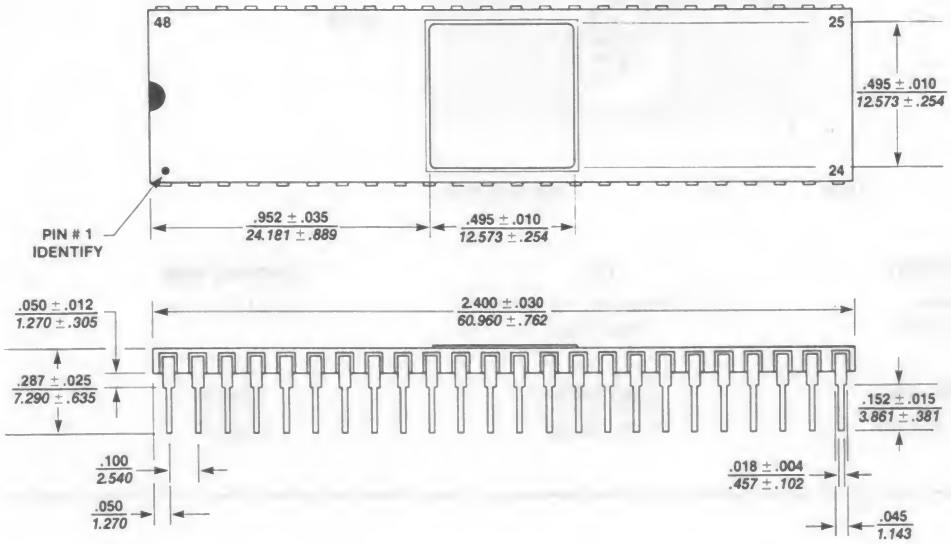
D40 Side Brazed Ceramic DIP

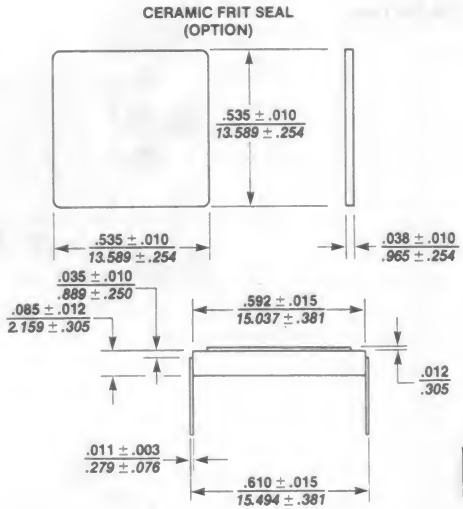


NOTES:

1. Top Dimension Specified in Inches.
   Bottom Dimension Specified in mm.
2. Drawing as Shown Is for Package with Metal Lid. Solder Fillets (5-15 Mils) Not Shown. Ceramic Frit Seal is Available as an Option.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Gold Plate Finish Only. Solder Dip Finish Adds 2-10 Mils Thickness to All Lead Tip Dimensions.

D48 Side Brazed Ceramic DIP

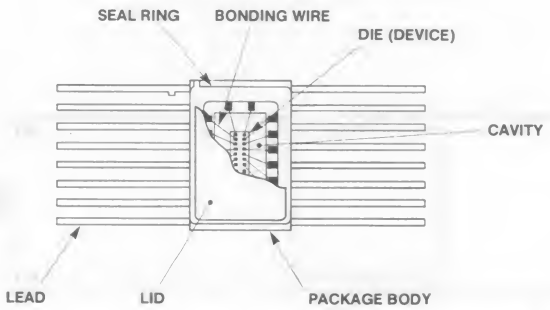




NOTES:

1. Top Dimension Specified in Inches.
   Bottom Dimension Specified in mm.
2. * Drawing as Shown Is for Package with Metal Lid. Solder Fillets (5-15 Mils) Not Shown. Ceramic Frit Seal is Available as an Option.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Gold Plate Finish Only. Solder Dip Finish Adds 2-10 Mils Thickness to All Lead Tip Dimensions.

Flat Pack



PACKAGE BODY
1. Alumina (Standard Dark)

LID
1. Metal (Plated Kovar) Soldered to Seal Ring

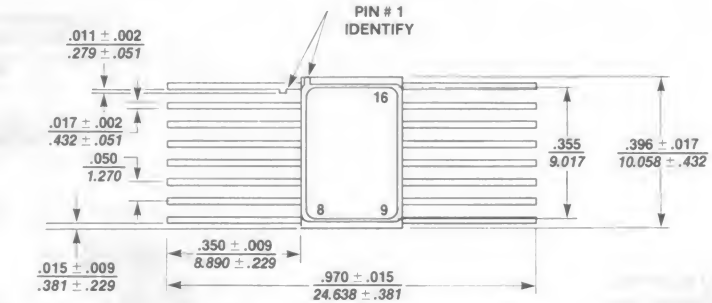
BONDING WIRE
1.25 Mil Aluminum

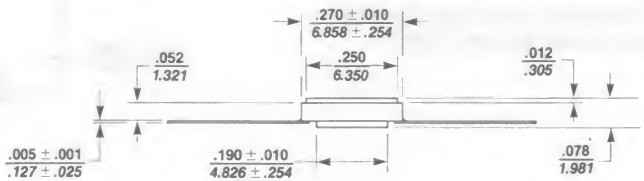
CAVITY/SEAL RING
Gold Over Alumina

LEAD FINISH
Gold Plating

LEADS
Alloy 42

F16 Flat Pack

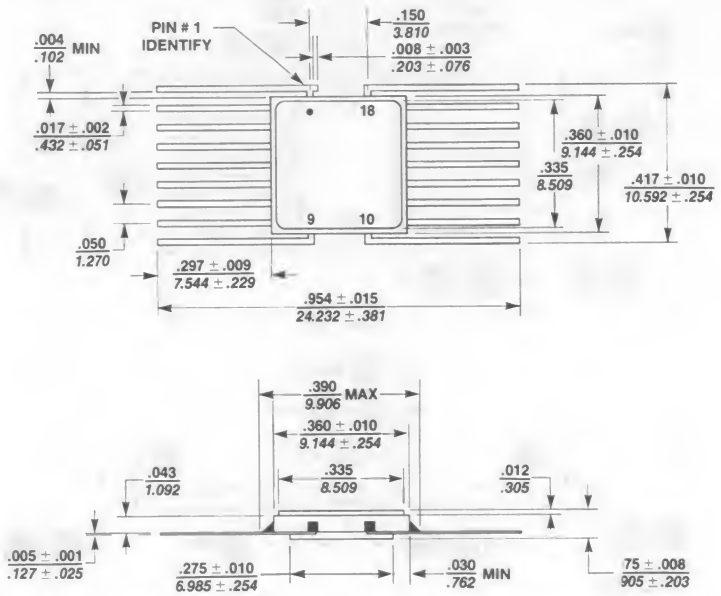




NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets on Lid Edges Not Shown.

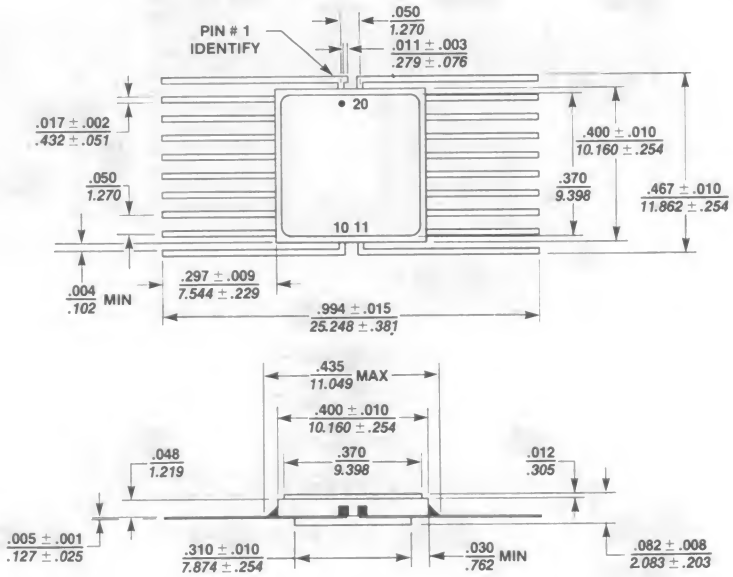
F18 Flat Pack (3/8"x3/8")



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.

F20-1 Flat Pack (3/8"x3/8")

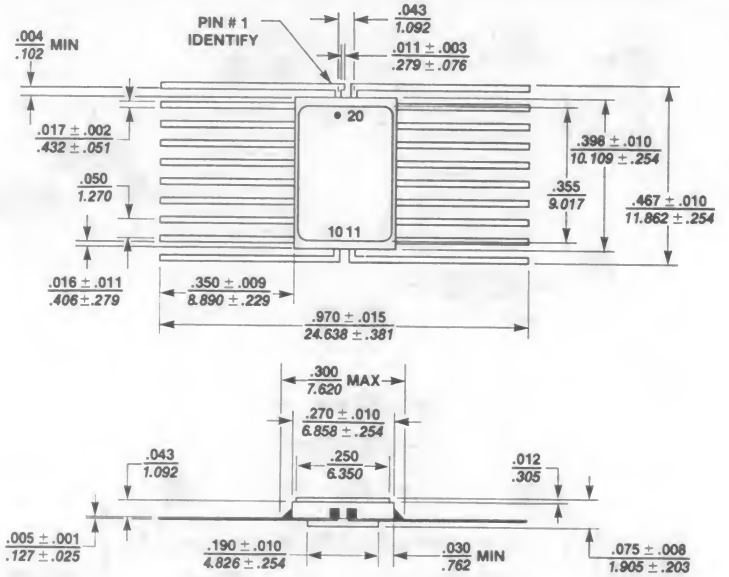


NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.

15

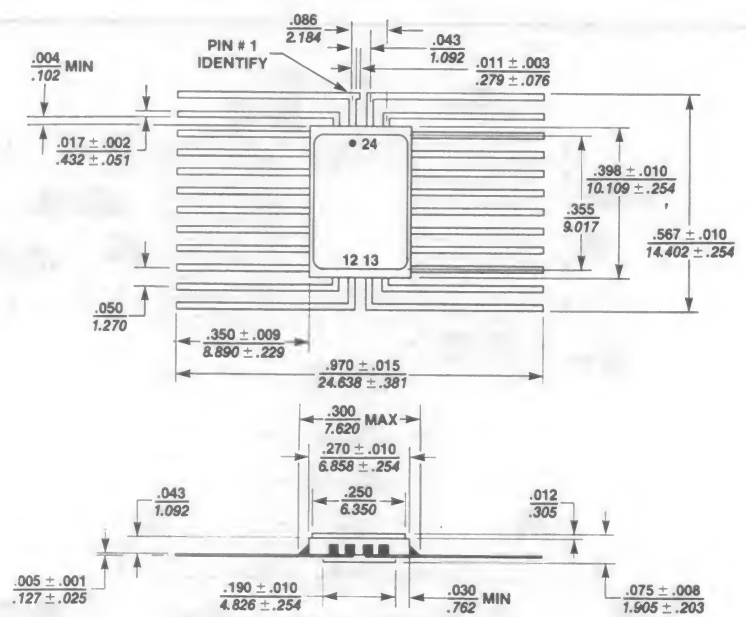
F20-2 Flat Pack
(1/4"x3/8")



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.

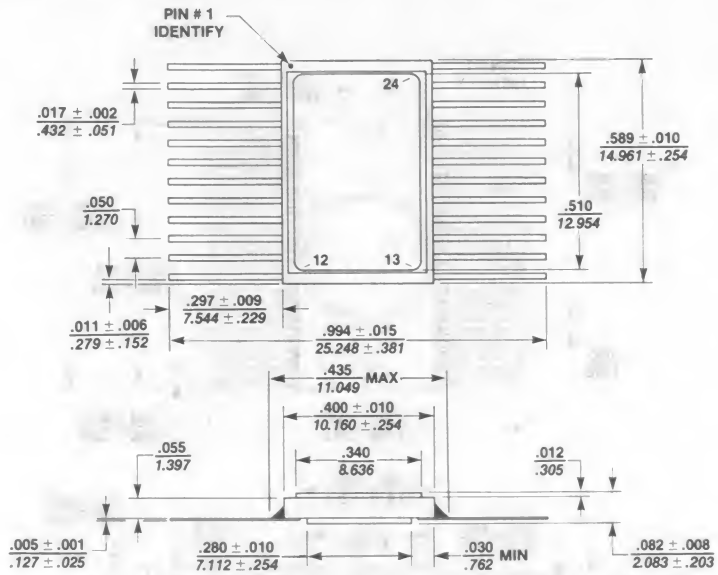
F24-3 Flat Pack
(1/4"x3/8")



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.

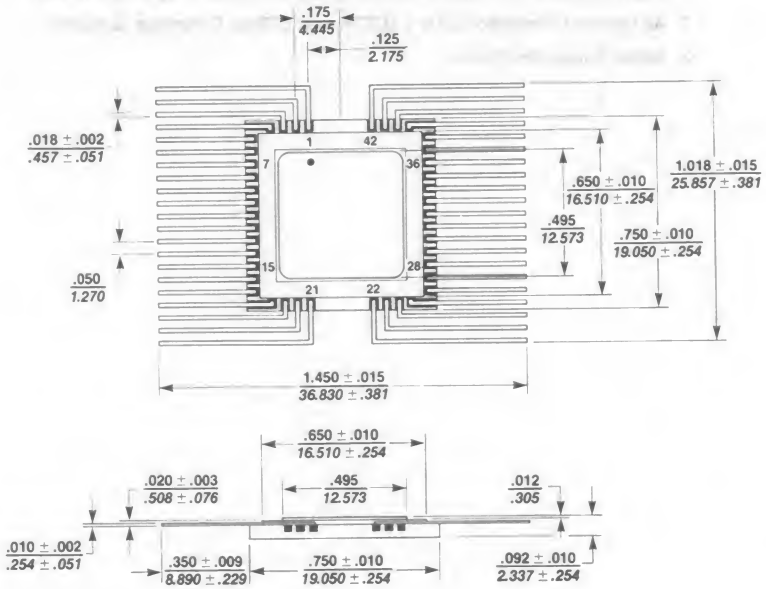
F24-4 Flat Pack



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.

F42-1 Flat Pack (3/4"x3/4")

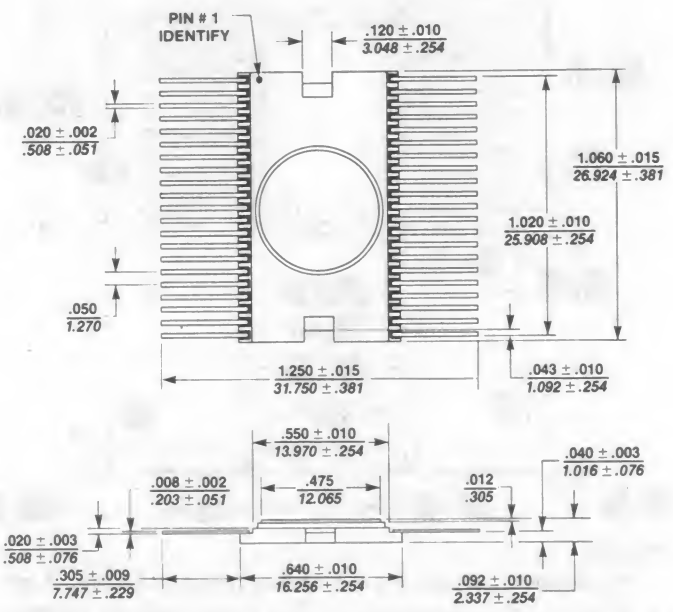


NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets Not Shown.

15

F42-2 Flat Pack



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets Not Shown.

Cerdip Package

Caps and Bases

Caps and bases consist of two sections, pressed alumina body and LS-0113 glass seal ring.

Properties of pressed Alumina (Nominal)

Alumina Content	91%
Water Absorption	~ 0%
Specific Gravity	3.80
Vickers Hardness	1,300
Coefficient of Linear Expansion	7.1×10^{-6} °C(40° C - 400° C)
Thermal Conductivity	.05 cal/cm·sec· °C
Flexural Strength	34,800 psi
Dielectric Strength	10 kv/mm
Volume Resistivity	10^{12} Ω · cm(25° C)
Volume Resistivity	10^{8} Ω · cm(25° C)

Physical Properties of LS-0113 Seal Glass

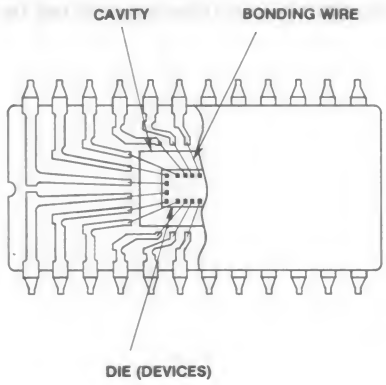
Coefficient of Thermal Expansion (30 - 250° C)	6.4×10^{-6}/° C
Specific Gravity	6.85
Transition Point	320° C
Softening Point	400° C
Seal Temperature	450° C
Dielectric Loss Tangent (1MHz·25° C)	33.0
Dielectric Constant	85.0
Volume Resistivity 250° C · Ω cm)	2.5×10^{9}
Thermal Conductivity @ 25° C, Kcal/m, hr° C)	.78
∝ Particle Emission CPH/cm^2	22

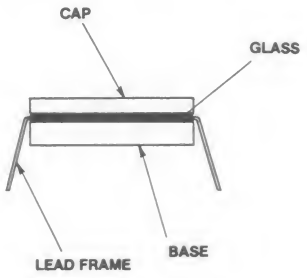
Cavity/Die Attach

Monolithic Memories Incorporated utilizes high strength eutectic die attach in CerDip packages. CerDip bases have a gold lined cavity and attachment of die occurs through the formation of a silicon/gold eutectic at elevated temperatures.

Leadframe Material/Lead Finish

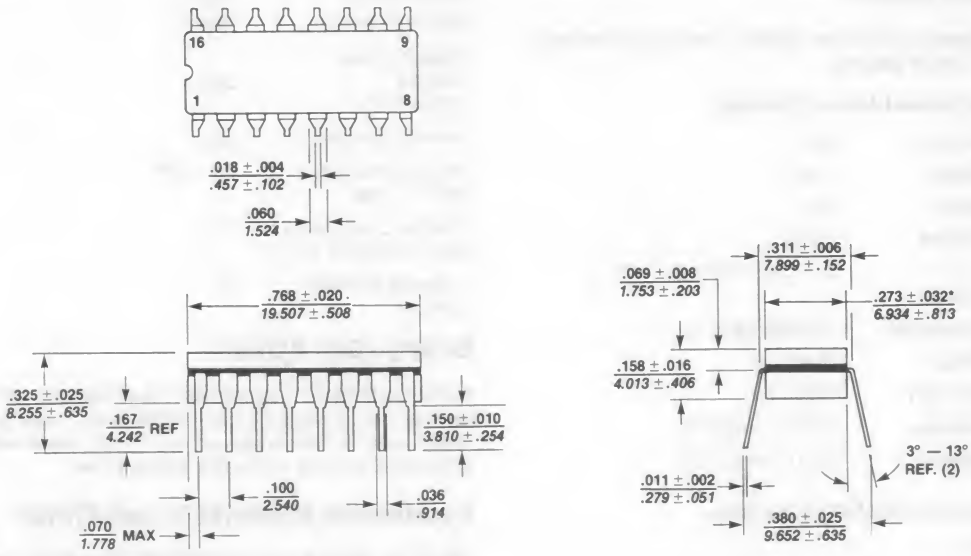
Monolithic Memories Incorporated uses Alloy 42 as a leadframe material for Cerdip packages. Standard lead finish is tin plate (300 - 600 μ). Solder dip is used to conform to 38510 lead finish spec.





LEAD FRAME	BONDING WIRE	CAP AND BASE
Alloy 42	1.25 Aluminum	Pressed Alumina
GLASS	**CAVITY**	**LEAD FINISH**
LS-0113	Gold Over Alumina For Eutectic Die Attach	1. Tin Plate 2. Solder Dip

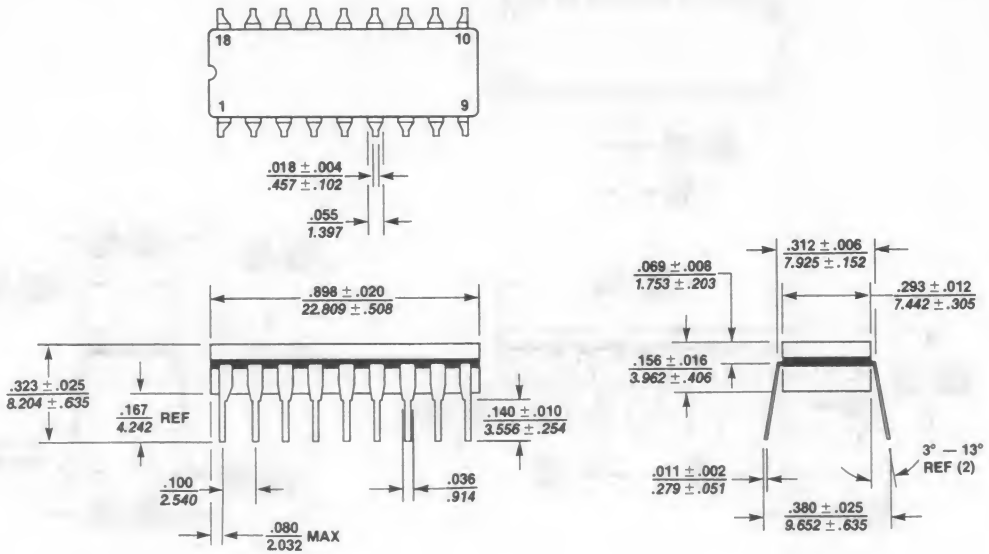
J16 Ceramic DIP



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. Specified Body Dimensions Allow for Differences Between SSI, MSI and LSI Packages.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

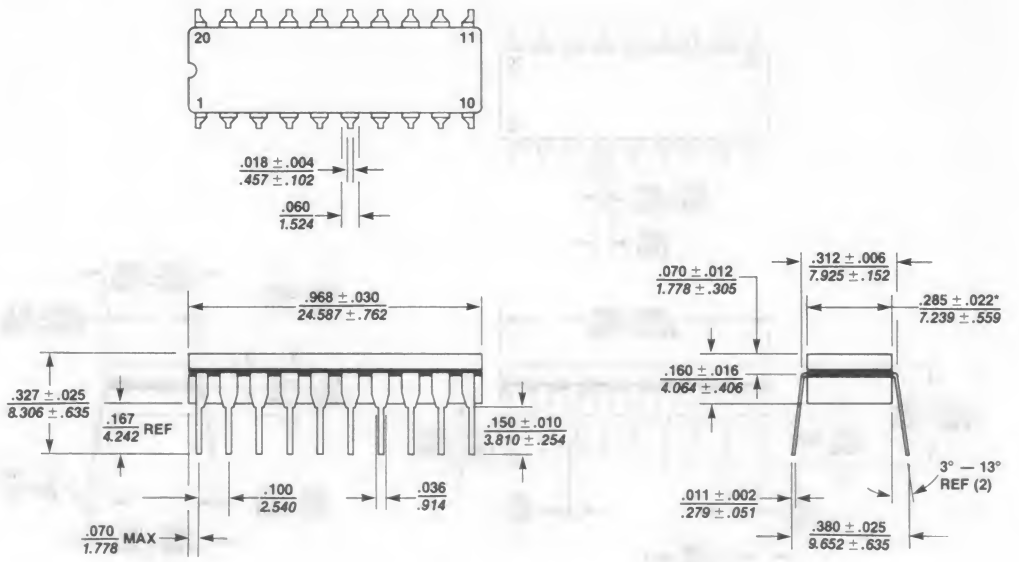
J18 Ceramic DIP



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.
4. Specified Body Dimensions Allow for Differences Between LSI and VLSI Packages.

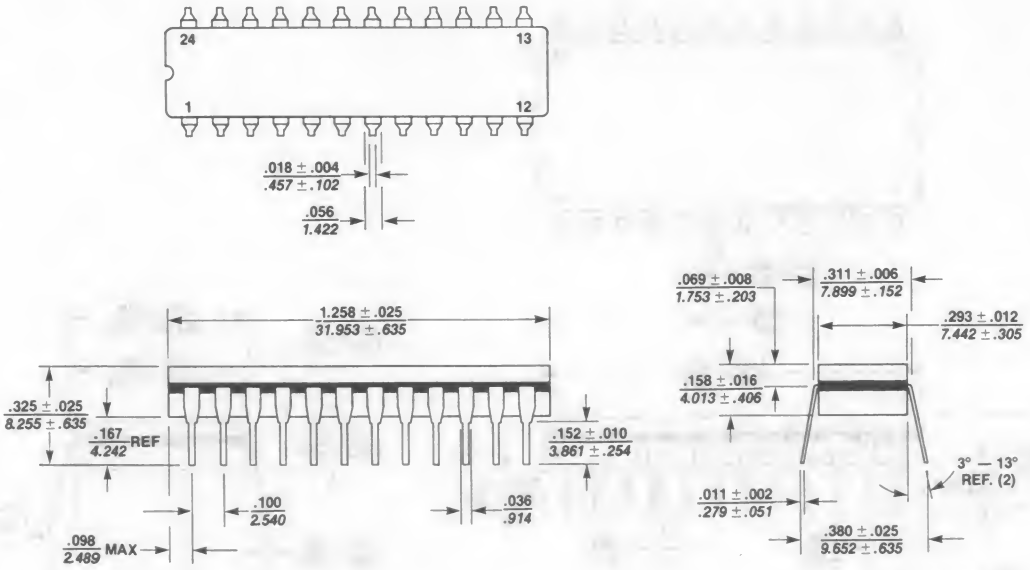
J20 Ceramic DIP



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. Specified Body Dimensions Allow for Differences Between SSI, MSI and LSI Packages.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

J24S Ceramic SKINNYDIP

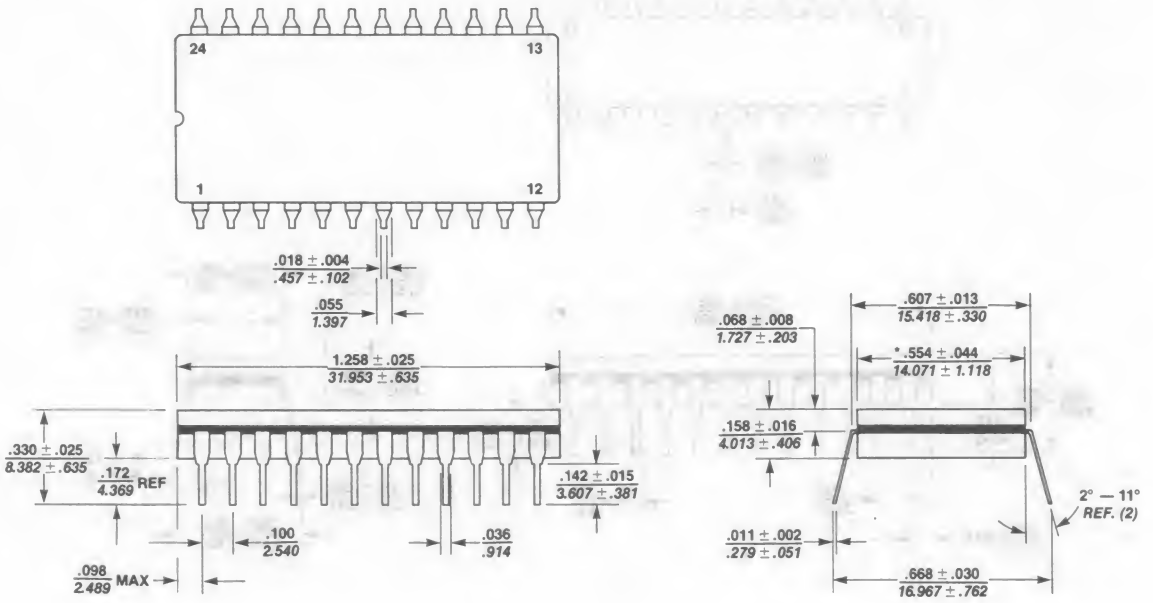


NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.
4. Drawing as Shown Covers Tolerances of Multiple Packages.

15

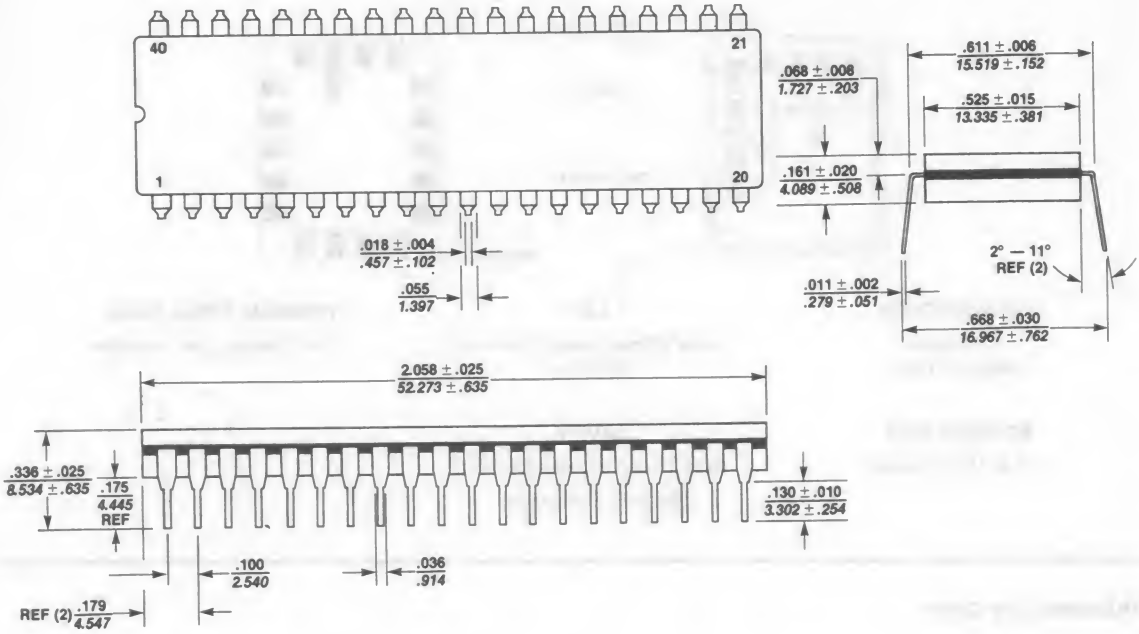
J24 Ceramic DIP



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. * Specified Body Dimensions Allow for Differences Between, MSI and LSI Packages, For Narrower Tolerance Window See Option
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

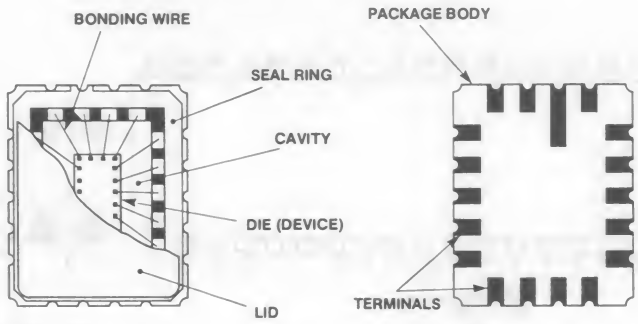
J40 Ceramic DIP



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. Specified Body Dimensions Allow for Differences Between, MSI and LSI Packages
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

Leadless Chip Carrier



PACKAGE BODY

1. Alumina (Standard Dark)

LID

1. Metal (Plated Kovar) Soldered to Seal Ring

TERMINALS/SEAL RING

1. Gold Plating Over Tungsten

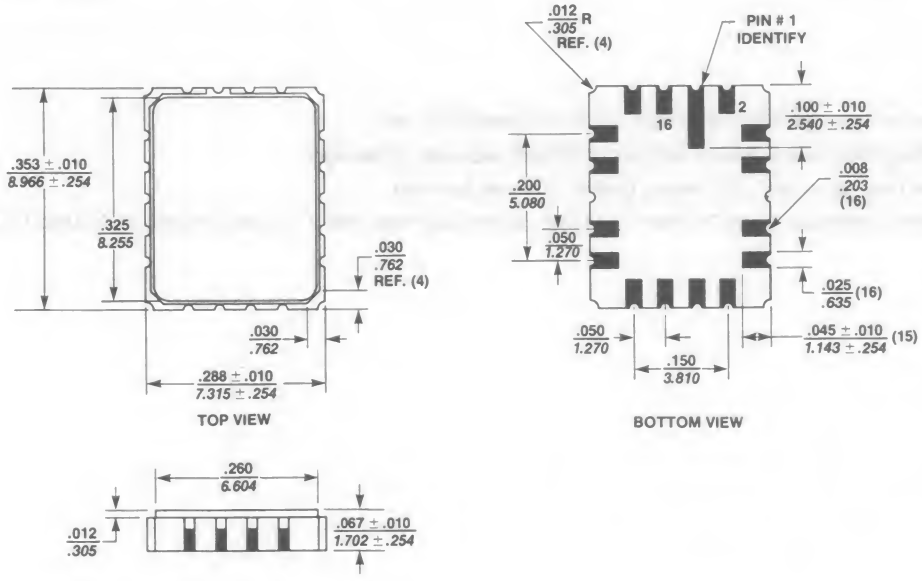
BONDING WIRE

1. 1.25 Mil Aluminum

CAVITY

Gold Over Tungsten for Au/Si Eutectic Die Attach

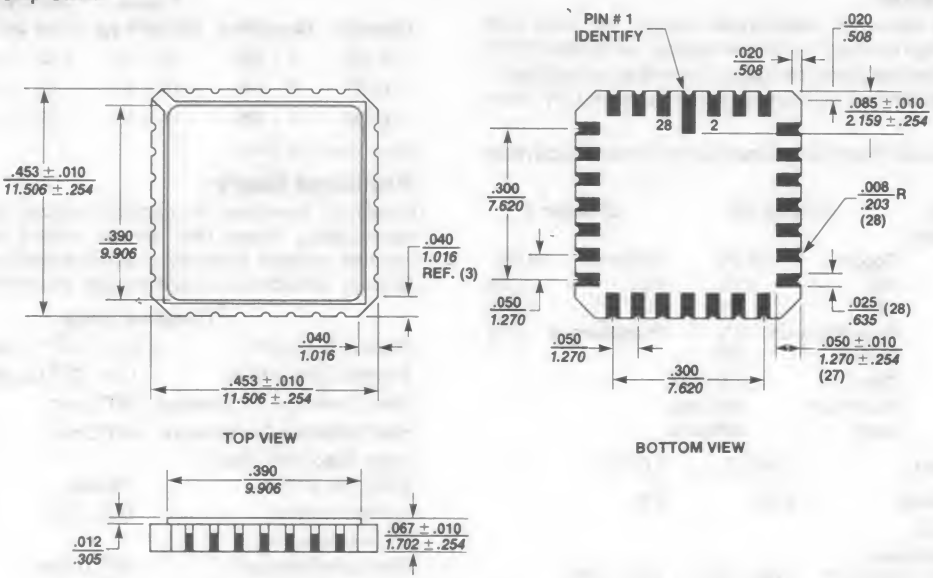
L16 Leadless Chip Carrier



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets on Lid Edges Not Shown.

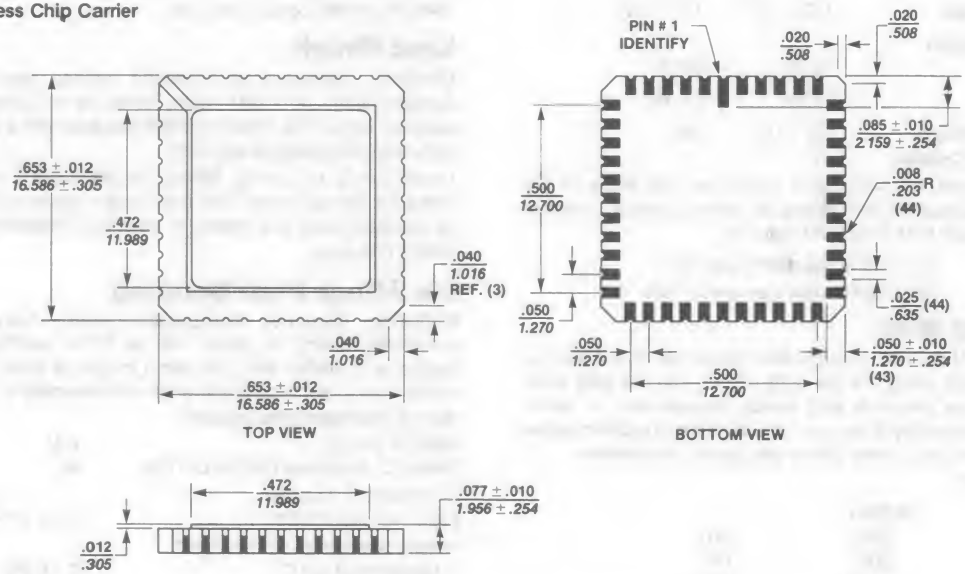
L28 Leadless Chip Carrier



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets on Lid Edges Not Shown.

L44 Leadless Chip Carrier



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
3. Solder Fillets on Lid Edges Not Shown.

Leadframe

Monolithic Memories Incorporated utilizes the latest high strength, high conductivity copper leadframes for assembling devices in molded plastic packages. Depending on availability, all copper leadframes will be stamped from either ALLOY 195 or TAMAC 5.

Listed below are the physical parameters of these two equivalent alloys:

Nominal Composition	(1) Alloy 195	(2)Tamac 5
	Copper 97.0%	Copper 98.0%
	Iron 1.5%	Iron .75%
	Tin .6%	Tin 1.25%
	Phosphorous .1%	Phosphorous .03%
	Cobalt .8%	
	Zinc .2% max.	
	Aluminum .02% max.	
	Lead .02% max.	
Melting Point	1,090° C	1.075° C
Density (G/cc)	8.92	8.8
Coefficient of Thermal Expansion (20 - 300° C) cm/cm/° C	1.69×10^{-5}	1.67×10^{-5}
Thermal Conductivity at 20° C cal - cm/sq cm - sec - °C	.47	.33
Electrical Resistivity (microhm - cm @ 20° C)	3.94	4.93
Modulus of Elasticity (psi)	1.73×10^{7}	1.71×10^{7}
Tensile Strength (ksi)	75/85	69/79
Elongation	2 - 5%	4 - 7%
Vickers Hardness	157 - 175	150 -

Mechanical Criteria

All leadframes are sufficiently strong so that leads in the finished package will survive two 90° bends (bend is complete cycle 0° to 90° to 0°) without fracturing.

(1) OLIN Brass data sheet, 1971

(2) TAMAGAWA data sheet, 1980

Bonding Wire

Monolithic Memories Incorporated chips are connected to package leads using 1.0 mil, 1.25 mil, or 1.30 mil gold wire, depending on assembly and device requirements. In some cases, the impurities of the gold wire will vary to accommodate particular devices. Listed below are typical parameters:

Composition

Gold	99.9990		
Silver	.0001	-	.001
Calcium	.0001	-	.001
Copper	.00001	-	.0002
Iron	.0001	-	.001
Beryllium	.0001	-	.001
Magnesium	.0001	-	.001
Others	.0001	-	.001

Diameter	Elongation	Tensile Strength (g)	*Resistance ohms per in.	Weight mg per ft
.00100	3 - 6%	8 - 12	1.13 - 1.20	2.83 - 3.20
.00125	3 - 6%	10 - 14	.72 - .77	4.42 - 5.00
.00130	3 - 6%	14 - 18	.67 - .71	4.78 - 5.41

*Secon Metal data sheet

Package Body

Monolithic Memories Incorporated utilizes a low chlorine thermosetting epoxy resin for all molded assembly. This moisture resistant thermally conductive plastic provides high reliability protection in a commercial environment.

	[1]Thermoset Plastic
Thermal Expansion	2.5×10^{-5} ° C max.
Thermal Conductivity	1.6×10^{-3} Cal/Sec cm °C min.
Glass Transition Temperature	150° C min.
Heat Deflection Temperature	200° C min.
Water Absorption After Boiling for 24 Hrs.	.5% max.
Specific Gravity	1.80 - 1.86
Volume Resistivity (Room Temperature)	10^{15} Ω -cm
Volume Resistivity (150° C)	10^{13} Ω -cm
Dielectric Constant (1MHz)	4.5 max.
Flexural Strength	19,000 PSI
Impact Strength	2.5 kgf • cm/mm^2
Free Na^+	5 PPM max.
Free Cl^-	5 PPM max.
Hydrolyzable Chlorine	300 PPM max.

[1] Sumitomo Bakelite Company data sheet

Lead Finish

Monolithic Memories Incorporated molded devices come standard with 300 - 600 micro inches of tin plating on all exposed leads. This finish provides the user with a solderable surface for PC board attachment.

In addition to tin plating, Monolithic Memories Incorporated offers a solder dip finish. This finish puts a coating of solder on all exposed metal and results in excellent solderability of the finished package.

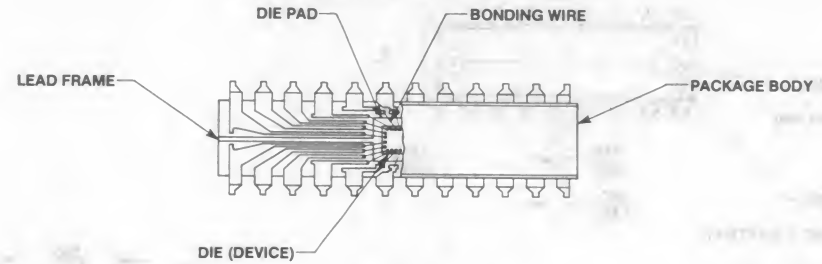
Die Attach Pad/Bonding

Monolithic Memories Incorporated utilizes high strength conductive epoxy to attach die to P-Dip leadframes. The leadframe is plated with 150 micro inches of silver in the die attach area to enhance the strength and reliability of the bond.

*Epoxy Characteristics (typical)	
Specific Gravity	2.31
Shore "D" Hardness (ASTM-D-1706)	84
Coefficient of Thermal Expansion (cm/cm° C)	2.5×10^{-5}
Tensile Strength (ASTM-D-1002)	
Measured at 25° C	2,100 PSI
Measured at 85° C	1,500 PSI
Volume Resistivity (ohm - cm, 25° C - 155° C)	.001
Resistivity After 200 Hrs. Aging at 180° C	.0001

* Amicon Corporation data sheet

Molded Package



LEAD FRAME

1. Copper Alloy 195.
2. Copper Alloy Tamac 5.

BONDING WIRE

1. 1.00 Mil Gold Wire.
2. 1.25 Mil Gold Wire.
3. 1.30 Mil Gold Wire.

PACKAGE BODY

Thermoset Plastic.

LEAD FINISH

1. Tin Plating.
2. Solder Dip.

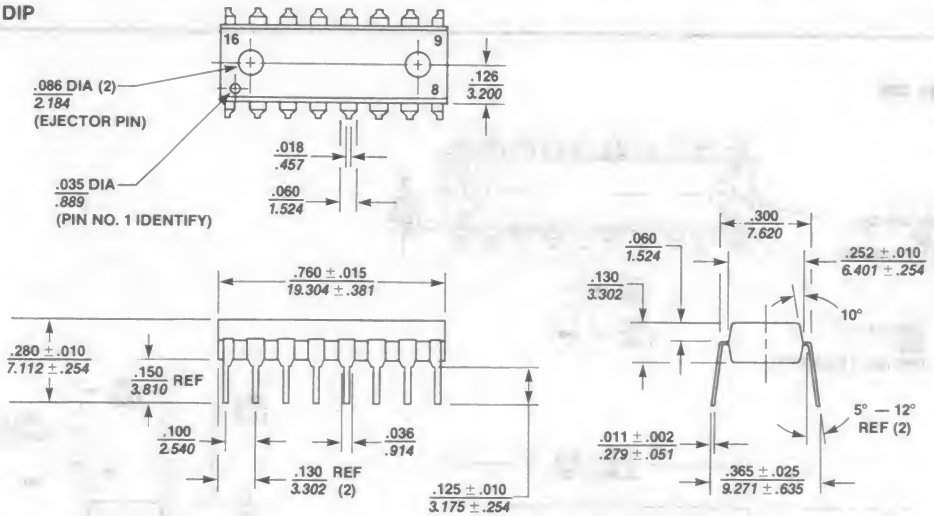
DIE PAD

Spot Silver Plating
(150 Micro - Inches).

DIE BOND

Silver Filled Epoxy.

N16 Molded DIP

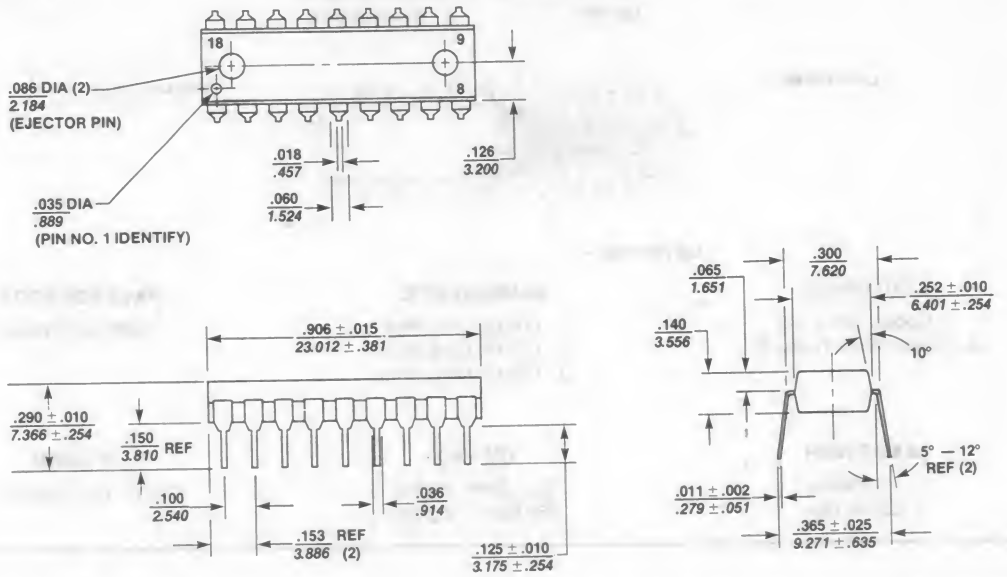


NOTES:

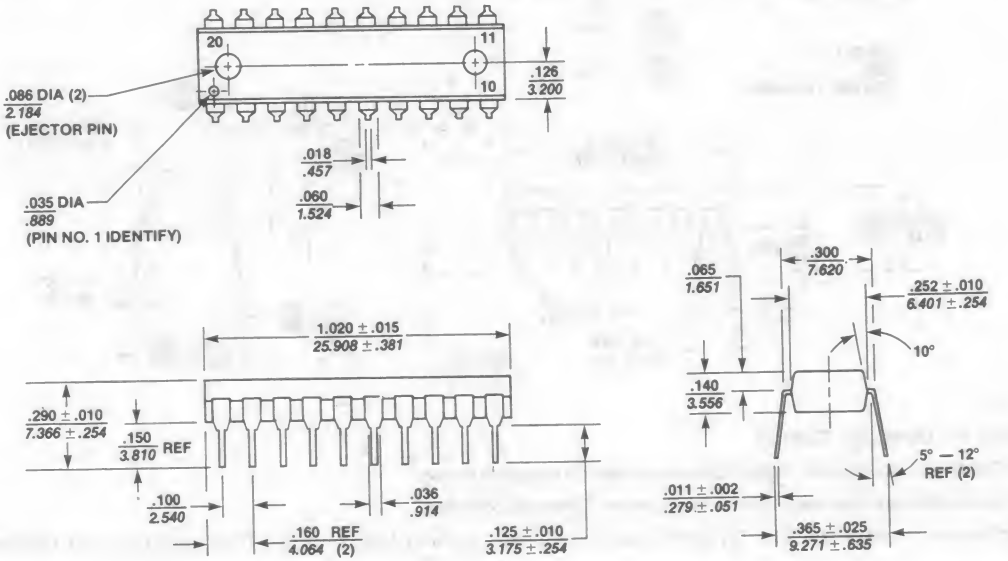
1. Ejector Pin Marks Are Optional.
2. Top Dimension Specified in Inches. Bottom dimension specified in mm.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

15

N18 Molded DIP



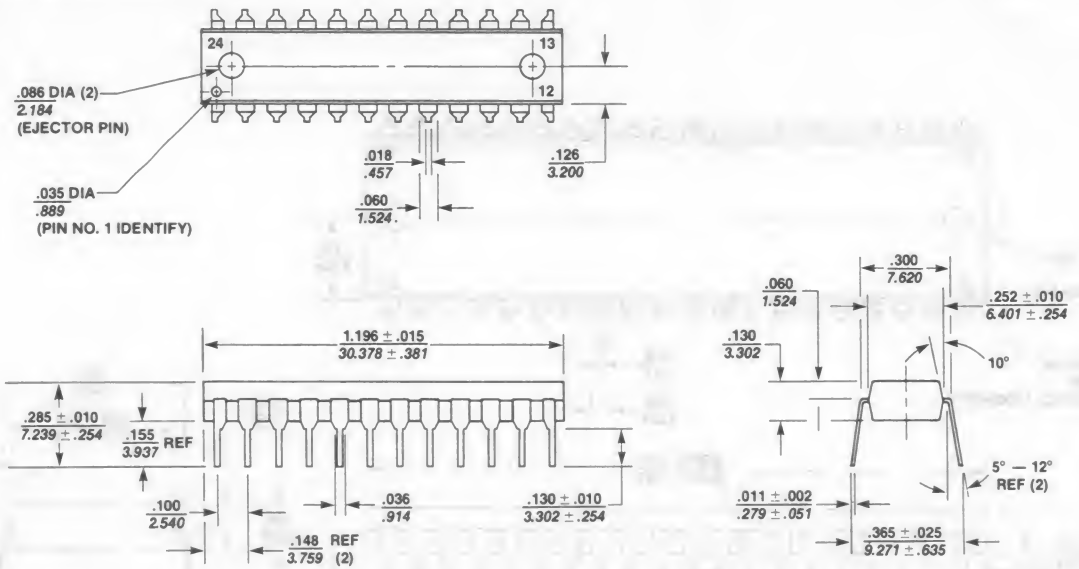
N20 Molded DIP



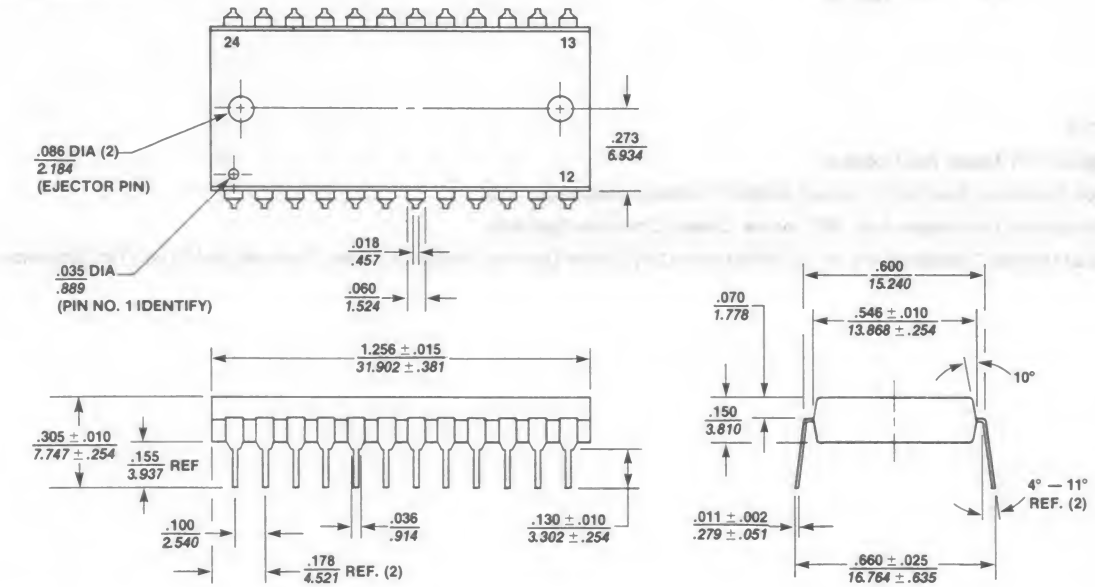
NOTES:

1. Ejector Pin Marks Are Optional.
2. Top Dimension Specified in Inches. Bottom dimension specified in mm.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

N24S Molded SKINNYDIP



N24 Molded DIP



NOTES:

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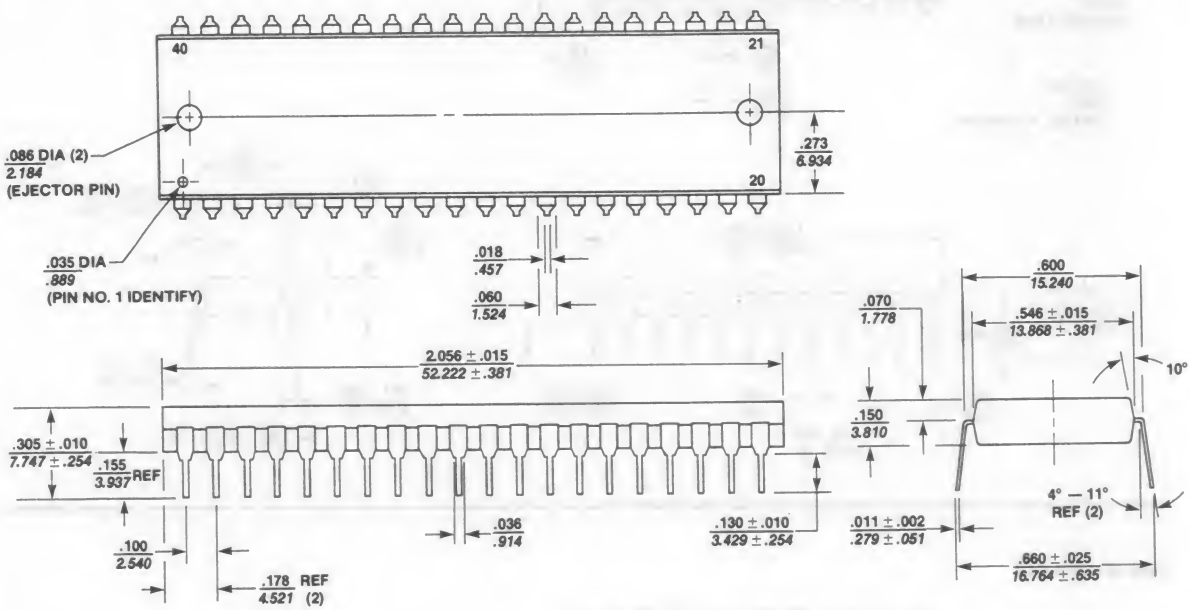
2. Top Dimension Specified in Inches. Bottom dimension specified in mm.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.,
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

N40 Molded DIP



NOTES:

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3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
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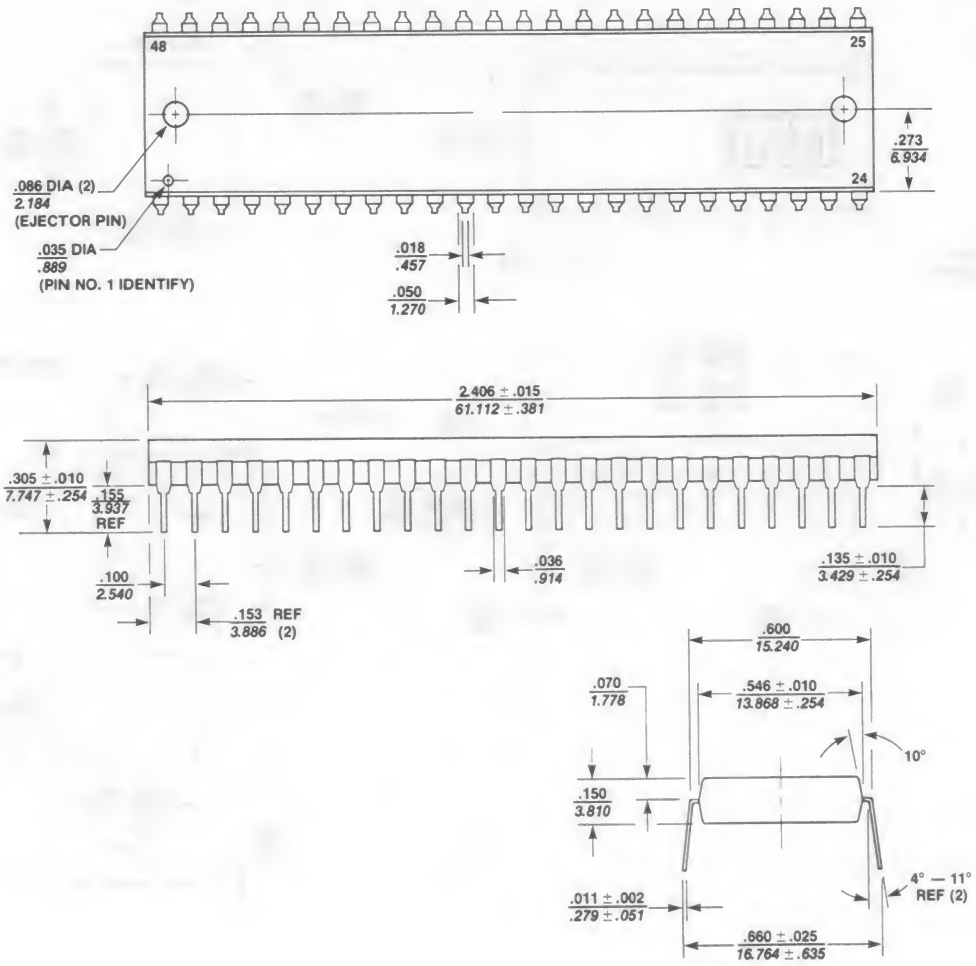
N48 Molded DIP



NOTES:

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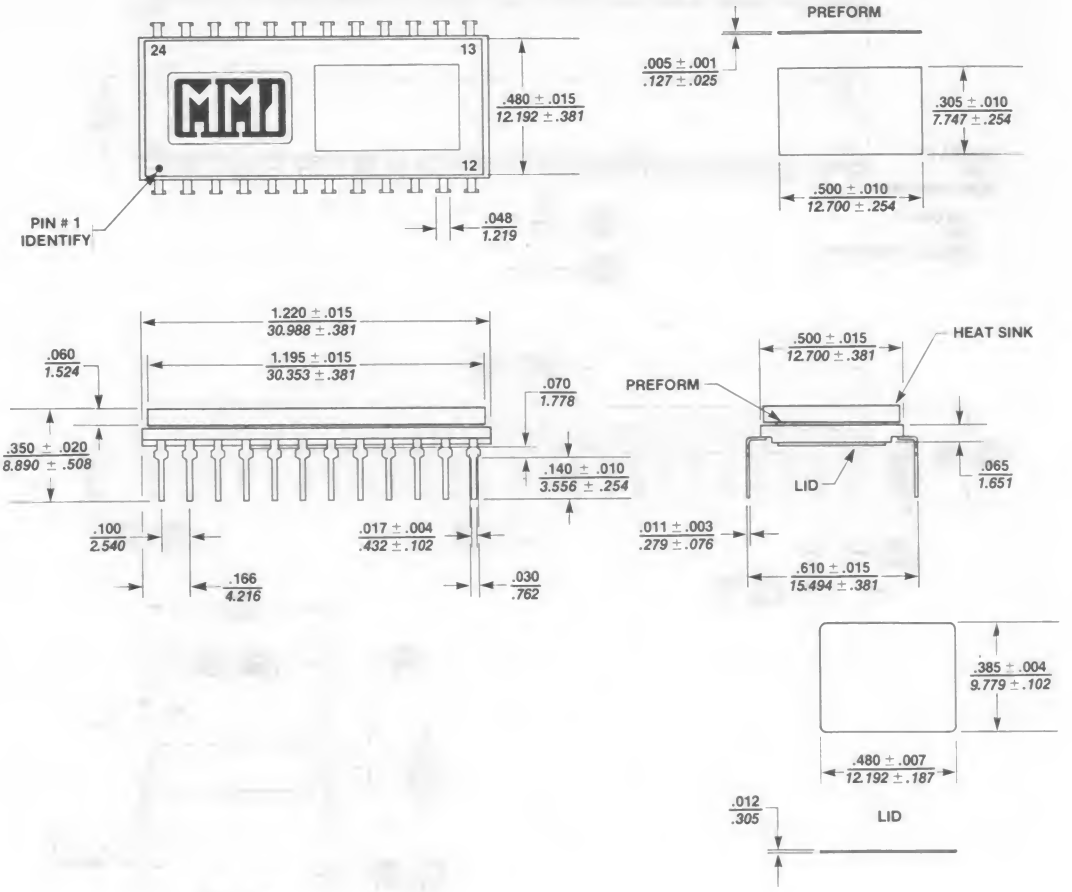
2. Top Dimension Specified in Inches. Bottom dimension specified in mm.
3. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.
4. Lead Material Tolerances Are for Tin Plate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

15

T24 Top Brazed Ceramic DIP
(With Heat Sink)

Top Brazed Heat Sink Package

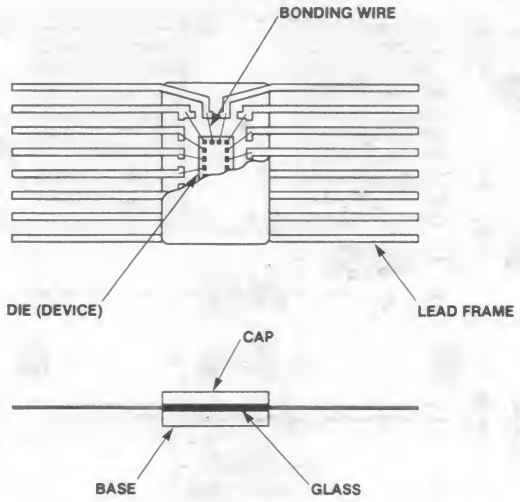


NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
2. All Nominal Dimensions Are ± .007 inches Unless Otherwise Specified.

PACKAGE BODY	LID	LEAD MATERIAL	BONDING WIRE
Alumina	Metal (Plated Kovar) Soldered to Seal Ring.	Alloy 42	1.25 Mil Aluminum
CAVITY	**LEAD FINISH**	**HEAT SINK**	**PREFORM**
Gold Over Tungsten For Eutectic Die Attach	1. Gold Plate (Standard) 2. Solder Dip Over Gold Plate.	Blue Anodized Aluminum	Conductive Epoxy

Cerpack



LEAD FRAME
Alloy 42

BONDING WIRE
1.25 Aluminum

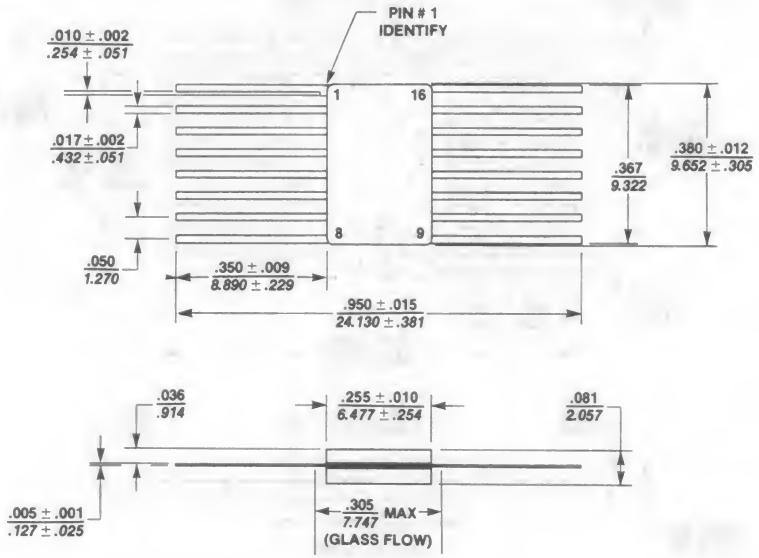
CAP AND BASE
Pressed Alumina

GLASS
LS-0113

CAVITY
Gold Over Alumina
For Eutectic Die Attach

LEAD FINISH
1. Bright Tin
2. Solder Dip

W16 CERPACK



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
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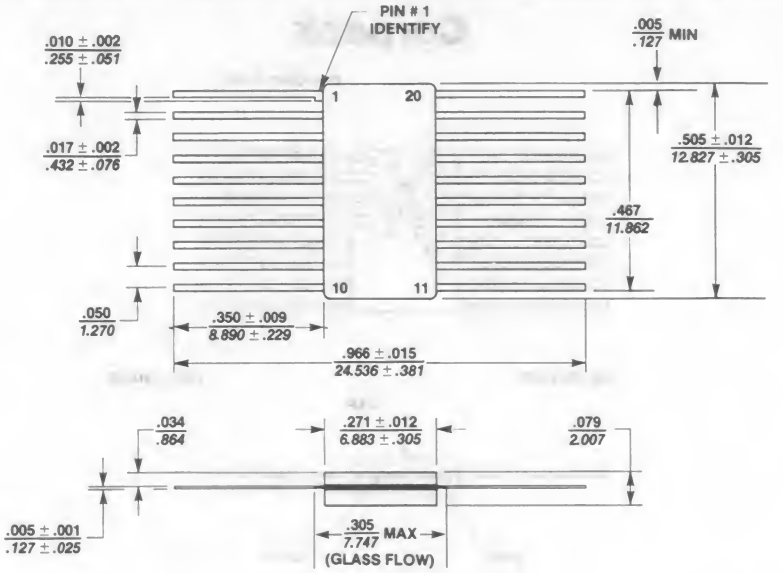
3. Lead Material Tolerances Are for TinPlate Finish Only. Solder Dip Finish Adds 2 - 10 Mils Thickness to All Lead Tip Dimensions.

W20 CERPACK



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
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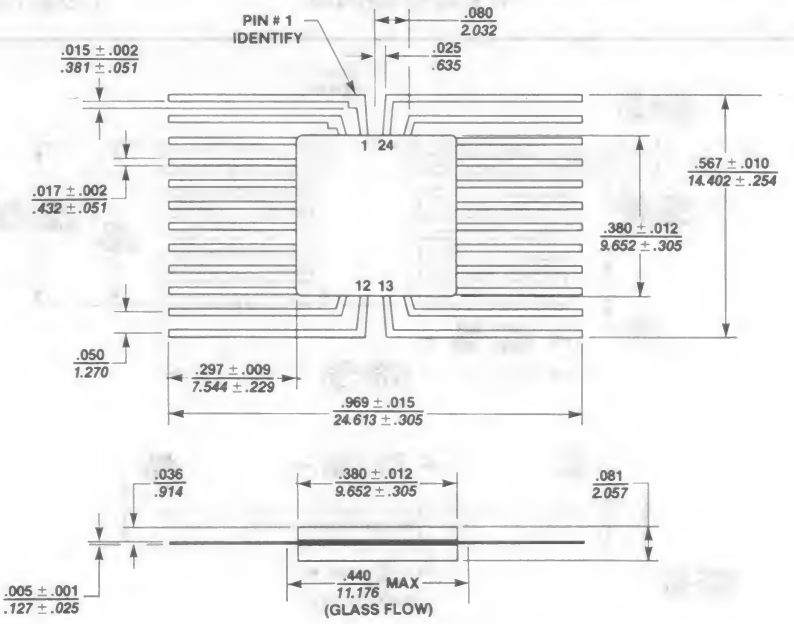
W24 CERPACK



NOTES:

1. Top Dimension Specified in Inches. Bottom Dimension Specified in mm.
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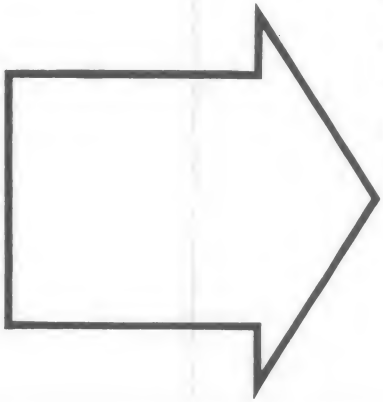

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